A 23.5GHz PLL with an adaptively biased VCO in 32nm SOI-CMOS

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***Abstract*- A 30% frequency tuning range 23.5GHz 32nm SOI-CMOS PLL features an adaptively biased VCO. Adaptive biasing of the VCO lowers the average PLL power consumption from 34mW to 24mW, while keeping the jitter below 1.5^{o} RMS across all frequency bands.**

I. Introduction

High-performance PLLs targeting 60GHz wireless communications have been recently reported [1-3]. In CMOS implementations, a 20-26GHz PLL followed by a frequency doubler is an attractive approach as the performance of both the active and passive devices is significantly better at lower frequencies. However, the design of low-phase-noise wide-tuning-range VCOs (>20% range) above 20GHz presents significant design challenges, as at these frequencies both the analog varactors and digitally switched capacitors suffer from a significant degradation of their quality factor and tuning range. At these frequencies the quality factor of the passives are typically frequency dependant, which results in a large variation in the VCO's phase noise performance. As a consequence a VCO with a fixed bias current, chosen so that the jitter meets system specifications at all frequencies, will at some frequencies perform better than required, which results in a waste of power. For high data rate portable wireless applications, such a PLL must achieve low phase noise while minimizing power consumption, which motivates the work presented here.

This paper presents an adaptive broadband PLL with a center frequency of 23.5GHz, tuning range of 30%, a RMS jitter of better than 1.5^{o}. The average power consumption is minimized by reducing the VCO current at frequencies at which less power is required to meet the performance specification. At frequencies at which achieving good jitter performance is most challenging, the bias current is increased. In this way the larges VCO bias current is only use when required; at other frequencies the bias current is reduced.

The VCO architecture is similar to the noise-shifting Colpitts, which was presented in [4]. This architecture has been shown to combine the strong phase noise performance of the classical Colpitts architecture with the advantages of differential oscillation. In addition, a well know limitation of the classical Colpitts architecture is that generating sufficient loop gain so as to guarantee startup is more challenging relative to a cross-coupled VCO. For oscillators operating in the K-band range guaranteeing oscillator start-up is more challenging than at lower frequencies. This is because as frequency increases active devices have less gain, and passive devices are more lossy. As discussed in [4], this new architecture has significantly more gain than a conventional Colpitts VCO. In this work we demonstrate that this VCO architecture is an attractive topology for K-band oscillators, as it combines the strong phase noise performance of Colpitts oscillators, without degrading the oscillators ability to robustly start-up, even at K-band frequencies.

In section II we will present the details of the VCO. In section III we will provide an overview of the remainder of the PLL, and additional peripheral support circuits which are required for the adaptive biasing scheme. In section IV we will present the measurements, and we present our conclusions in section V.

II. VCO Design

As discussed above, the VCO is a variant of the noise-shifting differential Colpitts VCO [4], and it can simultaneously provide a wide tuning range and low phase noise. The VCO is comprised of two common-gate Colpitts oscillators stacked on top of a cross-coupled differential pair (Fig. 1). The VCO current is controlled by changing the voltage bias of the common-gate Colpitts FETs. This critical noise sensitive node is digitally controlled with a low-noise resistor-ladder based 5-bit DAC. The 160pH tank inductor is implemented in a horseshoe symmetrical configuration in order to reduce parasitic resistance and capacitance. The resonator's capacitor is segmented into 3-bit binary and 10-bit thermometer banks to reduce the VCO gain and guarantee large band overlap.

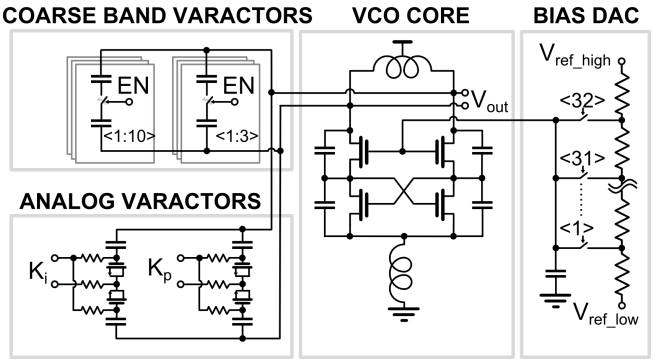

Fig. 1. Details of the modified Colpitts oscillator.

The proportional and integral analog controls required for the dual-path PLL (see section III) are designed using accumulation varactors which are isolated from the tank with back-end-of-the-line (BEOL) capacitors. This reduces VCO frequency pushing due to supply voltage variation and rejects input common-mode noise. The output of the VCO is buffered by a series of differential CML-style amplifiers (four cascaded

differential pair stages with NFET widths from 5um to 35um). The last stage is an open drain configuration with 20mA bias current and can deliver 3dBm differential output power into a 50Ω load at 25GHz.

II. PLL Architecture

An overview of the PLL architecture is shown in Fig. 2. Key components include the VCO, a divide-by-16 prescalar, a programmable divider, and a classical tri-state phase detector. The control loop is split into a proportional and an integral path control. The proportional path consists of a charge pump and a programmable loop filter. The integral path consists of a charge pump and a digital programmable capacitor. Details of the control loop can be found in [6]. The VCO amplitude is measured using an on-chip peak detector. The peak-detector consists of a rectifier and low pass filter. The output of the peak-detector consists of a low frequency signal which is proportional to the VCO amplitude. The input devices of the peak-detector were carefully sized so as to minimize the loading of the VCO. An integrated 6-bit SAR ADC digitized the peak detector output. An on-chip state machine uses the quantized output to control a voltage DAC that biases the VCO. The state machine and the PLL can be programmed externally through the serial interface.

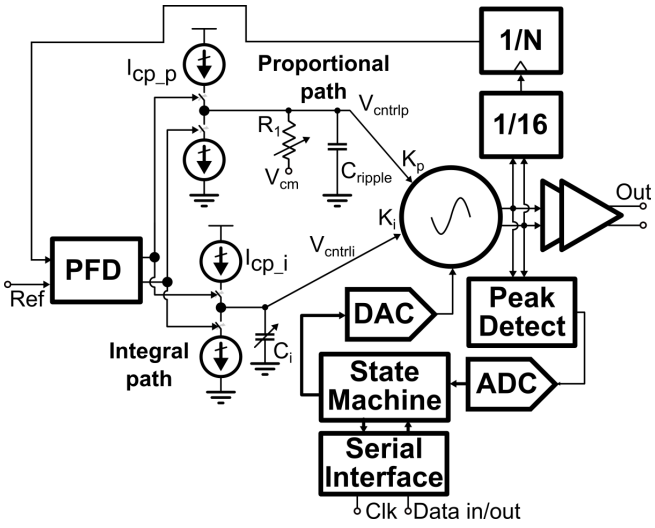

Fig. 2. Simplified PLL block diagram.

IV. Measurements Results

Fig. 3 shows the measured VCO output frequency versus the digitally controlled capacitor bank settings, with the analog varactor switched both high and low. (Note that there are two sets of digitally controlled capacitors: a 3-bit coarse band with binary weighting and a 10-bit fine band with thermometer weighting). As can been seen in Fig. 3, there is ample frequency overlap between all adjacent VCO bands. The measured frequency tuning range of 29.8% is the highest reported at this frequency. Spurious tones are below -85dBc between 500kHz and 1GHz which is 35dB lower than reported in [2].

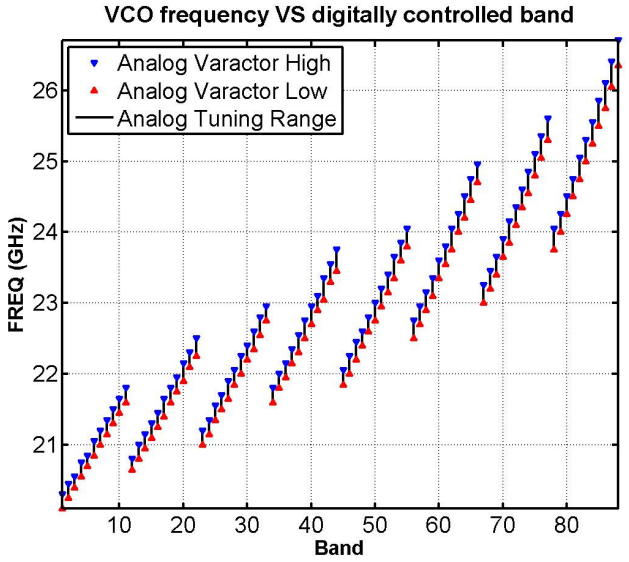

Fig. 3. VCO frequency range and band overlap.

Fig. 4 shows a measured phase noise spectrum, at an output frequency of 23.05GHz. The noise at 10MHz offset from the 23.05GHz carrier is -124.2dBc/Hz (Fig. 4) which is a 3.2dB improvement over [2].

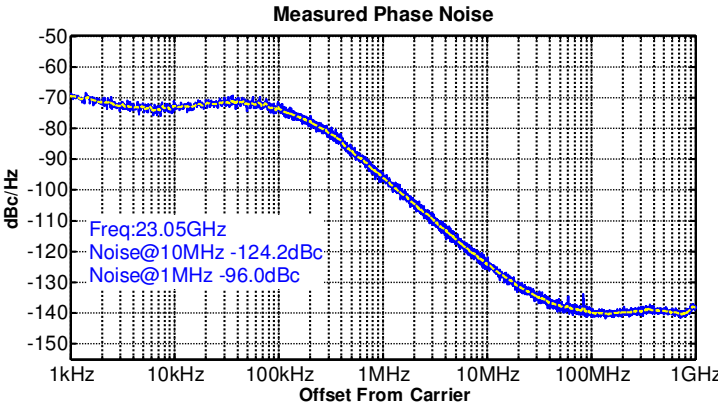

Fig. 4. Measured PLL phase noise at 23.1GHz.

The measured phase noise as function of the VCO bias current has more than 6dB variation and exhibits a minimum which corresponds to the current bias that achieves the best VCO signal to noise ratio (Fig. 5).

Since the resonator Q and NFET performance degrade as frequency increases the phase noise minimum follows the same degradation trend. As shown in figure 6, the measured RMS jitter (integrated between 1MHz and 1GHz) shown for each band as a function of biasing current exhibits a minimum for each band and degrades as band or frequency is increased.

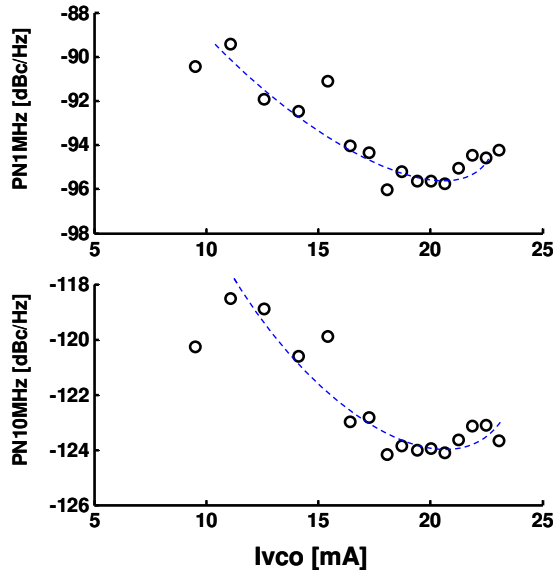

Fig. 5. 1 MHz and 10 MHz phase noise versus VCO current.

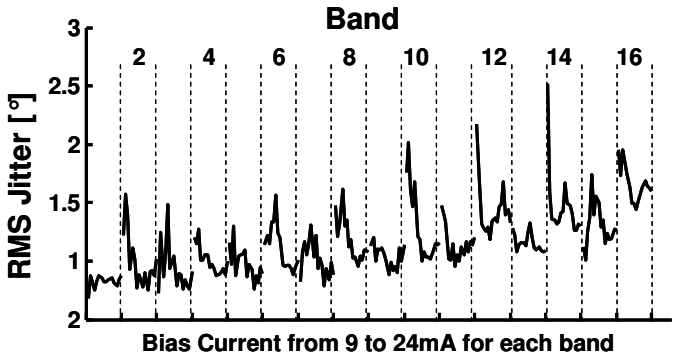

Fig. 6. Measured RMS jitter in degrees across bands and DAC settings.

It is also useful to note that in a typical communication system the PLL jitter performance is specified in RMS degrees, in order to achieve a targeted Bit Error Rate (BER). Maintaining a constant BER versus carrier frequency does not imply that the phase noise performance versus frequency is required to be constant. This can be simply explained by the relationship between RMS jitter in (s) and in (°) which is given by:

$$Jitter(s) = \frac{Jitter(^{o})}{360 \cdot F_{osc}} \qquad (1)$$

Therefore for a given RMS jitter in degrees specification, the RMS jitter in second decreases as frequency increases. This demonstrates that the PLL phase noise can be higher at the lowest frequency as compared to the highest frequency, and still achieve the same BER.

Based on this observation and the measurements, an adaptive VCO biasing strategy can be compared to a static bias approach. For a static VCO bias, the best static DAC current setting is the one that minimizes the worst-case RMS jitter across all the bands (Fig. 7). In the adaptive bias approach, the minimum RMS jitter as function of VCO bias current is first searched by going through all the VCO DAC settings. A measured RMS jitter minimum of 1.5° is found at the highest frequency band for a VCO biasing current of 17mA. For all the other frequency bands, the VCO is biased first at the minimum bias current; if the measured RMS jitter is higher than 1.5° the VCO bias current is increased to the point where the RMS jitter is less than 1.5°. This is the minimum VCO current bias required to meet a fixed angular RMS jitter target.

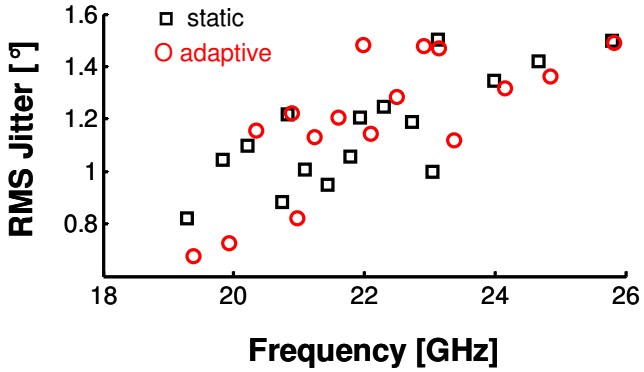

Fig. 7. Third measured RMS jitter in degree for static and adaptive bias.

This algorithm takes advantage of three fundamental properties to decrease PLL power consumption: the existence of a jitter minimum as a function of VCO current, the improvement of the resonator Q at low frequencies, and the linear decreased jitter in degrees for a constant jitter in seconds as frequency decreases. As shown in Fig. 8, the adaptive bias allows the average VCO current to be reduced from 18.2mA to 10.4mA.

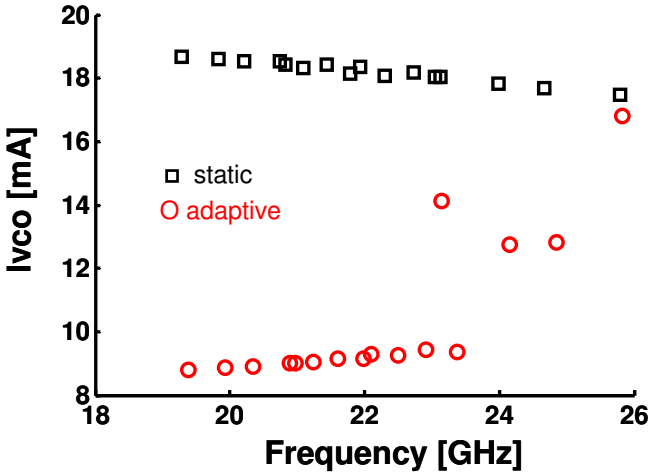

Fig. 8. Measured VCO current for static and adaptive bias.

For a static bias the PLL consumes an average total power of 34mW (excluding input and output buffers). However for an adaptive bias the average PLL power consumption across

the frequency range is reduced to 24mW. This is equivalent to a 29% reduction of the average PLL power consumption. This algorithm can be implemented in the integrated digital state machine following the methodology described in [5]. All circuits operate at 0.95V other than the VCO, which runs at 1.3V. The chip and active area are 0.96 mm^2 and 0.45 mm^2, respectively (Fig. 9).

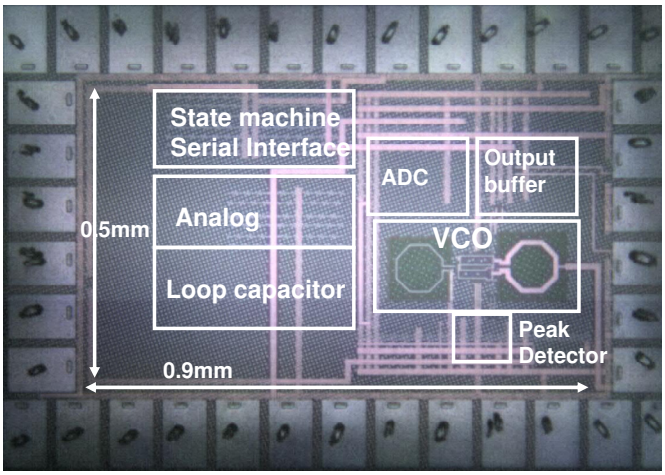

Fig. 9. Chip microphotograph.

Table I. Measurements Summary

	This work	[2]
Technology	32nm SOI	45nm CMOS
Center Frequency [GHz]	23.5	24.8
tuning range [%]	30	25
Filter type	on-chip programmable	External
10MHz Phase Noise [dBc/Hz]	-125.9 @ 23.4GHz	-121 @ 23.3GHz
RMS jitter [^{o}]	1.2 (1MHz-1GHz)*	1.3 (1MHz-100MHz)†
power bias [mW]	24*	32.3†
Ref. Spur [dBc]	-85	-50
Active area [mm^2]	0.9x0.5	0.48x0.29

*averaged on 16 frequency bands
†only 1 frequency available

V. Conclusion

A 23.5GHz PLL was implemented in a 32nm SOI technology. The modified Colpitts VCO exhibits broad 30% tuning range and record phase noise of -125.9dBc/Hz at 10MHz offset of the 23.4GHz carrier. By using adaptative biasing an average 1.2^o RMS jitter integrated from 1MHz to 1GHz is achieved at an average power of 24mW. The PLL is integrated in an area of 0.9 by 0.5 mm^2.

Acknowledgments

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