

3D Radar Imaging based on a Synthetic Array of 30GHz Impulse Radiators with On-Chip Antennas in 130nm SiGe BiCMOS

Peiyu Chen, *Student Member, IEEE*, and Aydin Babakhani, *Member, IEEE*

Abstract— We report a 30GHz impulse radiator chip for high-resolution 3D radar imaging. In this work, an asymmetrical topology in the cross-coupled pulsed VCO is introduced to minimize timing jitter of radiated impulses to 178fs, which enables highly efficient spatial combining. The coherent combining over the air has been performed with two widely spaced impulse radiators. The shortest FWHM pulse-width of 60ps is recorded. 3D images of various metallic objects and dielectric objects are produced using a custom-designed synthetic array imaging system. A depth resolution of 9mm and a lateral resolution of 8mm at a range of 10cm have been achieved. The impulse radiator was implemented in the IBM 130nm SiGe BiCMOS process technology with an area of 2.85mm² and an average power consumption of 106mW.

Index Terms—3D imaging, VCO, impulse radiator, on-chip antennas, radars & broadband systems, synthetic array, Silicon RFIC, SiGe BiCMOS, spatial power combining.

I. INTRODUCTION

OVER the past decade, microwave and mm-wave impulse radiators have been reported for short-range high-data rate communication [1], [2], [3], vital-signal monitoring [4], [5], security imaging [6], [7], [8], spectroscopy [9], [10], [11], and short-range automotive radar [12], [13], [14], [15]. Impulse radiators have three main advantages compared with continuous-wave (CW) radiators. First, impulse radiators have larger instantaneous bandwidth than CW radiators. Second, timing ambiguity can be suppressed without sacrificing image resolution by using repeated ultra-short impulses with a large repetition period. Third, energy consumption of impulse radiators can be easily adjusted by varying the repetition rate of radiated impulses.

Over the last few years, several groups have reported silicon-based mm-wave impulse radiators for imaging applications [16], [17], [18], [19], [20], [21]. Main objectives in designing silicon-based imaging radars are high image resolution, large image range, and short acquisition time. There exists a trade-off between higher image resolution and larger image range: Higher image resolution requires larger bandwidth of shorter impulses, but shorter impulses have

lower peak power, which degrades SNR and image range. This trade-off can be mitigated by coherent combining of radiated impulses over the air. By synchronizing radiators and applying proper time-delay to each radiator, the radiated impulses can be combined coherently at a certain point in 3D space. As a result, SNR at the combining point is increased quadratically as a function of the number of radiators.

The majority of published studies on silicon-based impulse radiators adopt oscillator-based architectures [19], [20], [21]. In [19], co-locked delay-lock-loop (DLL) and PLL were used to generate coherent impulses, resulting in a significant increase in power consumption, system complexity, and die area. In addition, only distance measurement (1D imaging) was performed in [19]. In [20], impulse-based 3D imaging was demonstrated by using a 4TX/4RX radar with electronic scanning, but two large high-gain (40dBi) reflector dishes were used to improve image resolution and range. Off-chip antennas were used to radiate and receive impulses. Therefore, the imaging system in [20] is bulky and lacks potential in further miniaturization. In [21], 2D localization measurement of a metal plate was performed by using a coherent UWB MIMO radar operating at 26GHz. In [21], no imaging was reported. Furthermore, the size of the MIMO radar was large due to the PCB-based transmitter and receiver antennas.

This paper is an extension of [22] with detailed simulations, updated measurement results, and more 3D radar imaging results. The impulse radiator converted an input digital trigger signal to radiated impulses with accurate timing, which is required by synthetic array 3D radar imaging. In contrast to previous designs [19], [20], [21], no PLL or DLL is required in this design. The asymmetric pulsed VCO topology is introduced to minimize timing jitter of radiated impulses. The design target FWHM pulse-width is 74ps, which matches closely with the measurement result. The whole system, including the on-chip antenna, has a 3dB bandwidth of 11GHz and a 6dB bandwidth of 23GHz. In the measurement, by optimizing the bias voltages, a shortest FWHM pulse-width of 60ps is recorded. In addition, coherent impulse combining over the air is performed by using two widely spaced radiators. Furthermore, high-resolution 3D imaging of metallic objects and dielectric objects are demonstrated.

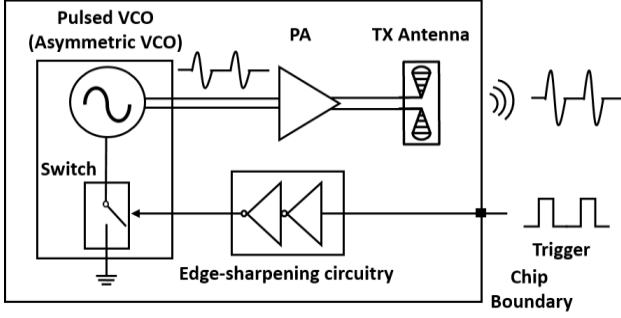


Fig. 1. System architecture of the 30GHz impulse radiator (pulsed-VCO-based architecture).

II. 30GHZ IMPULSE RADIATOR

The 30GHz impulse radiator designed in this work adopts a pulsed-VCO-based system architecture, as shown in Fig. 1. Compared with carrier-based architecture [19], [23], pulsed-VCO-based architecture [21], [24], [25], [26] has some intrinsic advantages: First, the pulsed VCO is switched on and off by a trigger signal to generate short impulses. Therefore, imaging sensitivity is enhanced due to zero leakage to RX from the pulsed VCO. Second, the pulsed VCO can be designed to ensure coherency of generated impulses [24], [25], [26], eliminating the need for co-locked PLL or DLL.

The designed 30GHz impulse radiator consists of an edge-sharpening circuitry, a pulsed VCO with asymmetric cross-coupled topology, a power amplifier, and an on-chip bowtie antenna (Fig. 1). The input trigger signal is a digital square wave, which is fed to the edge-sharpening block. This block is a two-stage digital inverter that switches the current source of the pulsed VCO. The input impedance of the edge-sharpening circuitry is designed to be 50Ω to minimize the reflection of the input trigger signal. The edge-sharpening circuitry consumes 8.4mW.

A. 30GHz Pulsed VCO

In order to radiate short impulses with large amplitude, the startup time of the pulsed VCO needs to be short [26]. Additionally, generating coherent impulses for efficient beamforming requires that the phase of the generated impulses must be locked with that of the input trigger signal. Therefore, two more requirements need to be achieved: first, the initial phase of the impulse signal must be deterministic; second, the timing jitter added by the pulsed VCO must be minimized. In this work, the timing jitter is defined as standard deviations of $\Delta\phi_i$ shown in Fig. 2

$$\text{Timing Jitter} = \sqrt{\frac{1}{N} \sum_{i=1}^N |\Delta\phi_i - \mu|^2} \quad (1)$$

where $\Delta\phi_i$ is the timing difference in one period between time t_{ia} when the generated impulse is at its minimum amplitude and time t_{ib} when the trigger signal is at 50% of its amplitude

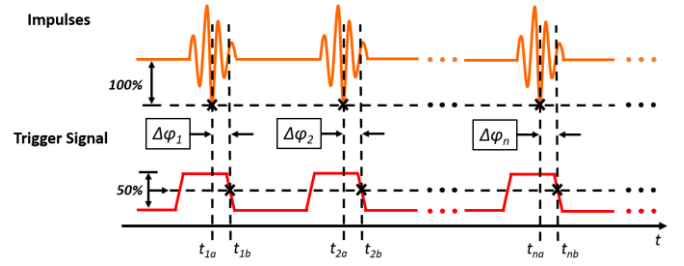


Fig. 2. Timing relationship between the generated impulses and the input trigger signal.

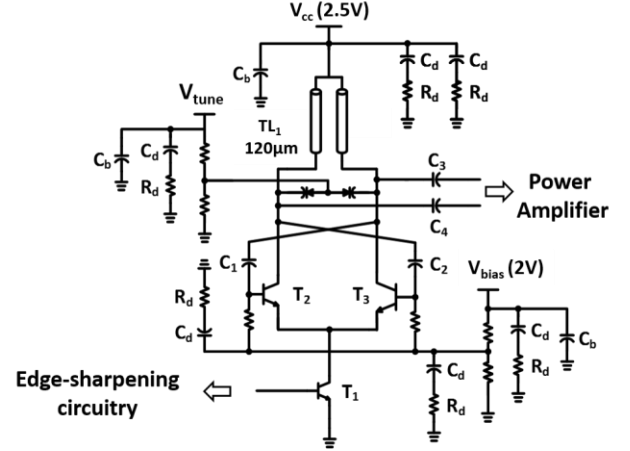


Fig. 3. Schematic of the 30GHz pulsed asymmetric cross-coupled VCO.

on its falling edge, and $\mu = \frac{1}{N} \sum_{i=1}^N \Delta\phi_i$.

Schematic of the pulsed VCO is shown in Fig. 3. An asymmetric cross-coupled topology is introduced to minimize timing jitter. The preceding edge-sharpening circuitry drives the current source T_1 . Emitter length ratio between transistors T_2 and T_3 is optimized to be 1:3 to minimize timing jitter. Two identical capacitors, C_1 and C_2 , boost the oscillation amplitude and hence phase noise is reduced. Two varactors are used to adjust oscillation frequency by applying tuning voltage at the common anode. An impedance matching network, consisting of the differential transmission line TL_1 , capacitors C_3 and C_4 , provides the required inductance for resonance from 30GHz to 35GHz, and also enables maximum power delivery from the pulsed VCO to the following power amplifier. Bypass capacitors C_b filter out the noise from bias voltages V_{cc} , V_{bias} , and V_{tune} . De-Q blocks, consisting of capacitors C_d and resistors R_d in series, eliminate undesired low-frequency common-mode oscillations caused by wirebonds.

As discussed earlier, startup time of the pulsed VCO needs to be short. An approximate startup transient response for differential output of oscillators can be expressed as [27]

$$v(t) = \frac{2v_0}{\sqrt{1 + \left(\frac{2v_0}{v(0)}\right)^2 - 1}} \cos(\omega_0 t - \phi) e^{-\epsilon\omega_0 t} \quad (2)$$

where $v(0)$ is the initial condition, $2v_0$ is the steady-state oscillation amplitude and ϵ is a damping factor. From (2), the startup time t_s for the oscillation $v(t)$ to reach 90% of its steady-state oscillation amplitude $2v_0$ is approximated as

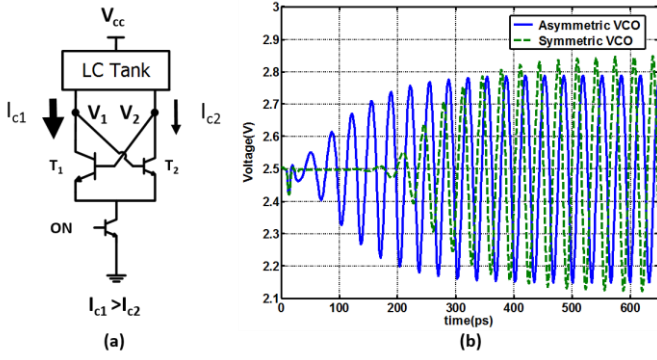


Fig. 4. (a) The initial collector current asymmetry in the asymmetric cross-coupled pulsed VCO. (b) Comparison between simulated oscillations of asymmetric VCO and symmetric VCO.

follows [26] [27],

$$t_s \approx \frac{C}{g_{m_eff}} \left[2 \ln \left(\frac{2v_0}{v(0)} - 1 \right) + 1.45 \right] \quad (3)$$

where g_{m_eff} is the effective average transconductance of transistors T_2 and T_3 in the asymmetric cross-coupled pair and C is the tank capacitance.

According to equation (3), to obtain a shorter startup time t_s , a larger initial condition $v(0)$ is required. In conventional (symmetric) cross-coupled pulsed VCOs, the initial condition is introduced by thermal noise. However, in the proposed asymmetric cross-coupled pulsed VCO, unbalanced initial collector current flows are generated when the pulsed VCO is switched on. The unbalanced current flows set the initial condition that is much stronger than thermal noise, as illustrated in Fig. 4(a). Therefore, the asymmetric cross-coupled pulsed VCO reduces the startup time (Fig. 4(b)).

In addition to reducing the startup time, the initial phase of the generated impulse signal should be deterministic. As stated above, the initial condition $v(0)$ of the asymmetric cross-coupled pulsed VCO is set by the unbalanced initial collector current flows, which are deterministic because they are controlled by a certain emitter length ratio of the asymmetric cross-coupled pair. As a result, the initial condition is deterministic, resulting in a deterministic initial phase of the generated impulse signal, which is the second design requirement of the pulsed VCO.

The final design requirement of the pulsed VCO is that the timing jitter added by the pulsed VCO must be minimized. There are two sources of timing jitter: noise-induced perturbation during the startup time and phase noise in the steady-state oscillation. In designing pulsed VCO, these two timing jitter sources are equally important. As stated in [28], [29], a symmetric cross-coupled pair improves phase noise in the steady-state oscillation by achieving high CMRR and high differential gain but it suffers from unsuppressed noise perturbation in the startup time, because the initial condition $v(0)$ is set mostly by thermal noise. However, for the pulsed VCO with asymmetric cross-coupled pair, the initial condition

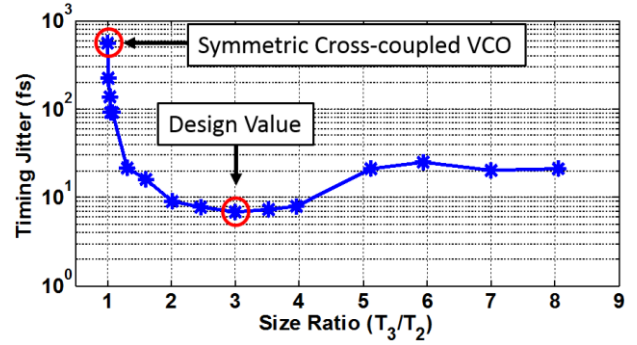


Fig. 5. Simulated timing jitter added by the pulsed VCO versus different emitter length ratios between transistors of the asymmetric cross-coupled pair.

$v(0)$ is predominately given by the deterministic unbalanced collector current flows when the pulsed VCO is switched on. The deliberate asymmetry in the cross-coupled pair suppresses the noise-induced perturbation in the startup time but sacrifices the phase noise performance in the steady-state oscillation. Therefore, there exists an optimum emitter length ratio of the two transistors in the cross-coupled pair for minimizing the timing jitter added by the pulsed VCO.

The summation of emitter lengths of transistors T_2 and T_3 is set to be $20.8\mu\text{m}$, which is limited by the power budget of the pulsed VCO. Timing jitter, as defined in Eq. (1), versus different emitter length ratios (T_3/T_2) is calculated from transient noise simulations. As shown in Fig. 5, the timing jitter is minimized to be 29.2fs at the emitter length ratio of 3:1, where the emitter length of T_2 is $5.2\mu\text{m}$ and the emitter length of T_3 is $15.6\mu\text{m}$. Fig. 5 shows that the timing jitter increases when the emitter length ratio between T_3 and T_2 approaches to 1, because the symmetric cross-coupled pulsed VCO has phase ambiguity at the startup time.

As discussed earlier, asymmetric cross-coupled VCO has a systematic tiny unbalance in the differential-mode outputs. In addition, unbalanced common-mode noise induced by the asymmetric cross-coupled pair slightly degrades phase noise performance, which is undesired in continuous-wave operations. However, instead of considering phase noise alone, minimizing timing jitter induced by the pulsed VCO is the objective, which is different from designing conventional VCOs. As a result, an asymmetric cross-coupled pair is designed with an optimum emitter length ratio of 1:3.

B. 30GHz Power Amplifier

In order to amplify impulses without distortions, the power amplifier is biased in the class A region and adopts a differential common-emitter topology, as shown in Fig. 6. $12 \times 0.12\mu\text{m}^2$ HBT npn transistors, T_1 and T_2 , are used as power transistors biased near their peak f_T current density at a quiescent current of $1.7\text{mA}/\mu\text{m}$. Fig. 7(a) presents the simulated output power contours of the PA core at 30GHz with respect to different differential load impedances. At the center frequency of 30GHz, the PA core generates a 14.5dBm output power with a $33 + j17.9\Omega$ differential load impedance. A revised single-stub shunt-matching network, noted in Fig. 6, is implemented with a simulated insertion loss of 1.5dB at

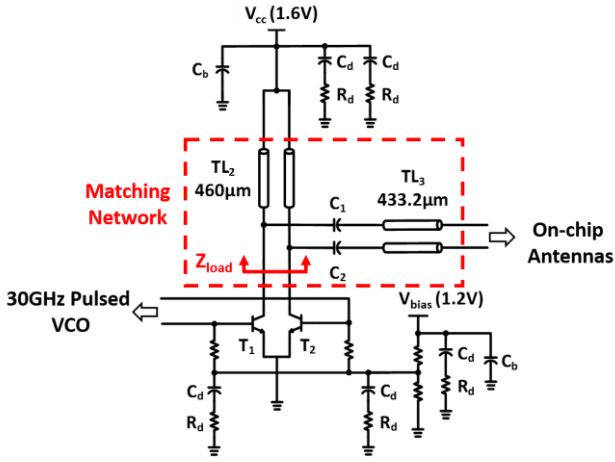


Fig. 6. Schematic of the 30GHz power amplifier.

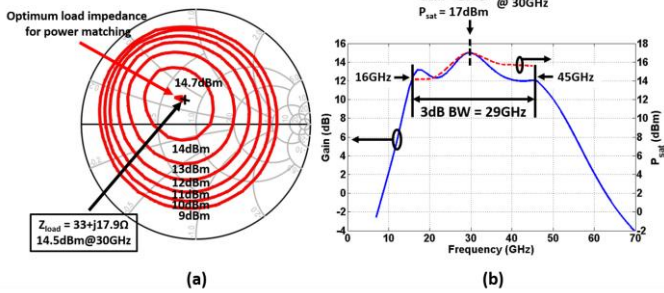


Fig. 7. (a) Simulated output power contours of the PA core at 30GHz. (b) Frequency response of the PA, including the matching network. The variation of simulated saturated output power is smaller than 3dBm within the 3dB bandwidth.

30GHz. The PA, including the matching network, has a 15dB simulated maximum power gain at 30GHz and a 3dB gain bandwidth of 29GHz, from 16GHz to 45GHz. Within the 3dB gain bandwidth, the variation of simulated saturated output power is within 3dBm, as shown in Fig. 7(b). De-Q blocks (C_d and R_d) and the parasitic resistance of metal interconnects ensure that both common-mode and differential-mode K-factors are greater than 1 in a wide frequency range from DC to 200GHz.

C. On-Chip Bowtie Antennas

In designing on-chip mm-wave antennas, surface waves are a major concern, because they degrade the radiation efficiency [30]. A Silicon lens [16], [23], [31] can be used to mitigate the surface wave problem, by collecting the surface waves and converting them to useful radiation. Unfortunately, attaching a silicon lens significantly increases the directivity of the on-chip antenna and limits the field-of-view. In this work, the impulse radiator chip is designed for short-range wide field-of-view 3D imaging. Therefore, adding a silicon lens is not a good choice for this work.

As suggested in [30], silicon substrate thickness can be optimized to increase radiation efficiency. Because wirebonds may affect topside radiations, the on-chip antennas are designed to radiate through substrate (bottom) side. Additionally, due to the die area constraints, the dimension of the on-chip antennas is limited to 2mm. Therefore, the on-

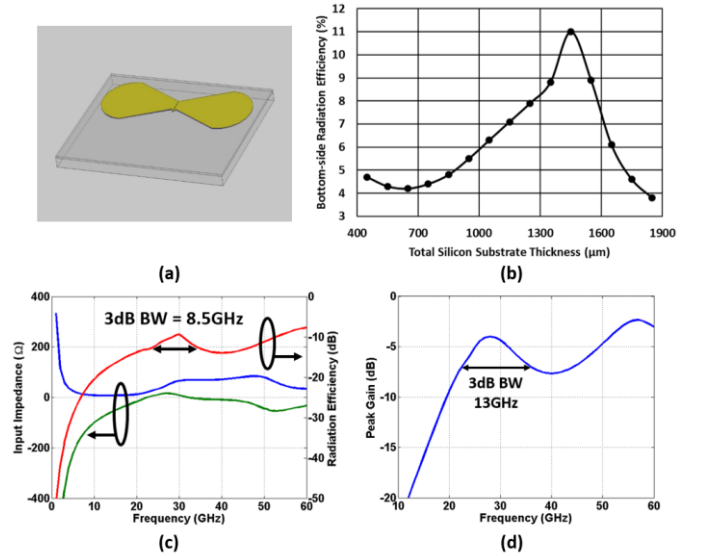


Fig. 8. (a) The designed on-chip bowtie antennas. (b) Simulated bottom-side radiation efficiency versus substrate thickness at 30GHz. (c) Simulated input impedance and radiation efficiency of the antenna versus frequency. (d) Simulated peak gain of the backside radiation of the antenna.

chip antenna can be considered as a small antenna at 30GHz. As discussed in section III, an undoped silicon slab is used to minimize the propagation loss and provide mechanical stability.

A moment-based electromagnetics simulator, HyperLynx 3D [32], is used to simulate the on-chip antenna and the silicon slab. As shown in Fig. 8(b), without grinding the chip substrate, when the total substrate thickness, including the chip substrate and the additional silicon wafer, is a half-dielectric wavelength at 30GHz, approximately 1440 μ m, the on-chip bowtie antenna has a peak radiation efficiency of 11% for bottom radiation. Fig. 8(c) and (d) demonstrate that, with 1440 μ m silicon substrate, the on-chip bowtie antennas have a 3dB radiation efficiency bandwidth of 8.5GHz, and a 3dB peak gain bandwidth of 13GHz. The peak gain at 30GHz is -4.3dB.

D. System Performance

In this design, the input trigger signal is generated by an external arbitrary waveform generator (AWG). Fig. 9 shows the measured waveform of the trigger signal used in the measurement, which has a pulse shape with a FWHM pulse-width of 88ps. By changing the DC offset of this trigger signal using an external bias-tee, the switching-on duration of the pulsed VCO is adjustable, resulting in tuning the FWHM pulse-width of the radiated impulse continuously.¹ In the simulations (Fig. 9), the VCO is tuned to oscillate at 30GHz. When the DC offset of the trigger signal is adjusted so that the pulsed VCO has an 83ps switching-on duration in each period, the simulated radiated impulse signal has a FWHM pulse-

¹ The external distortion effects by PCB traces and wirebonds, slightly increases the switching-on duration of the pulsed VCO. But these effects can be compensated by tuning down the DC offset of the input trigger signal.

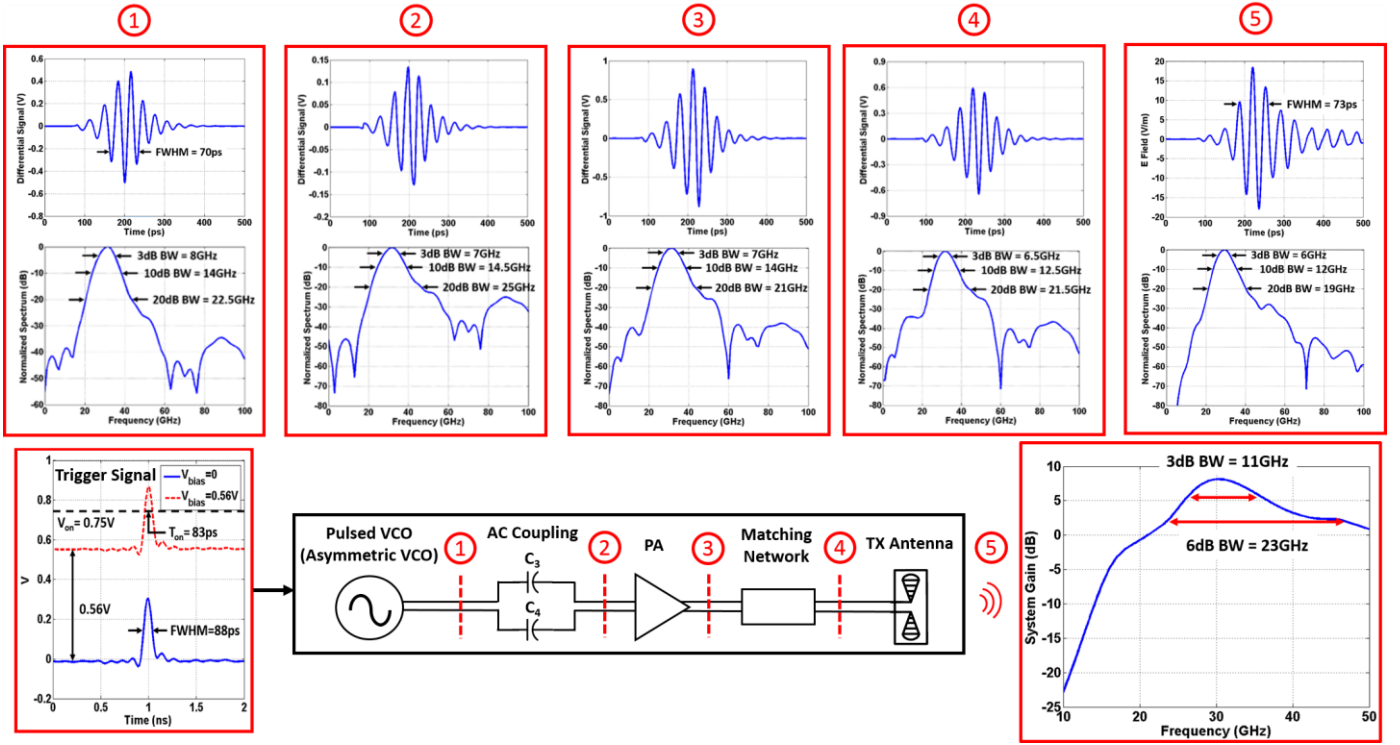


Fig. 9. Simulation details of the impulse signal from the asymmetric pulsed VCO in both time-domain and frequency-domain

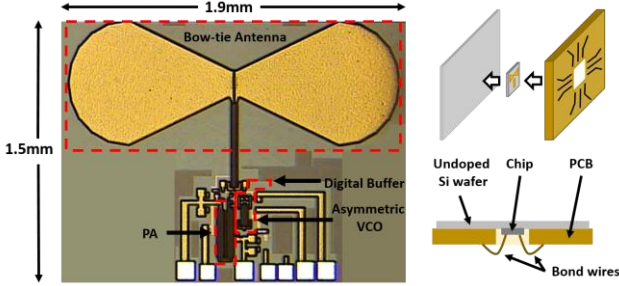


Fig. 10. Chip micrograph and chip assembly.

width of 73ps and a peak EIRP of 8.7dBm.²

Fig. 9 shows the evolution of the generated impulse signal from the asymmetric pulsed VCO to free space in both time-domain and frequency-domain. At the differential output node of the asymmetric pulsed VCO, the generated impulse signal has a 70ps FWHM pulse-width, with a 3dB bandwidth of 8GHz, from 27GHz to 35GHz, and a 20dB bandwidth of 22.5GHz, from 20.5GHz to 43GHz. Even though more even harmonics are generated due to the asymmetric topology of the pulsed VCO, it is not a concern for this impulse radiator.³ In terms of common-mode operations, the effects of the increased common-mode output from the asymmetric pulsed VCO is suppressed by the following differential PA and the

differential bowtie antennas due to their high CMRR.

In Fig. 9, the PA core and the following matching network reduce the 3dB bandwidth of the impulse signal slightly by 0.5GHz, due to the PA gain peaking at the center frequency of 30GHz (Fig. 7). Because the on-chip antenna is a small antenna at 30GHz limited by the die area, it has a smaller 3dB gain bandwidth than that of the PA, resulting in some late-time ringing shown in the simulated radiation waveform. The simulated radiated impulse signal has a 73ps FWHM pulse-width, with a 3dB bandwidth of 6GHz, from 26GHz to 32GHz, and a 20dB bandwidth of 19GHz, from 21GHz to 40GHz. Fig. 9 also presents the simulated system bandwidth, including the PA and the on-chip antennas. It has a 3dB bandwidth of 11GHz and a 6dB bandwidth of 23GHz. The main bandwidth limit in the system is the relatively small on-chip bowtie antennas. A FDTD-based 3D EM simulator, CST Microwave Studios [33], is used to simulate the time-domain performance of the on-chip differential bowtie antennas.

III. MEASUREMENT RESULTS

The 30GHz impulse radiator was fabricated in the IBM 130nm SiGe BiCMOS process technology. A micrograph of the chip, which occupies 1.9×1.5mm² die area, is shown in Fig. 10. The impulse radiator is mounted on a piece of undoped silicon slab that is glued to the backside of a Roger 4350B PCB, which has a cut-out to couple the radiation from the substrate side of the chip to air. Gold wirebonds are used to connect the on-chip pads to PCB traces (Fig. 10).

The impulse radiator is measured in both time-domain and frequency-domain. Fig. 11 illustrates the measurement setup. The trigger signal T is a 1GHz digital square wave signal,

² The simulated PA output power delivered to the antenna is 13dBm at 30GHz, including matching loss. Since the antenna has the simulated peak gain of -4.3dBi at 30GHz, the simulated peak EIRP at 30GHz is 8.7dBm.

³ The 2nd harmonic of the 3dB band of the generated impulse signal is from 54GHz to 70GHz, which lies out of the 20dB bandwidth of the impulse signal, resulting in negligible distortion effects on the generated impulse. In addition, the range from 54GHz to 70GHz lies out of the 3dB bandwidth of the designed power amplifier following the asymmetric VCO, as shown in Fig. 7(b).

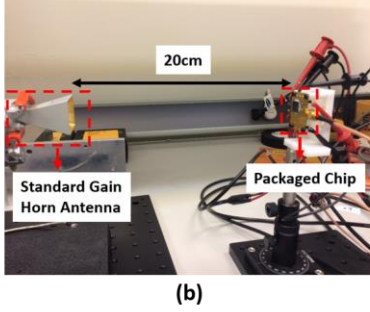
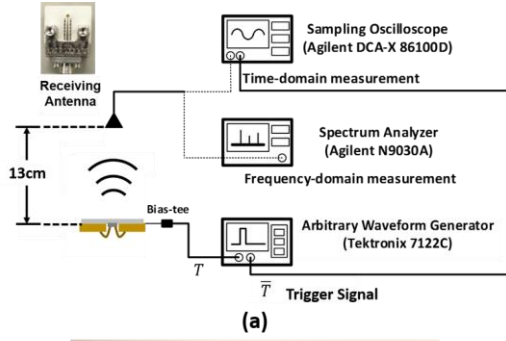


Fig. 11. Measurement setup for (a) time-domain and (b) frequency-domain characterization.

which is generated by the AWG (Tektronix 7122C). The trigger signal travels through a bias-tee (Picosecond Pulse Labs) before being fed into the impulse radiator. Tuning the bias-tee changes the FWHM pulse-width of the radiated impulses. In time-domain characterization, to capture radiated impulses without distortions, a custom broadband PCB impulse antenna was designed and used as a receiving antenna [16], [17].

Fig. 12(a) presents the measured impulse waveform with the minimum FWHM pulse-width of 60ps. It was achieved by tuning the oscillation frequency to 32GHz, sacrificing the gain of PA and the on-chip antenna. Its normalized power spectrum is demonstrated in Fig. 12(b). In contrast to the simulation results shown in Fig. 9, its center frequency is shifted to 32GHz and its 20dB bandwidth is increased to 20GHz. Fig. 12(c) shows that the generated impulses have a measured RMS jitter of 178fs when the measured RMS jitter of the input trigger signal is 150fs. An averaging of 64 is used in the measurement of timing jitter to reduce the noise from the sampling oscilloscope (Agilent DCA-X 86110D). The measured RMS jitter of the radiated impulses is limited by that of the input trigger signal. A more stable input trigger signal will result in a better measured RMS jitter.

The impulse radiator was designed to provide a center frequency of 30GHz. Fig. 13(a) shows the measured impulse waveform under the designed bias condition. It achieves a FWHM pulse-width of 74ps. Its EIRP frequency spectrum has been characterized using a standard gain horn antenna (A-Infomw LB-180400-KF, 18-40GHz, Gain=15dB) with a distance of 20cm. As shown in Fig. 13(b), the radiated 74ps impulse has an average EIRP of 0.5dBm at the center frequency of 30GHz with a 3dB bandwidth of 4.5GHz, a 10dB bandwidth of 10GHz, and a 20dB bandwidth of 18GHz. Because the radiated impulse train has a duty-cycle of nearly

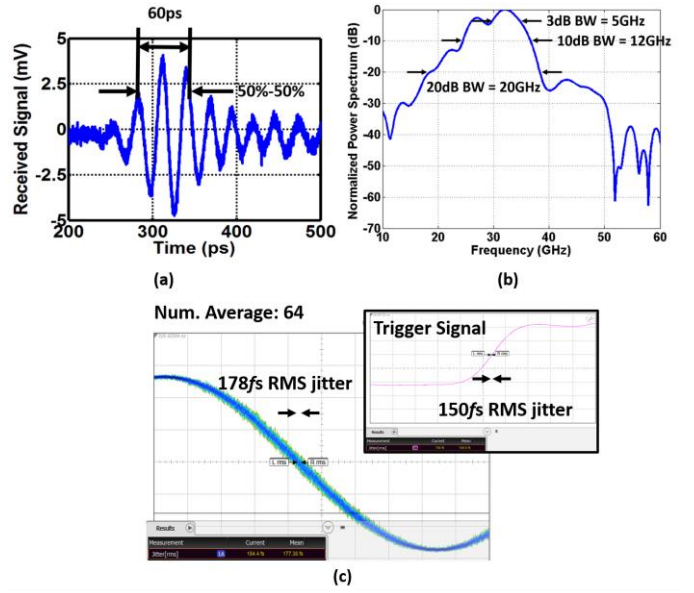


Fig. 12. Measurement setup for (a) time-domain and (b) frequency-domain characterization.

25%, the peak EIRP can be estimated to be 4 times larger (6dB larger) than the measured average EIRP, equaling to 6.5dBm.⁴ The differences between the measured EIRP (6.5dBm) and the simulated value (8.7dBm) arise from the effects of the packaging PCB, variations of the additional silicon slab thickness, and process variations. In addition to EIRP, antenna radiation patterns are measured at 20GHz, 30GHz and 40GHz, as shown in Fig. 13(c). The chip consumes an average DC power of 106mW.

IV. COHERENT IMPULSE COMBINING OVER THE AIR

In order to perform synthetic array 3D radar imaging, it is essential to achieve highly efficient coherent impulse combining over the air, which has been reported in [22] briefly. Details are provided here to analyze impulse combining accuracy and correlation factor between the individual radiated impulses for combining. These two factors are important, because the first factor interprets the combining error caused by timing jitter of impulses, and the latter factor represents the similarity between the impulse waveforms, which limits the maximum combined power due to destructive combining.

The measurement setup is shown in Fig. 14. Due to process variation and unbalanced signal travelling of the two input digital trigger signals (T_1 and T_2), timing shift between the generated impulse and the input trigger signal can be different between impulse radiators. To compensate this discrepancy in order to achieve highly efficient impulse spatial combining, two digital trigger output channels, T_1 and T_2 , are shifted with a resolution of 1ps. The receiving antenna is placed in the far field. In contrast to the work reported in [16] and [17], in this measurement, no millimeter-wave lens was used.

⁴ The definition of the peak EIRP in this paper is different from that in [22]. This definition is more accurate because it is based on the standard frequency-domain characterization method using a standard gain horn antenna.

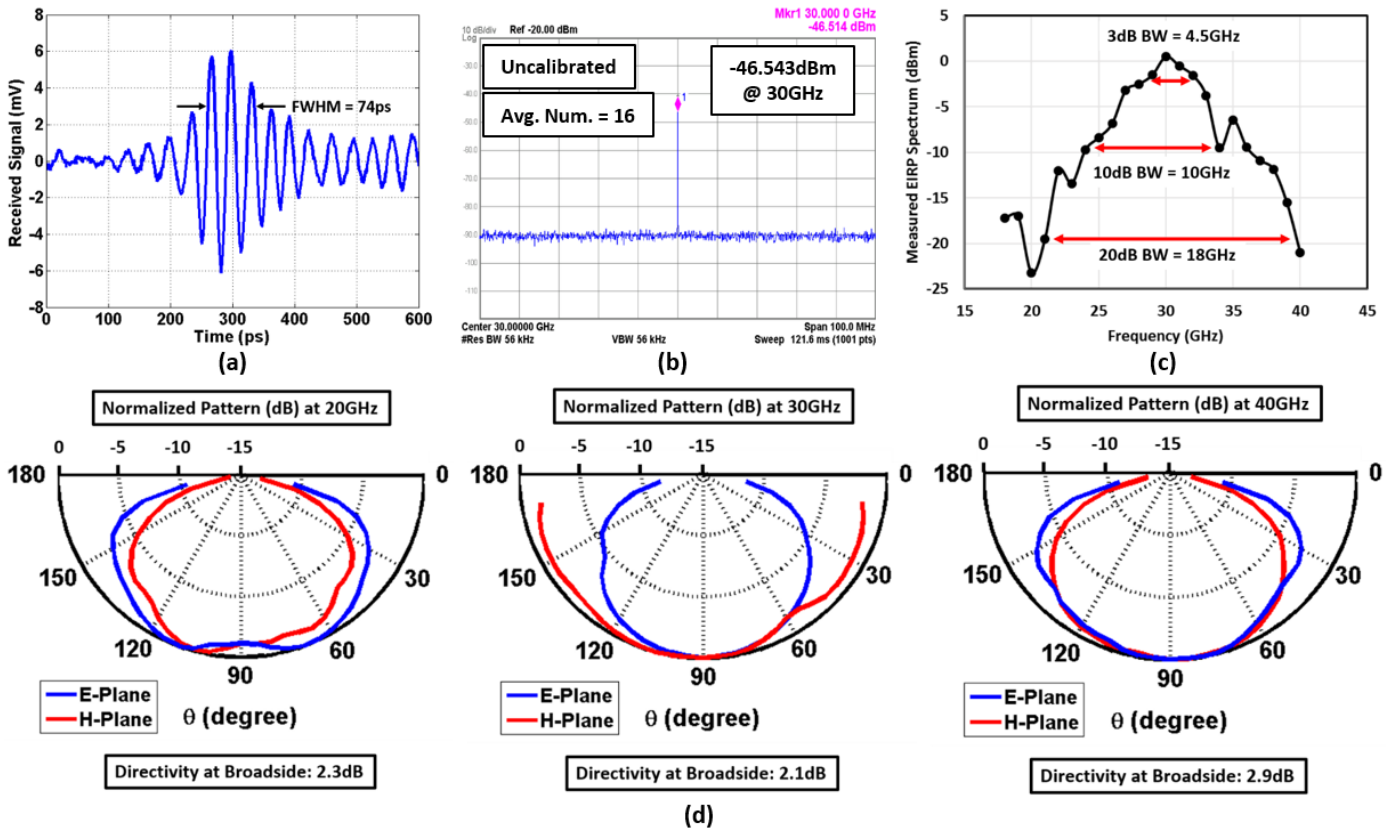


Fig. 13. (a) Measured 74ps radiated impulse using designed bias voltages. (b) Measured uncalibrated received power at 30GHz. (c) Measured EIRP spectrum. (d) Measured radiation patterns at 20GHz, 30GHz and 40GHz

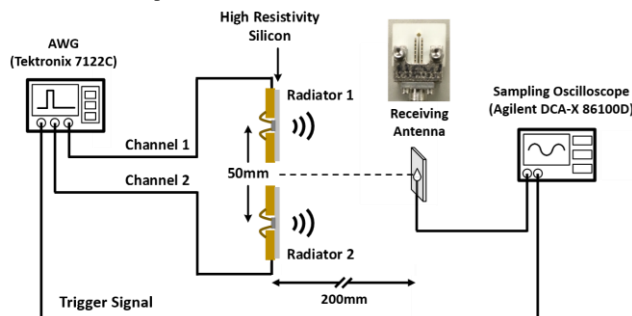


Fig. 14. Measurement setup of coherent impulse combining over the air.

Since the radiated impulse has an FWHM pulse-width of 60ps and the measured timing jitter is less than 0.2ps, the effects of timing jitter on impulse combining should be very small, resulting in an almost ideal impulse combining with negligible errors if all the discrepancies are compensated. As expected, Fig. 15(b) shows that the measured combined waveform is almost identical to the algebraic summation of the two separate impulse waveforms, meaning that the impulse combining accuracy is close to 1. Noise deteriorated the accuracy of impulse combining a little. Fig. 15(a) reports the measured impulses radiated from each chip. The correlation factor⁵ between them is 0.956, which shows a highly similarity between these two waveforms.

The measured RMS jitter of the combined waveform is

⁵ Correlation factor used in this work is defined and calculated as follows:

$$r = \int v_1(t) v_2(t) dt / \left[\sqrt{\int [v_1(t)]^2 dt} \sqrt{\int [v_2(t)]^2 dt} \right] = 0.956$$
, where $v_1(t)$ and $v_2(t)$ are the measured waveforms, respectively.

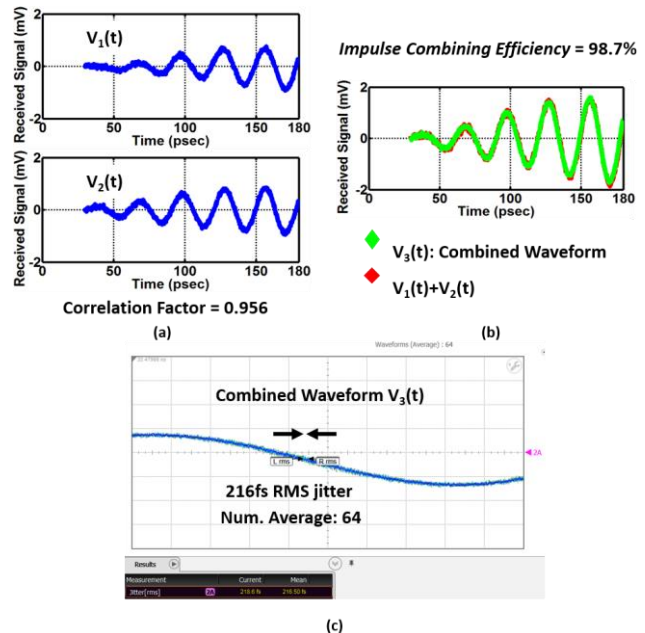


Fig. 15. Measurement setup of coherent impulse combining over the air.

216fs with an averaging of 64 (Fig. 15(c)). The increase in the measured RMS jitter compared with that of a single impulse radiator (178fs) is caused by the additional noise contributed by the second impulse radiator as well as the second input digital trigger signal.

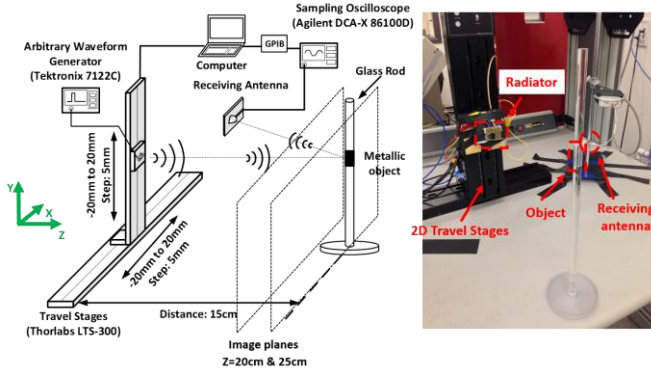


Fig. 16. Synthetic array imaging system for the 3D imaging of metallic objects.

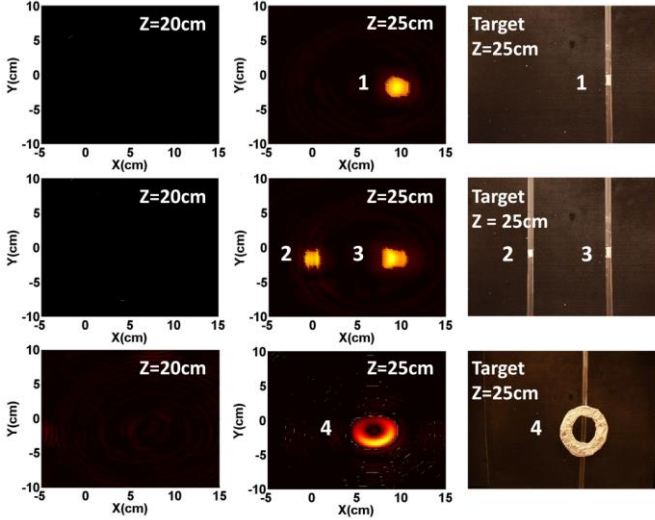


Fig. 17. 3D radar images of the metallic objects.

V. 3D RADAR IMAGING WITH A SYNTHETIC ARRAY

A custom synthetic impulse radiator array is built to produce high-resolution 3D images by adopting an impulse beamforming technique. As stated in the introduction, coherent impulse combining is the solution to the trade-off between higher image resolution and larger image range. In this work, a single radiator is utilized to construct a synthetic aperture radar [34] and DSP-based beamforming is applied to generate 3D images. Since the custom imaging systems built in this work have no RF amplification in the RX path, averaging is needed to reduce the noise from the sampling oscilloscope (Agilent DCA-X 86110D). The required time for acquiring data each time is about 1s. To increase image resolution, the impulse radiator is set to emit impulses with the minimum FWHM pulse-width of 60ps. The repetition rate is 300MHz.

A four-step methodology is proposed to perform 3D imaging by using a synthetic impulse radiator array ($N \times M$), built by moving one impulse radiator. After a complete array scan, based on time-of-flight calculation, DSP-based beamforming technique is applied to the received impulse waveforms in order to reconstruct 3D images. Enlarging the effective aperture size of the synthetic array enhances lateral image resolution. In addition, because beamforming technique has the essence of coherent impulse combining, SNR of

reconstructed 3D images can be improved by increasing the effective element number in the synthetic array.

A. 3D Radar Imaging of Metallic Objects

A custom 9×9 -element synthetic impulse radiator array is built to produce 3D images of metallic objects, as shown in Fig. 16. The impulse radiator is mounted on a 2D travelling stage (Thorlabs LTS-300). The 2D travelling stage moves the radiator to 9×9 locations to form a 9×9 -element synthetic array. The spacing between the elements in the synthetic array is 5mm, and therefore the effective aperture size of the synthetic array is $40\text{mm} \times 40\text{mm}$. A 3D coordinate system is built as follows: The top left element in the synthetic array is located at $(0, 0, 10\text{cm})$, and the synthetic array is on the XY plane. The Z coordinate of the metallic objects is 25cm, which means that the distance between the objects and the synthetic array is 15cm. The custom PCB-based broadband receiving antenna is placed at a fixed location in the 3D space. The entire imaging system is automated and controlled by a laptop with GPIB protocols.

In this work, image resolutions are defined as

$$\text{Depth Resolution} = \frac{\text{pulse_width} \times c}{2} \quad (4)$$

$$\text{Lateral Resolution} = \frac{\lambda \times D}{R} \quad (5)$$

where c is the speed of light in the medium, λ is the center wavelength of the impulse signal in the medium, D is the depth range, and R is the aperture size of the synthetic array.

Three scenarios are designed to produce 3D radar images of various metallic objects. As shown in Fig. 17, in the first scenario, the object is a small aluminum cylinder wrapped on a glass rod; in the second scenario, two spaced small aluminum cylinders are used as objects; in the third scenario, the object is an aluminum ring.

By adopting the proposed imaging methodology, 3D radar images of the three scenarios are generated with a depth resolution of 9mm and a lateral resolution of 2.65cm at a depth range of 15cm in the air (Fig. 17). When the image plane is on the XY plane with the Z-coordinate of 20cm, where there is no object, the generated 3D images are completely black in all three scenarios. These images show that the synthetic impulse radiator array detects no reflections from the image plane at $Z=20\text{cm}$. When the image plane is set as the XY plane at $Z=25\text{cm}$, which is the exact depth range of the objects, the generated 3D images in all three scenarios show clear reflections. Color scales are identical in both radar images at $Z=20\text{cm}$ and $Z=25\text{cm}$ for each scenario. In all three scenarios, the sizes of the reflections are close to those of real objects. Furthermore, in the third scenario, the reflection variations shown in the generated image at $Z=25\text{cm}$ also coincides with the surface roughness variations of the aluminum ring: The lower part of the aluminum ring is rougher than the upper part. Therefore, more EM waves are reflected by the lower part of the aluminum ring than the

TABLE I
Comparison with state-of-the-art microwave 3D imaging radiators

	This Work	[16]	[18]	[19]	[20]
Radiator Type	Pulsed	Pulsed	Stepped frequency	Pulsed	Pulsed
Minimum FWHM Pulse-Width	60ps^a	8ps	63ps	36ps	3.5ns
Peak EIRP	6.5dBm	13dBm ^b	N/A	N/A	N/A
RMS Jitter	178fs	270fs	680fs	1.2ps	N/A
Coherent Impulse Combining	Yes (Two Chips)	Yes	No	No	No
3D Imaging	Performed	Not Performed	Performed ^c	Not Performed	Performed ^c
Imaging Objects	Metallic objects & Oil-immersed rocks	N/A	Single metallic object & Breast phantom	N/A	Single metallic object
Depth Resolution ^d	9mm	1.2mm	9mm	5.4mm	0.1cm ^e
Lateral Resolution ^d	8mm@10cm	N/A	N/A	N/A	2.4cm@1m ^c
Total Area	2.85mm²	0.47mm ²	1.3mm ² ^f	6.16mm ²	7.56mm ² ^f
System Integration Level	TX+Antenna	TX+Antenna	TX+RX	TX+RX+Antenna	TX+RX
Power Consumption	106mW	220mW	204mW	580mW	960mW
Technology	130nm SiGe BiCMOS	130nm SiGe BiCMOS	65nm CMOS	130nm SiGe BiCMOS	65nm CMOS

^a The pulse-width is variable but the shortest measured value is 60ps.

^b It was calculated based on the peak voltage of the transient impulse waveform. The definition is different from this work.

^c 3D imaging were performed with external PCB TX/RX antennas and reflector dishes.

^d The values are compared when air is the medium.

^e Depth resolution is obtained by using a modulated time-of-flight algorithm.

^f No on-chip antennas are implemented.

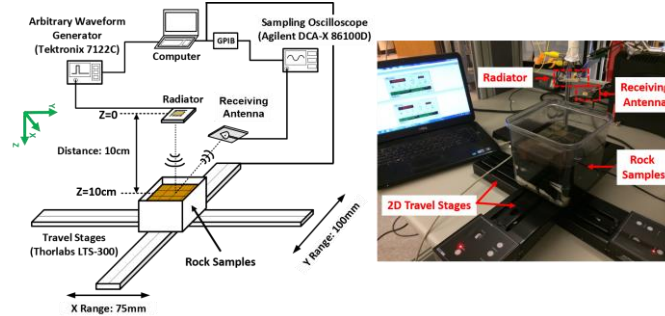


Fig. 18. Synthetic array imaging system for the 3D imaging of rock samples.

upper part, which is illustrated by the generated radar image.

B. 3D Radar Imaging of Rock Samples Immersed in Oil

The measurement setup of this test is demonstrated in Fig. 18. The proposed impulse radiator is fixed at the original point (0, 0, 0). A plastic box containing rock samples is placed on a 2D travelling stage (Thorlabs LTS-300), which is on an XY plane. The plastic box is moved in an XY plane relative to the impulse radiator in order to form a synthetic array with an effective aperture size of 75mm × 100mm. An element-to-element spacing of 1mm is chosen. The top surfaces of rock samples are placed on an XY plane with Z=100mm. The PCB receiving antenna is placed at a fixed position.

In this experiment, each rock cube has an approximate size of 25mm×25mm×25mm. These rock cubes have different reflection coefficients because of their various porosity and lithology. One of the limestone rock cubes is drilled and filled with distilled water. Another limestone rock cube, which

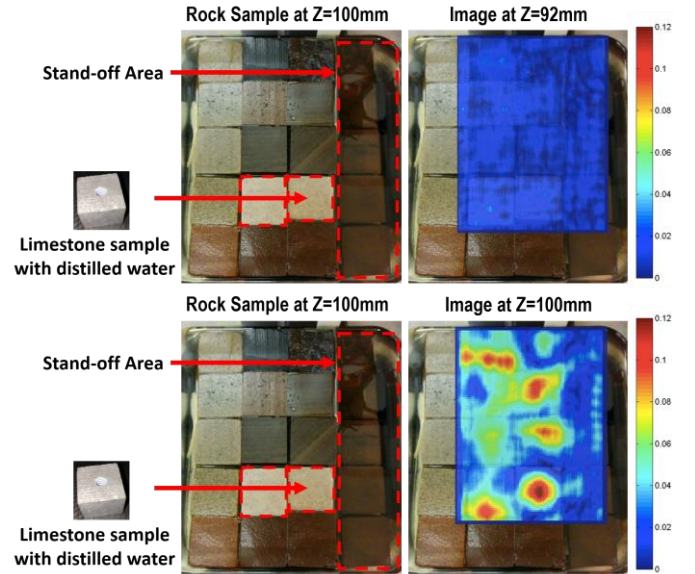


Fig. 19. 3D radar images of the rock samples.

contains no water, is placed next to it. The rock cubes and marble base are immersed in pure oil, whose relative permittivity is 2 (Fig. 19).

By applying the proposed imaging methodology, 3D radar images of rock samples are generated with a depth resolution of 6.4mm and a lateral resolution of 5.7mm at a range of 100mm in the oil, as shown in Fig. 19. In order to compare imaging results with real samples, the generated images are overlapped with the optical images of rock samples. When the

image plane is on the XY plane at $Z=92\text{mm}$, where no rock exists, intensities in the generated radar image are close to 0, because no objects are detected on this image plane. By shifting the image plane to the XY plane at $Z=100\text{mm}$, which is the top surfaces of the rock samples, the radar images of the rock samples reveal information about the rock types. The generated radar image at $Z=100\text{mm}$ shows significant reflection difference between the two limestone cubes. This is caused by high dielectric constant of the distilled water hidden in the right limestone cube. Furthermore, it is confirmed that there is little reflection shown across the stand-off area in the generated radar image at $Z=100\text{mm}$. This is because the stand-off surface is deeper than the image plane at $Z=100\text{mm}$.

VI. CONCLUSION

This paper reports an integrated 30GHz impulse radiator implemented in the IBM 130nm SiGe BiCMOS process technology. An asymmetric cross-coupled pulsed VCO topology is introduced to minimize the timing jitter of radiated impulses, which is crucial in achieving highly effective coherent spatial combining. With a 106mW average DC power consumption, the impulse radiator emits impulses with a minimum FWHM pulse-width of 60ps. The measured RMS jitter of the radiated impulses is 178fs when the input trigger signal has a 150fs RMS jitter. The chip achieves an average EIRP of 0.5dBm and a peak EIRP of 6.5dBm, when producing impulses with a FWHM of 74ps and center frequency of 30GHz. Coherent impulse combining over the air is performed by using two widely spaced impulse radiators. To the authors' knowledge, using a synthetic array based on a fully integrated impulse radiator in silicon, high resolution impulse-based 3D imaging is performed for the first time. 3D radar images of metallic objects and dielectric objects have been successfully demonstrated. In this work, a depth resolution of 9mm, a lateral resolution of 8mm at a range of 10cm in the air have been achieved. Table 1 shows the comparison of this work with the prior art.

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