A 6-to-18 GHz Tunable Concurrent Dual-Band Receiver Front End for Scalable Phased Arrays in 130nm CMOS

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***Abstract* — This paper presents a study and design of tunable concurrent dual-band receiver. Different system architectures and building blocks have been compared and analyzed. A tunable concurrent dual-band receiver front end has then been fabricated and characterized. It operates across a tri-tave 6-18GHz bandwidth with a nominal 17-25dB conversion gain, worst-case -15dBm IIP3, and worst-case -24.5dBm ICP1dB.**

***Index Terms* — Concurrent, dual-band, low-noise amplifier, receiver architecture, phased array.**

I. Introduction

The advancement of electronics demands more integration and flexibility, and radio frequency circuits are no exception. To meet such demands, multi-mode multi-band transceivers have been proposed to expand the capabilities of a single communication system. In addition, the concept of concurrent dual-band operation in radio frequency electronics has been introduced to improve the overall communication throughput [1]. However, the frequencies of the received RF signals in the architecture of [1] are fixed. This limits the application of this architecture to a subset of emerging standards.

This paper extends the previous work on concurrent dual-band receivers by introducing frequency tunability. As a proof of concept, a receiver element is designed for 6-18GHz scalable phased-array receiver [2]. The receiver is capable of receiving one signal within a low band (6-10.4GHz) and the other signal within a high band (10.4-18GHz) simultaneously. The center frequencies of these two signals can be selected independently with a 300MHz baseband bandwidth. In the final implementation, a GaN broad-band low-noise amplifier (LNA) will be placed in front of this receiver for pre-amplification.

Section II introduces the system architecture of this work, compares it with the ideas in [1], and explains why it is difficult for the architecture of the work in [1] to achieve the frequency tunability with a minor modification. Section III compares several topologies of tunable concurrent amplifiers, followed by the descriptions of the down-conversion mixer circuits and the baseband buffers. Experimental results of the proposed front-end will be presented in Section IV.

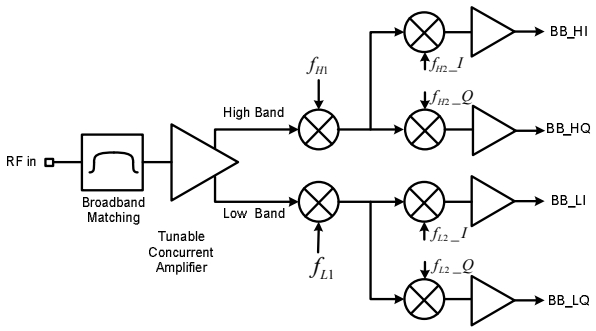

Fig. 1. Proposed system architecture of this work.

II. Tunable Concurrent Receiver Architecture

Fig. 1 shows the proposed receiver architecture of this work. A single-input, double-output tunable concurrent amplifier (TCA) amplifies the RF input signal and separates it into its low-band and high-band components. Both the high-band and the low-band have their own down-conversion signal paths. If the second LO frequency is chosen to be half of the first LO frequency, image signals will always fall out of the 6-18GHz frequency range; thus they can be filtered out easily by an off-chip filter. A total of six mixers are required to offer quadrature outputs for complex modulation scheme. Two frequency synthesizers are used for LO generation, whose implementation details can be found in [3].

Fig. 2 shows the concurrent receiver architecture and the concurrent dual-band LNA proposed in [1]. As opposed to this work, the receiver in Fig. 2 relies on the concurrent dual-band LNA for pre-amplification and for filtering image signals. By carefully designing the frequency plan and the polarity of Weaver's architecture, RF signals at $f_{LO1} - f_{LO2}$ and $f_{LO1} + f_{LO3}$ can be down-converted to two separate baseband outputs without image problems. The relationship among f_{LO1}, f_{LO2}, and f_{LO3} can be further designed, (e.g., $f_{LO2} = f_{LO3}/2$) to reduce the number of independent frequency synthesizers required.

The real challenge to make the receiver in Fig. 2 fully tunable lies in the dual-band LNA. The dual-band LNA has a dual-resonance input matching network, and a dual-resonance output network. For concurrent operations, resonant frequencies of these two networks need to be matched.

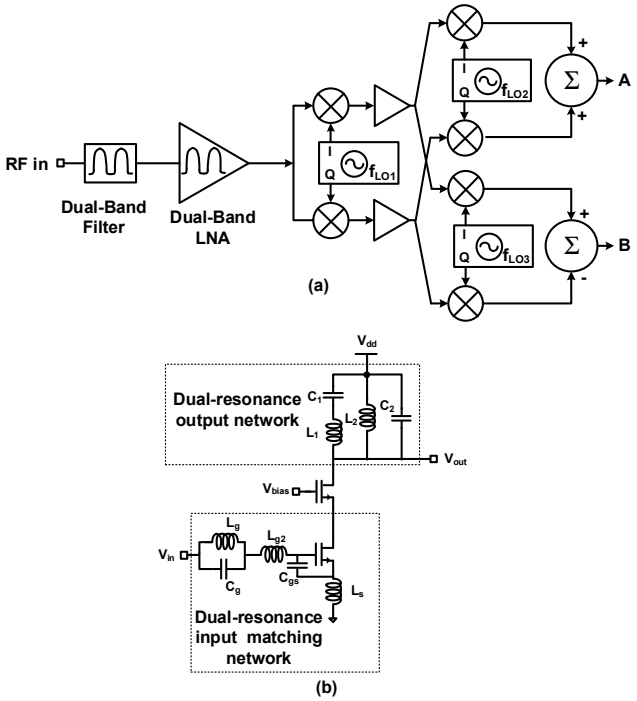

Fig. 2. (a) Concurrent dual-band receiver architecture (b) concurrent dual-band LNA proposed in [1]

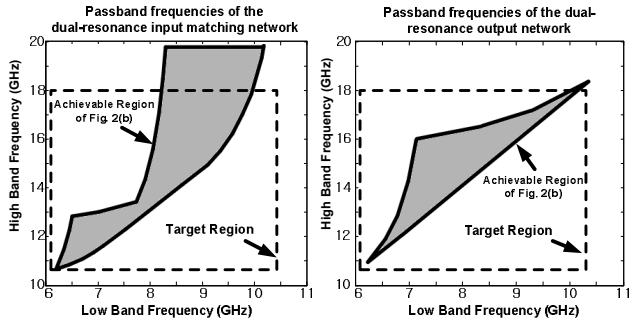

Fig. 3. Achievable frequency region of tunable dual-band operation of the LNA in Fig. 2 (b) with capacitor tuning range equals to three, and all frequencies between 6-18GHz covered by either band.

To make the dual-band LNA in Fig.2(b) tunable, variable capacitors (C_g, C_{gs}, C_1 and C_2) need to be implemented, which have a typical tuning range of three (e.g. MOS varactors). Under this constraint, a tunable dual-resonance input matching network and output network can be designed to cover any frequency between 6 and 18GHz by either of the pass-bands of the dual-resonance networks. The gray area enclosed by thick black lines in Fig.3 represents the achievable region of the concurrent dual-band operation. There are three major problems of this architecture: firstly, the high band and the low band frequencies can not be independently controlled, secondly, the achievable region of operation is only a small portion of the desired operation region, which is the rectangle enclosed by dotted lines, thirdly, matching the resonant frequencies of the two networks is difficult. Furthermore, it is not clear how and if it is possible to achieve this with a higher order networks due to resonant couplings in the system.

III. Circuit Blocks

A. Tunable Concurrent Amplifier (TCA)

The TCA needs to provide good broadband input matching and good isolation between its two outputs. Fig.4 illustrates several candidate topologies for the TCA. The inductive degeneration architecture [4] is not compared here due to its non-flat frequency response of the effective trans-conductance of its core amplifying device.

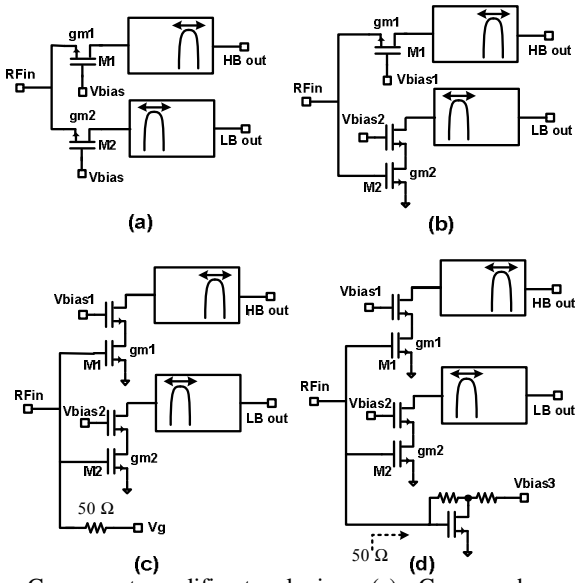

Fig. 4. Concurrent amplifier topologies. (a) Common base (CB)-CB (b) CB-Common Source(CS) (c) resistor termination (d) active termination.

The topology of Fig. 4 (a) consists of two common-base (CB) transistors. By sizing the two CB transistors carefully, good input matching and isolation between two resonant tanks can be simultaneously achieved. However, noise generated from M_1 will not be isolated from M_2, which results in poor noise performance. Fig. 4(b) replaces one of the CB transistors in Fig. 4(a) with a common source (CS) cascode topology. The benefits of doing so are that a larger g_{m1} can be used for input matching, which improves noise figure of the upper path; that the noise generated in M_2 is isolated from the upper path, and that possibly a larger g_{m2} can be used to

improve the noise figure of the lower path, at the cost of higher power consumption.

The topology in Fig. 4 (c) uses a simple 50Ω resistor for input matching. This way, the relationship between the transistor g_m and input matching can be decoupled; thus, a large g_m can be used for both paths to improve noise figure. However, the termination resistor contributes noise power, and the overall power consumption is higher than the circuit in Fig. 4(b). In this work, an active termination [5] replacing the 50Ω termination resistor is used to reduce the noise contribution, shown in Fig. 4(d). The detailed schematic of this TCA is shown in Fig. 5.

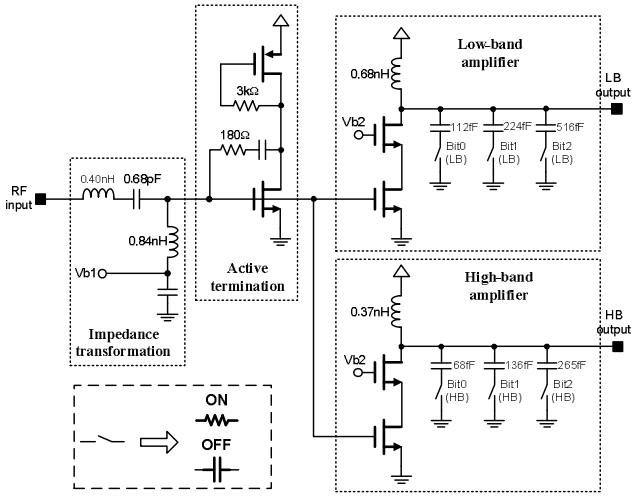

Fig. 5. Concurrent amplifier schematic.

B. Mixers

After the TCA, both high-band and low-band signals are down-converted to baseband by RF and IF mixers in cascade. Gilbert-type double-balanced mixers have been adopted to improve LO-IF feedthrough for all the mixers. A shunt-peaking inductor has been used in the low-band RF mixer to extend the IF port 3-dB bandwidth, while the high-band RF mixer uses a 3-bit switched LC-tuned load to compensate for the effect of the parasitic capacitances seen at its IF output. The resonant frequency of the switched tuned load needs to be adjusted to the correct IF frequency during operation. The common-mode feedback circuitry is also used to guarantee correct bias voltage for the following stage. Fig. 6 shows the schematics of both the high-band and the low-band RF mixers. The IF mixers are similar to the low-band RF mixers except that the differential CS transistors are degenerated for better linearity, and that the mixer loads are simple first-order RC filters.

C. Baseband Buffer Variable Gain Amplifiers(VGA)

The baseband buffer amplifiers utilize a differential CS topology with resistive source degeneration to improve their linearity performance. The open-drain output requires an external DC supply of 1.5V. The gain variation of 11dB in five steps is implemented by combining digitally-controlled current-commutating cells.

IV. Measurement Results

The implemented IC was mounted on a printed circuit board for mechanical stability during measurements. Dual-band RF inputs were applied through a coplanar waveguide probe, and baseband output pads are connected to SMA connectors through PCB traces and bond-wires. All measurement results are calibrated with, if not otherwise specified, the input reference plane at the TCA's GSG pads, and the output reference plane at the SMA connectors.

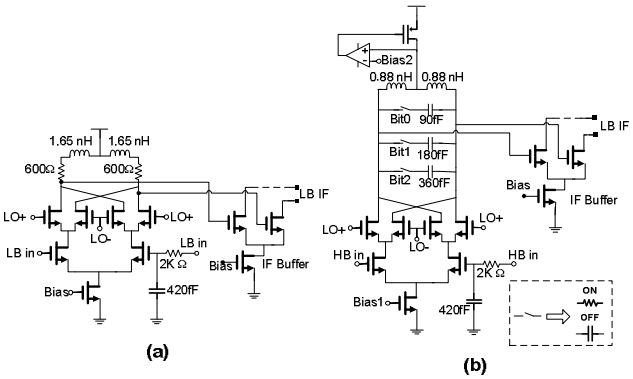

Fig. 6. Mixer schematics. (a) low-band RF mixer (b) high-band RF mixer.

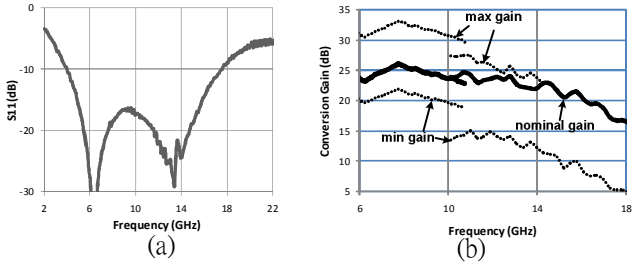

Fig. 7. (a) Input matching, (b) conversion gain.

Fig. 7(a) shows the measurement results of the receiver input matching. S_{11} is insensitive to supply voltage variations and the TCA tuned load bit settings.

Fig. 7(b) shows the nominal conversion gain (black thick line) and the variable gain range (the range between the upper and the lower dotted line.) Since both the TCA and the high-band RF mixer are tuned circuits, at a given set of RF inputs, each tuned load is set to be in-band,

meaning its resonant frequency is matched to the corresponding operating RF and IF frequencies. The conversion gain decreases with frequency in the high-band due to the large parasitic capacitance at the output of the RF mixers. However, this can be recovered by setting the VGA to higher gain. In addition, the isolation between high-band and low-band signal paths is better than 47dB.

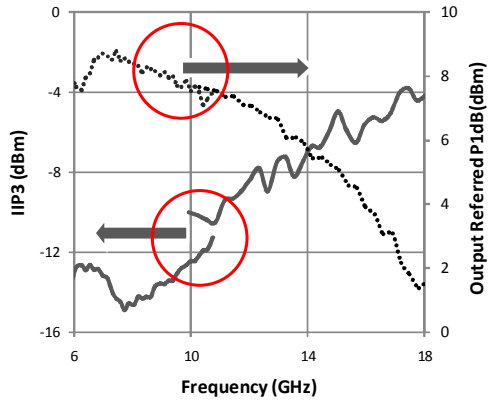

Fig. 8. In-band Input-referred IP3, and output-referred 1dB compression at maximum gain.

Third-order intercept point was measured by standard offset two-tone tests, and the measurement results are shown in Fig. 8. Improved IIP3 at higher frequency is due to the conversion gain drop. The output referred in-band 1dB compression point is also shown in Fig 8.

The solid line and the dashed line in Fig. 9 show the noise figure of the whole receiver with or without the GaN LNA, respectively. The noise figure increases at higher frequencies because the gain of the RF mixer drops due to its excessive parasitic capacitance at its IF port. The die photo of the reported front-end is shown in Fig. 10.

The receiver excluding baseband VGAs consumes 17 mA from a 1.2V power supply, and 81.2 mA from a 2.5V power supply. Each of the open-drain VGAs consumes 33.5 mA under nominal operation.

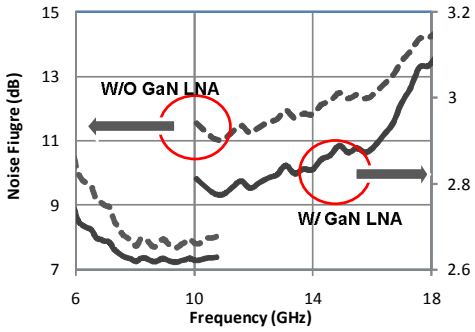

Fig. 9. Noise figure of the receiver system including GaN LNA.

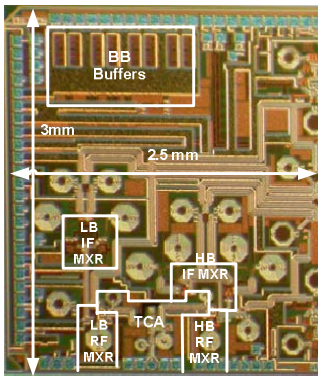

Fig. 10. Chip micrograph.

V. Conclusion

The first tunable concurrent dual-band receiver front end has been proposed and prototyped for the 6-18GHz phased-array receiver. Several design issues at the system and circuit level particular to such a system have been identified and remedied. The overall system performance is reported.

Acknowledgement

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