An Ultra-Wideband Impulse Receiver for sub-100fsec Time-Transfer and sub-30μm Localization

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***Abstract*— An ultra-wideband impulse receiver capable of detecting sub-200psec pulses is presented. The chip detects a specific zero-crossing of an incoming pulse and mitigates the undesired effects of ringing. The time detection sensitivity of the chip is limited by the jitter of the incoming pulse rather than the pulse width. A mean RMS jitter of 94fsec is recorded, which translates to the localization accuracy of sub-30μm. The chip is fabricated in IBM 130nm SiGe BiCMOS process technology.**

***Index Terms*— Wide-band receiver, impulse detector, direct RF-to-digital, synchronization, localization, time-transfer.**

I. Introduction

The ability to generate ultra-short pulses in silicon has drastically improved over the last decade. With the availability of advanced technology nodes, designers can now generate and radiate pulses as narrow as a few pico-seconds. The ability to produce such narrow pules has opened the door to inexpensive silicon-based 3D imaging radars, precision localization and time transfer, and high-speed communication [1]. On the receiving end, high-speed samplers are used to detect these pulses. These samplers are based on compound semiconductors, which makes them expensive. Even silicon-based high-speed samplers [2] need a lot of power and generate large amount of data, which need to be processed in real-time. This imposes strict design requirements on the processor and memory. In order to avoid the use of real-time samplers, fast energy detectors are currently used to detect the presence of short pulses.

Traditional pulse detectors use the energy envelope to detect the presence of pulses [3]. Such detectors use a diode-based topology and have major drawbacks. First, diode-based detectors detect the energy of the incoming signal irrespective of the shape/type of the pulse. Any signal with sufficient energy will trigger the system. This makes such detectors difficult to use in everyday scenarios where the environment is flooded with EM waves from wifi routers, cellphones, TV transmission towers, etc. This degrades the sensitivity of the receiver and makes it unreliable. Second, the timing accuracy of the energy detectors is limited by the pulse width and not the pulse jitter, which can be smaller than the pulse width by several orders of magnitude. Fig. 1 illustrates the difference between a conventional envelope detector and the proposed main zero-crossing detector.

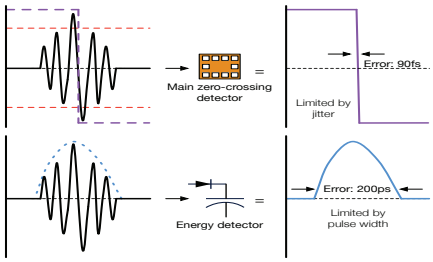


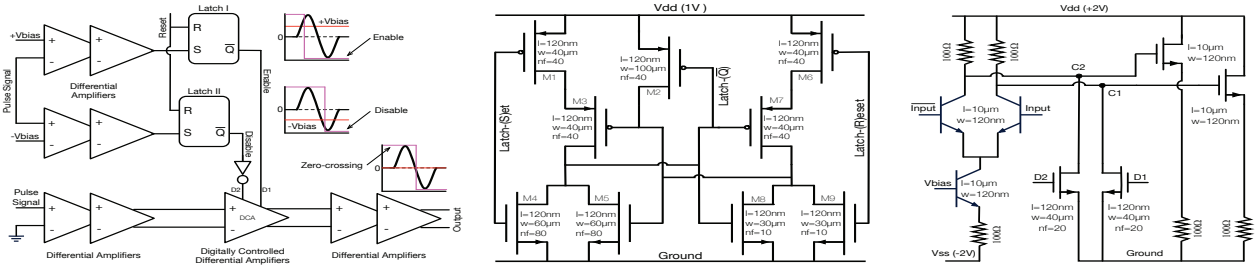
Fig. 1: Energy detector versus main zero-crossing detector

In this paper, we present a direct RF-to-Digital pulse detector architecture, which is only sensitive to the main zero-crossing of an incoming pulse. The chip detects a specific time-domain waveform and produces a trigger signal with timing error limited by the pulse jitter and not the pulse width. In this topology, the incoming signal should meet a predefined voltage, shape, and timing criteria to be detected. The proposed circuit rejects the undesired ringings, which otherwise would have contributed to the energy envelop. The small timing error makes the chip ideal for wireless time synchronization or distance estimation for imaging and localization.

II. Architecture

The reported pulse detector is designed to detect three specific events at high speed. First, it detects when the instantaneous pulse voltage crosses a positive threshold; second, it detects when the instantaneous pulse voltage crosses a negative threshold. The third and final event is to detect the zero-crossing when positive and negative amplitude criteria are satisfied by the first two voltage level detectors. These three rules are set to capture pulses, which meet the amplitude criteria and to minimize the error caused by the undesired ringing. Moreover, the voltage thresholds can be programmed dynamically depending on the signal strength. The timing criteria is implemented according to Fig. 2a and is discussed next.

The proposed architecture consists of three distinct signal paths. The first signal path (positive signal path) produces a trigger when the instantaneous voltage crosses a positive threshold. To detect is event, the input signal is passed through a differential amplifier whose one input is the threshold voltage and other is the signal itself.



(a) Core architecture (b) SR latch with feedback transistor (c) Digitally-Controlled Amplifier

Fig. 2: Architecture and schematics for core blocks in the main zero-crossing detector

As long as the input signal is smaller than the threshold voltage, one of the outputs of the differential amplifier is zero. When a pulse with the desired instantaneous positive voltage arrives, the output changes from 'zero' to 'one'. This output is fed to a SR latch, which locks when the differential amplifier's output changes from 'zero' to 'one'. When the latch locks, the output $\overline{Q}$ changes from state 'one' to state 'zero'. This transition marks an event in time when the positive amplitude of the pulse crosses a positive threshold. A similar signal path (negative signal path) is designed to register the event when the pulse crosses a negative threshold.

Finally, to detect the pulse's main zero-crossing, in a separate signal path (zero-crossing signal path), the input signal is passed through a differential amplifier, whose one input is grounded and the other input is the signal itself. Every time the signal crosses the zero reference, the differential amplifier toggles its output. To separate the undesired zero-crossings from the main zero-crossing, the output of the positive and negative signal paths are used, as shown in Fig. 2a. As shown in this figure, when the input signal becomes larger than the positive threshold, a Digitally-Controlled Amplifier (DCA) becomes active and produces a trigger when the input signal passes the zero reference. This amplifier remains active till the second latch in the negative signal path deactivates it. This happens when the input signal passes the negative threshold level. After the main zero-crossing is detected and a trigger signal is generated, an external reset signal is provided to reset the latches. After this step, the chip goes into the waiting mode and waits for another pulse to arrive.

III. Circuit Schematics

The main zero-crossing detector consists of three major circuit blocks; the latch, the digitally-controlled amplifier with enable/disable switches, and the wide-band differential amplifier. The circuit schematic of the latch is shown in Fig. 2b. This is an SR latch with a feedback path. In order to increase the speed of the latch, a feedback transistor (M2) is added. When the latch's (S)et port is changed to state 'one', transistor M1 switches off and transistor M4 switches on, but due to the presence of a charge on transistor M3 and slow switching speed of PMOS, the output '$\overline{Q}$' changes slowly. To mitigate this issue, the feedback transistor M2 is added, which provides an additional path for the charge stored on M3 to discharge. This effect reduces the fall-time of '$\overline{Q}$'

The circuit schematic of the digitally-controlled amplifier with enable/disable switches is shown in Fig. 2c. In this figure, when the chip is in the waiting mode, D2 is low and D1 is high. This guarantees that the voltage of the collector of the left bipolar transistor, node C2, remains higher than the voltage of the collector of the right bipolar transistor, node C1, irrespective of the differential input signal. When the input signal passes a predefined positive threshold level, Latch-I locks and D1 changes to low. In this phase, the DCA operates as a regular differential amplifier and reacts to the input signal. When the differential input signal changes from positive to negative and crosses the zero level, the output of the DCA toggles. At this time, the voltage at node C1 becomes higher than C2. To register this event and reject any further toggling, D2 is switched to high by Latch-II. This guarantees that node C1 remains higher than C2, irrespective of the input signal. By properly adjusting the values of the positive and negative threshold levels, the proposed circuitry becomes only sensitive to the main zero-crossing and the ringing effects are mitigated.

IV. Experimental Setup and Measurement Results

In the experimental setup, a two-channel arbitrary waveform generator was used to generate ultra-short sub-200ps pulses. These pulses were amplified before radiating from an impulse antenna. The transmitting antenna was mounted on a motorized travel stage and placed in front of a receiving antenna. The receiver antenna was also a broadband impulse antenna, whose signal was amplified with LNAs before being fed to the chip. A reset signal was also generated using a waveform generator, which was locked to the arbitrary waveform generator. The output of the chip was measured using a sampling oscilloscope. The oscilloscope was triggered

TABLE I COMPARISON TABLE WITH PRIOR ART

IC Specifications	This work	ISSCC 2015 [4]	ISSCC 2014 [5]	ISSCC 2011 [6]
Process	130nm BiCMOS	65nm CMOS	40nm CMOS	130nm BiCMOS
Die specifications	**0.42mm^2**	5mm^2	2.93mm^2	11.88mm^2
Power consumption	800mW	270mW	195mW	695mW
Signal Type	Impulse	Impulse	Multi-Tone	Impulse
Pulse Width (FWHM)	**80ps**	CF: 4GHz BW: 500MHz	CF: 60GHz BW: 2GHz	CF: 0.8-5GHz BW: 3GHz
Precision	**30μm**	1.9mm	4mm	7.3mm
Jitter	**<100fs**	Not reported	Not reported	<20ps (simulation)
TOA calculation	**Zero-crossing**	Correlation	Phase-shift	Direct-sampling with integration
Repetition Rate	5MHz	<1.25MHz	500KHz	10MHz

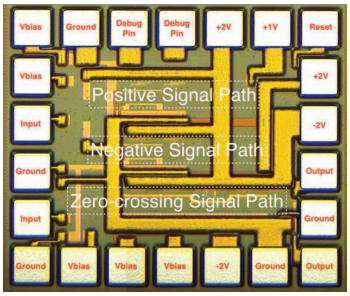


Fig. 3: Impulse receiver

with the clock generated by the second channel of the arbitrary waveform generator. Both channels of the arbitrary waveform generator are internally locked. This configuration was used to reduce the jitter between the trigger signal provided to the oscilloscope and the input signal sent to the chip. Fig.4 shows the block diagram of the measurement setup.

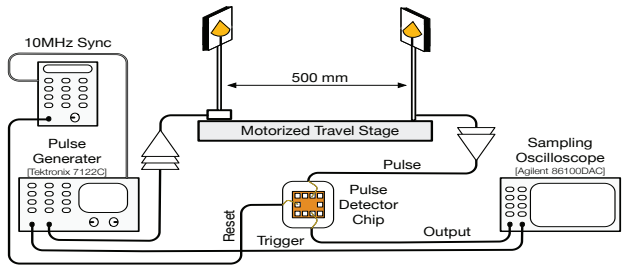
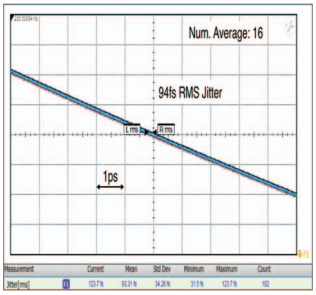


Fig. 4: Experimental setup for pulse detector chip

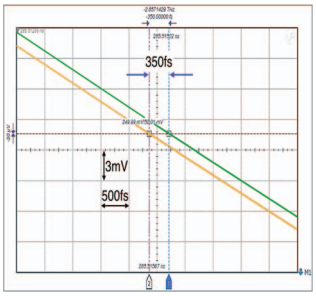
The timing accuracy in the measurement was limited by the jitter of the combined chip, arbitrary waveform generator, and the sampling oscilloscope. To measure the jitter, the input signal was repeatedly sent over the air and the sampling oscilloscope measured the mean RMS jitter over 100 cycles. The sampled signal was averaged 16 times to reduce the noise of the Agilent sampling head. Based on this measurement, a mean RMS jitter of 94fsec was measured, as shown in Fig. 5a.

The low jitter of the system allows for very fine and precise distance measurements, which can be used for localization or imaging. In this measurement, the transmitting antenna was placed on a motorized travel stage and moved 100μm in the direction of the receiver antenna. The reduction in the travel distance by 100μm made the pulse detection signal arrive 350fsec earlier than before, as seen in Fig. 5b. The earlier arrival of the pulse should ideally shift the detection signal by 336fsec. The 14fsec error in the shift is due to the combined jitter of the chip and the measurement setup.

The chip works with input signal amplitudes ranging from 1mVp-p to 1.5Vp-p. It was designed and fabricated in IBM's 130nm BiCMOS SiGe technology node and



(a) Jitter measurement results



(b) Zero-crossing detection

Fig. 5: Measurement Results

measures 700μm×600μm including bondpads. The results of this chip is compared with the prior art in table 1. Finally, the chip micrograph is shown in Fig. 3.

V. CONCLUSIONS

In this paper, a pulse detection chip is presented which is sensitive to the main zero-crossing of the incoming pulse. It is shown that the main zero-crossing can be detected with sub-100fsec jitter and the effects of the undesired ringings can be eliminated. In contrast with traditional energy detectors that have a timing accuracy on the order of the pulse width, in the proposed architecture, the timing accuracy is limited by the jitter of the pulse. It is shown that 200psec pulses can be utilized to provide a time transfer accuracy of sub-100fsec, which translates to the localization accuracy of sub-30μm.

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