Solving Large-Scale Hybrid Circuit-Antenna Problems

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***Abstract*—Motivated by different applications in circuits, electromagnetics, and optics, this paper is concerned with the synthesis of a particular type of linear circuit, where the circuit is associated with a control unit. The objective is to design a controller for this control unit such that certain specifications on the parameters of the circuit are satisfied. It is shown that designing a control unit in the form of a switching network is an NP-complete problem that can be formulated as a rank-minimization problem. It is then proven that the underlying design problem can be cast as a semidefinite optimization if a passive network is designed instead of a switching network. Since the implementation of a passive network may need too many components, the design of a decoupled (sparse) passive network is subsequently studied. This paper introduces a tradeoff between design simplicity and implementation complexity for an important class of linear circuits. The superiority of the developed techniques is demonstrated by different simulations. In particular, for the first time in the literature, a wavelength-size passive antenna is designed, which has an excellent beamforming capability and which can concurrently make a null in at least eight directions.**

***Index Terms*—Antenna radiation pattern, circuit network analysis, circuit optimization, convex optimization, integrated antennas, linear matrix inequalities, reconfigurable antenna.**

I. Introduction

MANY important problems in circuits, electromagnetics (EMs), and optics can be reduced to the analysis and synthesis of some linear systems in the frequency domain. These systems, in the circuit theory, consist of passive elements including resistors, inductors, capacitors, ideal transformers, and ideal gyrators [1]. Since the seminal work [2], there has been a remarkable progress in characterizing such passive (dissipative) systems using the concept of positive real functions. This notion plays a vital role not only in circuit design but also in various control problems [1], [3], [4].

The application of control theory in circuit and communication areas evidently goes beyond the passivity concept. Indeed, the emerging optimization tools developed by control theorists, such as linear matrix inequalities (LMIs) [5] and sum of squares (SOS) [6], have been successfully applied to a number of fundamental problems in these fields. The study in [7] is one of the earliest works connecting the convex optimization theory to circuit design, whose objective is to optimize the dominant time constant of a linear resistor–capacitor circuit using semidefinite programming. The recent paper [8] proposes an LMI optimization to check whether a given multiport network can be realized using a prespecified set of linear time-invariant components (namely, an inductor and a small-signal model of a transistor). Moreover, the study in [9] formulates the pattern synthesis of large arrays with bound constraints on the sidelobe and mainlobe levels as a semidefinite programming problem.

Different problems in circuits, EMs, and optics may be formulated as an optimization over the parameters of a multiport passive network that is obtained, for instance, via an EM simulation. As an example, it is shown in [10] that a strikingly efficient and practical way to deal with certain complex antenna problems is to extract a circuit model and then to search for the appropriate values of its parameters. The circuit model proposed in [10] is indeed a simple and general model that could be considered as the abstract model of different types of problems. A question arises as to whether there exists a systematic method to study such circuit problems by means of efficient algorithms. This paper basically aims to address this question using the available techniques developed in the control theory, especially the LMI and passivity concepts.

Motivated by the studies in [10] and [11] on the design of on-chip antennas, a linear multiport network is considered in this paper, where certain design specifications on its input admittance and output voltages must be satisfied at a desired frequency. To achieve this, some of the output ports of the network, referred to as *controllable ports*, are connected to a control unit. It is shown that designing a control unit in the form of a switching network that makes the circuit meet the design specifications is an NP-complete problem. Instead, the design of a passive network for the control unit can be cast as a semidefinite optimization. Since a passive network may require many components (elements) for its implementation, the design of a sparse (decoupled) passive controller is also studied. To this end, a rank-minimization problem is obtained, which can be handled using the convex-based heuristic method proposed in [12] (and further studied in [13]). This heuristic method is able to correctly solve the rank-minimization problem in some cases. Note that the main assumption required in this paper is the linearity of the given network at the desired frequency, and hence, the developed technique is not applicable to nonlinear circuits that cannot be satisfactorily linearized at the frequency of interest.

The techniques developed here are applied to two antenna design problems to demonstrate how the optimal antenna configurations with a superior performance can be engineered. In par-

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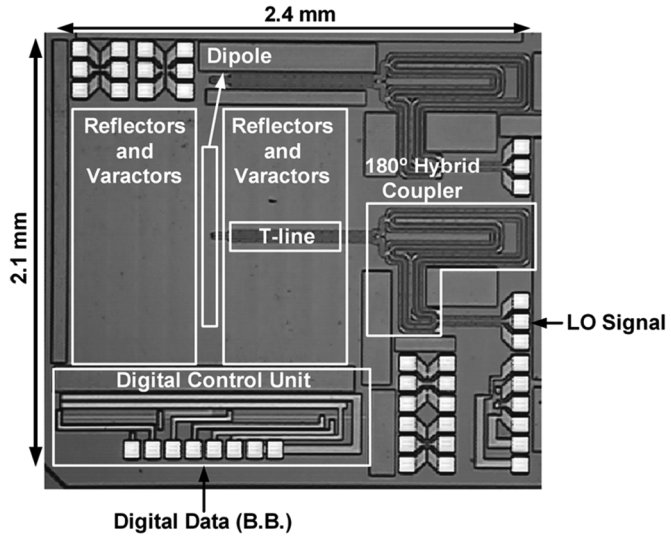

Fig. 1. This is an implementation of an important antenna configuration whose optimal synthesis can be cast as the problem studied in the present paper (see [10] for more details on this chip micrograph).

ticular, an on-chip wavelength-size passive antenna is designed, which can steer the beam to an arbitrary direction and can simultaneously make a null in at least eight directions. This is the first antenna system reported in the literature with such properties, which has a significant beamforming capability. Note that the type of antenna designed here is practically implementable. In particular, we have already implemented a nonoptimal antenna with the same structure as in [10], leading to the chip micrograph shown in Fig. 1.

The rest of this paper is organized as follows. The problem is formulated in Section II, and some practical motivations and related works are then outlined. The main results are developed in Section III. The efficacy of this paper is demonstrated in Section IV through different simulations. Some concluding remarks are drawn in Section V. A proof is finally provided in the Appendix.

II. Problem Formulation and Motivation

Given a natural number n, consider a linear passive $(n+1)$-port (reciprocal) network, where ports $1, 2, \ldots, n$ play the role of the outputs of the network and port $n+1$ is the input of the network that is connected to a voltage source with a fixed voltage v_{in}. The output ports of this network are divided into two groups, for a number $z \in \{1, 2, \ldots, n-1\}$, as follows.

1) *Output ports* $1, 2, \ldots, z$: These ports are the output ports of interest, i.e., the ones whose voltages must satisfy some design specifications (linear constraints).
2) *Output ports* $z+1, z+2, \ldots, n$: These ports are the *controllable* output ports, i.e., the ones that are connected to a control unit and the ones that must be controlled in such a way that the output voltages at ports $1, 2, \ldots, z$ as well as the input admittance of the network at port $n+1$ satisfy certain linear specifications.

Since the output ports $1, 2, \ldots, z$ will not be connected to any device/controller and since they are used to only measure their voltages, the current through each of these ports must be zero.

The circuit corresponding to the aforementioned configuration is shown in Fig. 2, which will be referred to as *Circuit 1* throughout this paper. As shown in the figure, let v_p and i_p denote the voltage and current of port p, respectively, for every

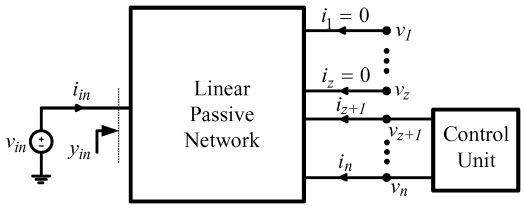

Fig. 2. Circuit 1 studied in this paper.

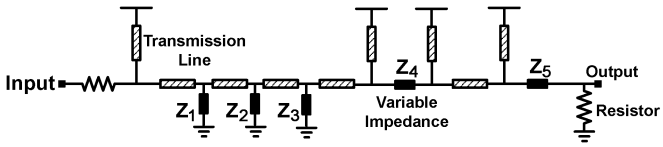

Fig. 3. Distributed circuit with variable impedances.

$p \in \{1, 2, \ldots, n\}$. Moreover, let i_{in} be the current at port $n+1$, and let y_{in} be the input admittance of the linear network. To be more specific about the objective of the present work, consider a desired frequency ω_0. The goal is to design a controller for the control unit so that the parameters of Circuit 1 at frequency ω_0 satisfy the design specifications

$$\left|\text{Re}\left\{v_j - v_j^d\right\}\right| \leq \varepsilon_j, \qquad \forall j \in \{1, 2, \ldots, z\} \tag{1a}$$

$$\left|\text{Im}\left\{v_j - v_j^d\right\}\right| \leq \bar{\varepsilon}_j, \qquad \forall j \in \{1, 2, \ldots, z\} \tag{1b}$$

$$\left|\text{Re}\left\{y_{\text{in}} - y_{\text{in}}^d\right\}\right| \leq \varepsilon \tag{1c}$$

$$\left|\text{Im}\left\{y_{\text{in}} - y_{\text{in}}^d\right\}\right| \leq \bar{\varepsilon} \tag{1d}$$

$$i_j = 0, \qquad \forall j \in \{1, 2, \ldots, z\} \tag{1e}$$

where the operators $\text{Re}\{\cdot\}$ and $\text{Im}\{\cdot\}$ return the real and imaginary parts of a complex number and

1) $v_1^d, \ldots, v_z^d$ are the given desired voltages for output ports $1, \ldots, z$, respectively;
2) y_{in}^d is the desired input admittance;
3) $\varepsilon_j, \bar{\varepsilon}_j$ $(\forall j = 1, 2, \ldots, z)$, ε, and $\bar{\varepsilon}$ are arbitrary nonnegative numbers.

The primary objective of this paper is to study the design of different types of control units, such as switching, passive, and decoupled passive controllers, for Circuit 1 and then to investigate the tradeoff between design simplicity and implementation complexity for each of these types.

Note that the circuit that is being studied here is assumed to be passive and is connected to only one voltage source. However, the results of this paper can be generalized to the case when there are more than one voltage (current) source, and besides, certain active elements exist in the circuit.

A. Simple Illustrative Example

Although the main motivation of the present work is the synthesis of circuits derived from EM structures, it is helpful to illustrate how some generic circuit problems may be modeled as Circuit 1. To this end, consider the simple filter shown in Fig. 3. Assume that the goal is to find the numerical values of the impedances Z_1 to Z_5 in such a way that the input–output gain of the filter is maximized at a prespecified frequency ω_0. To this end, one can reorganize the elements of this filter to obtain the equivalent model shown in Fig. 4, where the known elements are clustered in the block "linear passive network" and the unknown components are grouped in the block "control unit." Under this setting, the objective reduces to designing the control unit in

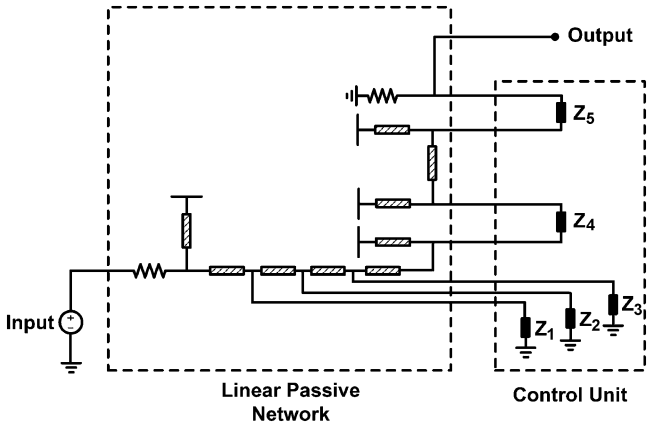

Fig. 4. Filter shown in Fig. 3 is redrawn in the form of Circuit 1.

Fig. 4 so that the magnitude of the observed output of the circuit is maximized. The following three points can be made here.

1) The control unit in Fig. 4 is highly structured in the sense that its seven terminal ports are connected to each other in a particular way by the elements Z_1 to Z_5. How to design a control unit with a prescribed structure will be explained later in Section III-F.
2) The linear passive network in Fig. 4 has some distributed elements, namely, transmission lines. However, they can be replaced by their lumped models at frequency ω_0.
3) As a generalization to the feasibility problem defined earlier by (1), one can also maximize some quantity of interest in addition to imposing the constraints given in (1). For example, the magnitude of the observed output of the circuit can be maximized (this is explained in Section III-F).

B. Motivation

Numerical methods and efficient optimization techniques, enabled by increasing the computational power, have been markedly instrumental in advancing the field of modern electrodynamics. The progress in this field, which was limited to the development of analytical models for antenna characteristics such as pattern, efficiency, and impedance, has been greatly influenced by novel numerical techniques in time or frequency domains. Frequency-domain techniques such as the finite element method [15] and the method of moments [16], as well as the time-domain algorithms such as the finite difference technique [17], have been extensively used in designing the EM structures. These numerical methods, combined with optimization techniques such as genetic algorithm [18] and particle swarm optimization (PSO) [19], provide a valuable, but inefficient, tool in designing large-scale EM structures where thousands of passive elements are involved. Indeed, the available numerical techniques iteratively search for a suboptimal solution. Since a new time-consuming EM simulation needs to be run at each iteration, this approach could be really prohibitive due to the exponential number of iterations.

In the recent paper [10], this crucial issue is partially resolved by introducing a novel method, which requires performing the EM simulation only once to extract the equivalent circuit model of the system at a single frequency of interest. The EM problem then reduces to solving a noniterative optimization problem over the parameters of this circuit model. It is noteworthy that this circuit model is in the form of Circuit 1, in which ports $1, 2, \ldots, z$ correspond to the receiving antennas at the far field and ports $z+1, \ldots, n$ correspond to the controllable ports on the transmitting antenna. Now, ports $z+1, \ldots, n$ on the transmitting antenna should be controlled in such a way that the desired voltages are received in the far field of the receiving antennas $1, 2, \ldots, z$. Roughly speaking, many problems governed by Maxwell's differential equations seeking optimal values of the termination impedances/voltages can be converted to the circuit problem introduced earlier.

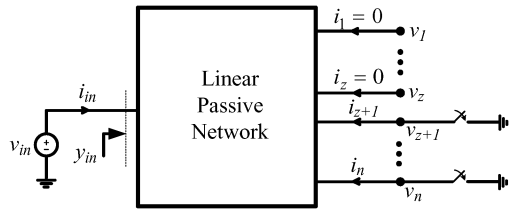

Fig. 5. Circuit 2 obtained from Circuit 1 by using a switching control unit.

C. Related Work

The study in [7] studies a linear resistor–capacitor (RC) circuit described by the differential equation

$$C\frac{d\mathbf{v}(t)}{dt} = -G\left(\mathbf{v}(t) - \mathbf{u}(t)\right) \tag{2}$$

where $C \in \mathbf{R}^{n\times n}$ and $G \in \mathbf{R}^{n\times n}$ are the symmetric positive-definite capacitance and conductance matrices to be designed, $\mathbf{v}(t) \in \mathbf{R}^n$ is a vector of the node voltages, and $\mathbf{u}(t) \in \mathbf{R}^n$ is a vector of the independent voltage sources. Let $\mathbf{x} := [x_1 \quad x_2 \quad \cdots \quad x_n]$ be a vector of unknown design parameters, and assume that matrices C and G that are being sought are required to depend affinely on $\mathbf{x}$, i.e.,

$$C = C_0 + C_1x_2 + \cdots + C_nx_n$$
$$G = G_0 + G_1x_2 + \cdots + G_nx_n$$

where $C_0, \ldots, C_n$ and $G_0, \ldots, G_n$ are some given matrices. It is shown in [7] that the problem of finding the parameter vector $\mathbf{x}$ in such a way that the dominant time constant of the circuit (2) is optimized can be cast as a semidefinite programming problem. The present work deals with another type of circuit problem, which is more complicated than the one tackled in [7]. The reason is that the control unit that is to be designed for Circuit 1 may not be characterizable as an affine function of the design parameters $v_1, v_2, \ldots, v_z$ and y_{in}. However, it will be shown in this paper that the underlying problem can also be cast as a semidefinite programming problem.

III. Main Results

Different types of control units will be designed for Circuit 1 in the following sections.

A. Switching Control Unit

Motivated by the antenna application [10] discussed earlier, the most desirable (and simplest) type of control unit is likely a switching controller, which connects every port $p \in \{z+1, \ldots, n\}$ to an ideal switch that is either on or off (the switch connected to port p is called *switchp*). This is shown in Fig. 5, and the corresponding circuit is referred to as *Circuit 2*. The problem that is being addressed here is formalized next.

Problem 1: Find whether it is possible to turn on a subset of switches $z+1, z+2, \ldots, n$ in Circuit 2 so that the design specifications given in (1) are all satisfied.

To analyze Circuit 2, introduce the shorthand notations

$$\mathbf{i} = [\, i_1 \quad i_2 \quad \cdots \quad i_n \,]$$
$$\mathbf{v} = [\, v_1 \quad v_2 \quad \cdots \quad v_n \,].$$

One can write a number of equations as

$$[\mathbf{i} \quad i_{\text{in}}] = [\mathbf{v} \quad v_{\text{in}}] Y_s \tag{3a}$$
$$i_{\text{in}} = y_{\text{in}} v_{\text{in}} \tag{3b}$$
$$i_j = 0, \qquad \forall\, j \in \{1, 2, \ldots, z\} \tag{3c}$$

where Y_s denotes the admittance transfer function of the linear passive $(n+1)$-port network (the middle block in the circuit) at a given frequency ω_0 or, equivalently, the Y-parameter matrix of the network at frequency ω_0. Note that Y_s is a complex-valued matrix whose real and imaginary parts are both symmetric.

Denote the set of complex numbers with $\mathbf{C}$. Define $\{\mathbf{e}_1, \mathbf{e}_2, \ldots, \mathbf{e}_n\}$ and $\{\tilde{\mathbf{e}}_1, \tilde{\mathbf{e}}_2, \ldots, \tilde{\mathbf{e}}_{n+1}\}$ to be the sets of standard basis vectors of $\mathbf{R}^n$ and $\mathbf{R}^{n+1}$, respectively. Throughout this paper, the notation $\succ$ is used to show the matrix inequalities in the positive definite sense. The symbol "*" is also used to denote the conjugate transpose of a matrix. The following theorem recasts Problem 1 as an optimization problem.

Theorem 1: Minimize the rank of the matrix

$$\begin{bmatrix} X & \begin{bmatrix} \mathbf{u}^* \\ v_{\text{in}} \end{bmatrix} \\ [\mathbf{u} \quad v_{\text{in}}] & 1 \end{bmatrix} \tag{4}$$

for the variables $X \in \mathbf{C}^{(n+1)\times(n+1)}$ and $\mathbf{u} \in \mathbf{C}^{1\times n}$ that are subject to the constraints

$$\left|\text{Re}\left\{\mathbf{u}\mathbf{e}_j - v_j^d\right\}\right| \le \varepsilon_j, \qquad \forall\, j \in \{1, 2, \ldots, z\} \tag{5a}$$
$$\left|\text{Im}\left\{\mathbf{u}\mathbf{e}_j - v_j^d\right\}\right| \le \bar{\varepsilon}_j, \qquad \forall\, j \in \{1, 2, \ldots, z\} \tag{5b}$$
$$\left|\text{Re}\left\{\begin{bmatrix} v_{\text{in}}^{-1}\mathbf{u} & 1 \end{bmatrix} Y_s \tilde{\mathbf{e}}_{n+1} - y_{\text{in}}^d\right\}\right| \le \varepsilon \tag{5c}$$
$$\left|\text{Im}\left\{\begin{bmatrix} v_{\text{in}}^{-1}\mathbf{u} & 1 \end{bmatrix} Y_s \tilde{\mathbf{e}}_{n+1} - y_{\text{in}}^d\right\}\right| \le \bar{\varepsilon} \tag{5d}$$
$$[\mathbf{u} \quad v_{\text{in}}] Y_s \tilde{\mathbf{e}}_j = 0, \qquad \forall\, j \in \{1, 2, \ldots, z\} \tag{5e}$$
$$\mathbf{x}_j Y_s \tilde{\mathbf{e}}_j = 0, \qquad \forall\, j \in \{z+1, \ldots, n\} \tag{5f}$$
$$X = X^* \tag{5g}$$

where $\mathbf{x}_j$ denotes the jth row of matrix X. Problem 1 is feasible if and only if the value of the minimum rank is equal to one, in which case a feasible solution can be extracted as follows: for every $j \in \{z+1, \ldots, n\}$, turn on switch j if and only if the jth entry of $\mathbf{u}$ is zero.

Proof of Necessity: Assume that Problem 1 has a feasible solution. Let k denote the number of switches whose connection makes the design specifications given in (1) be satisfied. Denote the set of such switches with $\{p_1, p_2, \ldots, p_k\} \subseteq \{z+1, \ldots, n\}$. The goal is to construct a matrix $X \in \mathbf{C}^{(n+1)\times(n+1)}$ and a vector $\mathbf{u} \in \mathbf{C}^{1\times n}$ for which the rank of matrix (4) is one, and in addition, the constraints in (5) are all satisfied. To this end, consider Circuit 2, with switches $p_1, p_2, \ldots, p_k$ turned on (and the remaining switches turned off). One can write

$$v_j = 0, \qquad \forall\, j \in \{p_1, p_2, \ldots, p_k\}$$
$$i_j = 0, \qquad \forall\, j \in \{z+1, z+2, \ldots, n\} \setminus \{p_1, p_2, \ldots, p_k\}.$$

This implies that

$$v_j^* i_j = 0, \qquad \forall\, j \in \{z+1, z+2, \ldots, n\}. \tag{6}$$

On the other hand, it follows from (3a) that

$$i_j = [\mathbf{v} \quad v_{\text{in}}] Y_s \tilde{\mathbf{e}}_j, \qquad \forall\, j \in \{1, 2, \ldots, n\}. \tag{7}$$

Equation (7) can be substituted into (6) to obtain

$$v_j^* [\mathbf{v} \quad v_{\text{in}}] Y_s \tilde{\mathbf{e}}_j = 0, \qquad \forall\, j \in \{z+1, z+2, \ldots, n\}. \tag{8}$$

Define

$$\mathbf{u} := \mathbf{v} \quad X := \begin{bmatrix} \mathbf{v}^* \\ v_{\text{in}} \end{bmatrix} [\mathbf{v} \quad v_{\text{in}}]. \tag{9}$$

The constraints given in (5) are all satisfied for this particular choice of X and $\mathbf{u}$ because of the following observations.

1) In light of the relations

$$v_j = \mathbf{v}\mathbf{e}_j, \qquad \forall\, j \in \{1, 2, \ldots, z\}$$
$$y_{\text{in}} = v_{\text{in}}^{-1} i_{\text{in}} = v_{\text{in}}^{-1} [\mathbf{v} \quad v_{\text{in}}] Y_s \tilde{\mathbf{e}}_{n+1}$$

the constraints (5a)–(5d) in Theorem 1 correspond to the design specifications (1a)–(1d), respectively, which are already assumed to hold when switches $p_1, p_2, \ldots, p_k$ are turned on.

2) The constraint (5e) corresponds to the design specification (1e) [due to the equality (7)].

3) The constraint (5f) corresponds to the relation (8) on noting that

$$\mathbf{x}_j = v_j^* [\mathbf{v} \quad v_{\text{in}}], \qquad \forall\, j \in \{1, 2, \ldots, n\}.$$

4) The condition $X = X^*$ given in (5g) holds due to the definition of matrix X in (9) as

$$X = \begin{bmatrix} \mathbf{v}^* \\ v_{\text{in}} \end{bmatrix} [\mathbf{v} \quad v_{\text{in}}].$$

5) The rank of the matrix provided in (4) is equal to one in light of the vector decomposition

$$\begin{bmatrix} X & \begin{bmatrix} \mathbf{u}^* \\ v_{\text{in}} \end{bmatrix} \\ [\mathbf{u} \quad v_{\text{in}}] & 1 \end{bmatrix} = \begin{bmatrix} \mathbf{v}^* \\ v_{\text{in}} \\ 1 \end{bmatrix} [\mathbf{v} \quad v_{\text{in}} \quad 1].$$

Proof of Sufficiency: Assume that there exist a matrix $X \in \mathbf{C}^{(n+1)\times(n+1)}$ and a vector $\mathbf{u} \in \mathbf{C}^{1\times n}$ such that the rank of matrix (4) is equal to one and such that the constraints in (5) are all satisfied. Identify every index $j \in \{z+1, \ldots, n\}$ for which the jth entry of $\mathbf{u}$ is zero, and denote the set of all such indices as $\{p_1, p_2, \ldots, p_k\}$. The intent is to prove that Problem 1 is feasible, and indeed, the design specifications (1) are satisfied for Circuit 2 when switches $p_1, p_2, \ldots, p_k$ are turned on. To this end, consider the matrix

$$\begin{bmatrix} X & \begin{bmatrix} \mathbf{u}^* \\ v_{\text{in}} \end{bmatrix} \\ [\mathbf{u} \quad v_{\text{in}}] & 1 \end{bmatrix} \tag{10}$$

whose rank is assumed to be one. Since X satisfies constraint (5g), this matrix is Hermitian. Since the aforementioned matrix is both Hermitian and rank 1, one can apply the singular value decomposition theorem to this matrix to infer that there exists

a vector $\boldsymbol{\alpha} \in \mathbf{C}^{n+2}$ such that this matrix is equal to either $\boldsymbol{\alpha}\boldsymbol{\alpha}^*$ or $-\boldsymbol{\alpha}\boldsymbol{\alpha}^*$. However, the last diagonal entry of matrix (10), being equal to one, does not allow this matrix to be equal to the negative semidefinite matrix $-\boldsymbol{\alpha}\boldsymbol{\alpha}^*$. Hence

$$\begin{bmatrix} X & \begin{bmatrix} \mathbf{u}^* \\ v_{\text{in}} \end{bmatrix} \\ \begin{bmatrix} \mathbf{u} & v_{\text{in}} \end{bmatrix} & 1 \end{bmatrix} = \boldsymbol{\alpha}\boldsymbol{\alpha}^*.$$

This relation can be simplified to obtain

$$\boldsymbol{\alpha}^* = \pm[\mathbf{u} \quad v_{\text{in}} \quad 1].$$

As a result, X satisfies the equation

$$X = \begin{bmatrix} \mathbf{u}^* \\ v_{\text{in}} \end{bmatrix} [\mathbf{u} \quad v_{\text{in}}]. \tag{11}$$

Define now

$$\tilde{\mathbf{u}} := [\mathbf{u} \quad v_{\text{in}}] Y_s \tag{12}$$

and denote the jth entries of $\mathbf{u}$ and $\tilde{\mathbf{u}}$ with u_j and $\tilde{u}_j$, respectively, for every $j \in \{1, 2, \ldots, n\}$. Equality (5e) yields

$$\tilde{u}_j = 0, \qquad \forall j \in \{1, 2, \ldots, z\}.$$

Likewise, (5f), (11), and (12) lead to

$$u_j^* \tilde{u}_j = 0, \qquad \forall j \in \{z+1, z+2, \ldots, n\}$$

or

$$\tilde{u}_j = 0, \qquad \forall j \in \{z+1, z+2, \ldots, n\} \setminus \{p_1, p_2, \ldots, p_k\}$$

(because u_j is assumed to be nonzero if $j \in \{z+1, z+2, \ldots, n\} \setminus \{p_1, p_2, \ldots, p_k\}$). So far, it is shown that there are two vectors $\mathbf{u} \in \mathbf{C}^{1\times n}$ and $\tilde{\mathbf{u}} \in \mathbf{C}^{1\times(n+1)}$ such that

1) the relation $\tilde{\mathbf{u}} = [\mathbf{u} \quad v_{\text{in}}] Y_s$ holds;
2) $\tilde{u}_j$ is equal to zero for every $j \in \{1, 2, \ldots, z\}$;
3) u_j is equal to zero for every $j \in \{p_1, p_2, \ldots, p_k\}$;
4) $\tilde{u}_j$ is equal to zero for every $j \in \{z+1, z+2, \ldots, n\} \setminus \{p_1, p_2, \ldots, p_k\}$.

It can be concluded from these properties and the set of equations in (3) that

$$\mathbf{u} = \mathbf{v} \quad \tilde{\mathbf{u}} = [\mathbf{i} \quad i_{\text{in}}]$$

where $\mathbf{v}$, $\mathbf{i}$, and i_{in} are the parameters of Circuit 2 when switches $p_1, p_2, \ldots, p_k$ are turned on. Now, notice that the design specifications (1a)–(1e) are equivalent to (5a)–(5e) in Theorem 1, respectively (see the proof of necessity for an explanation of this equivalency). Hence, the design specifications are satisfied for this particular switching in Circuit 2. ■

Theorem 1 states that Problem 1 is tantamount to an optimization problem whose constraints are all linear. However, the rank of a Hermitian matrix is to be minimized, which makes the problem nonconvex. Since a rank-minimization problem is NP-hard in general, there may not be an efficient algorithm to exactly solve it. The possibility of using a heuristic method to solve this problem will be discussed later in Section III-D.

A question arises as to whether it is possible to convert Problem 1 to another optimization problem that can be efficiently solved using deterministic algorithms (rather than randomized or heuristic algorithms). This question is tackled in the Appendix, where it is shown that Problem 1 is NP-complete, which makes it one of the hardest problems from the computational point of view. An intuitive argument for the NP-completeness of Problem 1 is as follows: *the constraint that each controllable port must be connected to an ideal switch can be interpreted as the input power of each port must be exactly zero. Since the power is a nonconvex function of the voltage and current parameters, deciding whether there are appropriate voltage and current values to make several power terms precisely equal to zero becomes a hard problem.*

We wish to study how Problem 1 can be slightly modified so that it becomes convex. This is the crux of the next section.

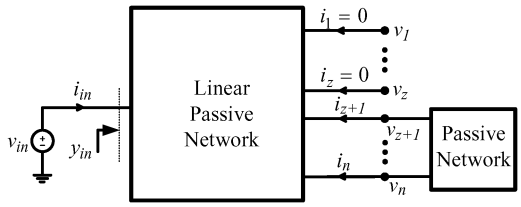

Fig. 6. Circuit 3 obtained from Circuit 1 by using a linear and passive control unit.

B. Passive Control Unit

The nonconvexity of Problem 1 originates from the fact that the output ports $z+1, z+2, \ldots, n$ are controlled by ideal switches. In this part, let the control unit in Circuit 1 be a general linear and strictly passive network, as opposed to a switching network. This leads to Circuit 3, shown in Fig. 6. Henceforth, assume that the network corresponding to the admittance Y_s is *strictly* passive (rather than being only passive). The objective of this section is formalized in the following.

Problem 2: Find whether it is possible to design a control unit in the form of a linear and strictly passive (reciprocal) network such that the design specifications given in (1) are met for Circuit 3.

Let Y denote the admittance of the linear and strictly passive network that is being designed at a given frequency ω_0. Note that the reciprocity condition in the aforementioned problem can be translated as the real and imaginary parts of Y are both symmetric. It is aimed to show that Problem 2 can be turned into a convex optimization problem with a simple form. In what follows, a lemma is presented, which will be used later to prove this important result.

Lemma 1: Given symmetric matrices $M, N \in \mathbf{R}^{n\times n}$, if M is nonsingular, then the following statements are equivalent.

1) M is a positive definite matrix.
2) $M + NM^{-1}N$ is a positive definite matrix.

Proof: First, assume that M is a positive definite matrix. Thus, M^{-1} is positive definite and so is $NM^{-1}N$. This implies that $M + NM^{-1}N$ is a positive definite matrix. So far, it

is shown that 1) implies 2). To complete the proof, it remains to show that the converse statement is also true. To this end, assume that $M + NM^{-1}N$ is a positive definite matrix. Define the matrices

$$P := \begin{bmatrix} M & N \\ N & -M \end{bmatrix}$$
$$T := \begin{bmatrix} I & -NM^{-1} \\ 0 & I \end{bmatrix}$$
$$Q := \begin{bmatrix} M + NM^{-1}N & 0 \\ 0 & -M \end{bmatrix}. \tag{13}$$

It is easy to verify that $P = TQT^*$. Denote the number of positive, negative, and zero eigenvalues of the symmetric matrix P with η_1, η_2, and η_3, respectively. Analogously, denote the same quantities of matrix Q with the triple $(\bar{\eta}_1, \bar{\eta}_2, \bar{\eta}_3)$. Since matrix T is nonsingular, applying the Sylvester's Law of Inertia to the relation $P = TQT^*$ yields

$$(\eta_1, \eta_2, \eta_3) = (\bar{\eta}_1, \bar{\eta}_2, \bar{\eta}_3). \tag{14}$$

On the other hand, it can be concluded from the Hamiltonian structure of matrix P that

$$\eta_1 = \eta_2. \tag{15}$$

Furthermore, since every eigenvalue of $M + NM^{-1}N$ is an eigenvalue of Q and since all eigenvalues of $M + NM^{-1}N$ are positive, the quantity $\bar{\eta}_1$ is at least equal to n. In light of the equalities (14) and (15), the relation $\bar{\eta}_1 \geq n$ is possible only if $\eta_1 = \eta_2 = \bar{\eta}_1 = \bar{\eta}_2 = n$. Thus, matrix Q has n negative eigenvalues. Nonetheless, the negative eigenvalues of this matrix are the same as those of matrix $-M$; hence, $-M \in \mathbf{R}^{n\times n}$ has the maximum number of negative eigenvalues. This simply proves that the eigenvalues of M are all positive, which completes the proof. ∎

Decompose matrix Y_s in a block form as

$$Y_s = \begin{bmatrix} W_{11} & W_{12} & W_{13} \\ W_{21} & W_{22} & W_{23} \\ W_{31} & W_{32} & W_{33} \end{bmatrix}$$

where $W_{11} \in \mathbf{C}^{z\times z}$, $W_{22} \in \mathbf{C}^{(n-z)\times(n-z)}$, and $W_{33} \in \mathbf{C}$. For the given symmetric square matrices A and B of the same dimension with $\det(A) \neq 0$, it can be verified that

$$(A + B\mathrm{i})^{-1} = (A + BA^{-1}B)^{-1} - (A + BA^{-1}B)^{-1}BA^{-1}\mathrm{i} \tag{16}$$

where "i" stands for the imaginary unit. This identity will be exploited in the next theorem.

Theorem 2: Problem 2 is feasible if and only if there exist symmetric matrices $M, N \in \mathbf{R}^{(n-z)\times(n-z)}$ and vectors $\mathbf{u}_1 \in \mathbf{C}^{1\times z}$ and $\mathbf{u}_2 \in \mathbf{C}^{1\times(n-z)}$ such that

$$\begin{bmatrix} \left(\mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\}\right)^{-1} - M & N \\ N & M \end{bmatrix} \succ 0 \tag{17}$$

and such that

$$\left|\mathrm{Re}\{[\mathbf{u}_1 \quad \mathbf{u}_2]e_j - v_j^d\}\right| \leq \varepsilon_j, \qquad \forall j \in \{1, 2, \ldots, z\} \tag{18a}$$
$$\left|\mathrm{Im}\{[\mathbf{u}_1 \quad \mathbf{u}_2]e_j - v_j^d\}\right| \leq \bar{\varepsilon}_j, \qquad \forall j \in \{1, 2, \ldots, z\} \tag{18b}$$
$$\left|\mathrm{Re}\{v_{\mathrm{in}}^{-1}\mathbf{u}_1W_{13} + v_{\mathrm{in}}^{-1}\mathbf{u}_2W_{23} + W_{33} - y_{\mathrm{in}}^d\}\right| \leq \varepsilon \tag{18c}$$
$$\left|\mathrm{Im}\{v_{\mathrm{in}}^{-1}\mathbf{u}_1W_{13} + v_{\mathrm{in}}^{-1}\mathbf{u}_2W_{23} + W_{33} - y_{\mathrm{in}}^d\}\right| \leq \bar{\varepsilon} \tag{18d}$$
$$\mathbf{u}_1 = -\mathbf{u}_2W_{21}W_{11}^{-1} - v_{\mathrm{in}}W_{31}W_{11}^{-1} \tag{18e}$$
$$\mathbf{u}_2 = v_{\mathrm{in}}\left(W_{31}W_{11}^{-1}W_{12} - W_{32}\right)(M + N\mathrm{i}). \tag{18f}$$

Moreover, if there exist such matrices M and N satisfying the aforementioned constraints, then one candidate for the admittance matrix Y is

$$Y = (M + N\mathrm{i})^{-1} - W_{22} + W_{21}W_{11}^{-1}W_{12}. \tag{19}$$

Proof of Necessity: Assume that there exists a linear and passive controller (control unit) with an admittance Y at frequency ω_0 such that the design specifications listed in (1) are satisfied for Circuit 3 under this controller. The objective is to prove that there exist symmetric matrices $M, N \in \mathbf{R}^{(n-z)\times(n-z)}$ and vectors $\mathbf{u}_1 \in \mathbf{C}^{1\times z}$ and $\mathbf{u}_2 \in \mathbf{C}^{1\times(n-z)}$ for which the constraints given in (17) and (18) are satisfied. For this purpose, consider Circuit 3 under the passive network Y, and define the vectors

$$\mathbf{v}_1 = [\, v_1 \quad v_2 \quad \cdots \quad v_z \,]$$
$$\mathbf{v}_2 = [\, v_{z+1} \quad v_{z+2} \quad \cdots \quad v_n \,].$$

Two equations can be written for Circuit 3 as follows:

$$[\mathbf{i} \quad i_{\mathrm{in}}] = [\, \mathbf{v}_1 \quad \mathbf{v}_2 \quad v_{\mathrm{in}} \,]Y_s$$
$$[\mathbf{i} \quad i_{\mathrm{in}}] = -[\, \mathbf{v}_1 \quad \mathbf{v}_2 \quad v_{\mathrm{in}} \,] \begin{bmatrix} 0 & 0 & 0 \\ 0 & Y & 0 \\ 0 & 0 & -y_{\mathrm{in}} \end{bmatrix}. \tag{20}$$

These equations can be combined to obtain

$$\mathbf{v}_1W_{11} + \mathbf{v}_2W_{21} + v_{\mathrm{in}}W_{31} = 0$$
$$\mathbf{v}_1W_{12} + \mathbf{v}_2(W_{22} + Y) + v_{\mathrm{in}}W_{32} = 0$$
$$\mathbf{v}_1W_{13} + \mathbf{v}_2W_{23} + v_{\mathrm{in}}(W_{33} - y_{\mathrm{in}}) = 0.$$

The aforementioned relations can be manipulated to arrive at

$$\mathbf{v}_1 = -\mathbf{v}_2W_{21}W_{11}^{-1} - v_{\mathrm{in}}W_{31}W_{11}^{-1} \tag{21a}$$
$$\mathbf{v}_2 = v_{\mathrm{in}}\left(W_{31}W_{11}^{-1}W_{12} - W_{32}\right)\tilde{Y} \tag{21b}$$
$$y_{\mathrm{in}} = v_{\mathrm{in}}^{-1}\mathbf{v}_1W_{13} + v_{\mathrm{in}}^{-1}\mathbf{v}_2W_{23} + W_{33} \tag{21c}$$

where

$$\tilde{Y} := \left(W_{22} - W_{21}W_{11}^{-1}W_{12} + Y\right)^{-1}. \tag{22}$$

Note that the invertibility of the term $W_{22} - W_{21}W_{11}^{-1}W_{12} + Y$ follows from the strict passivity of Y and Y_s. It is desired to show that constraints (17) and (18) in Theorem 2 hold if M, N, $\mathbf{u}_1$, and $\mathbf{u}_2$ are defined as

$$M := \mathrm{Re}\{\tilde{Y}\} \quad N := \mathrm{Im}\{\tilde{Y}\}$$
$$\mathbf{u}_1 := \mathbf{v}_1 \quad \mathbf{u}_2 := \mathbf{v}_2.$$

To this end, first observe that M and N are symmetric matrices due to the reciprocity of Y and Y_s. Moreover, it can be con-

cluded from the aforementioned definitions and (21c) that the constraints (18a)–(18d) correspond to the design specifications (1a)–(1d), respectively, which are assumed to hold for Circuit 3. The constraints (18e) and (18f), on the other hand, are satisfied in light of the relations (21a) and (21b). The only challenging part is to show that inequality (17) in Theorem 2 holds. For this purpose, notice that the strict passivity of the network associated with Y implies the relation $\mathrm{Re}\{Y\} \succ 0$[1]. By applying identity (16) to (22) and by using this fact, one can write

$$\begin{aligned}\mathrm{Re}\{Y\} &= \mathrm{Re}\left\{\tilde{Y}^{-1} - W_{22} + W_{21}W_{11}^{-1}W_{12}\right\} \\ &= (M + NM^{-1}N)^{-1} \\ &\quad - \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \succ 0. \end{aligned} \tag{23}$$

Since the term $(W_{22} - W_{21}W_{11}^{-1}W_{12})^{-1}$ is the (1,1) block entry of the inverse of the matrix

$$\begin{bmatrix} W_{11} & W_{12} \\ W_{21} & W_{22} \end{bmatrix}$$

which is a principal submatrix of Y_s, it follows from the strict passivity of the admittance matrix Y_s that

$$\mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \succ 0. \tag{24}$$

Inequalities (23) and (24) lead to

$$(M + NM^{-1}N)^{-1} \succ \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \succ 0. \tag{25}$$

The following two properties can be deduced from this relation.

1) First, Lemma 1 yields

$$M \succ 0. \tag{26}$$

2) Second, inequality (25) can be rearranged to obtain

$$\left(\mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\}\right)^{-1} \succ M + NM^{-1}N$$

or equivalently

$$\left(\mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\}^{-1} - M\right) - NM^{-1}N \succ 0. \tag{27}$$

Schur's complement formula can be used to conclude that inequalities (26) and (27) are equivalent to (17). This completes the proof of necessity.

Proof of Sufficiency: Since the proof can be carried out in line with the approach taken at the proof of necessity, only a sketch of the proof will be provided here. Assume that the constraints given in (17) and (18) are satisfied for some symmetric matrices $M, N \in \mathbf{R}^{(n-z)\times(n-z)}$ and vectors $\mathbf{u}_1 \in \mathbf{C}^{1\times z}$ and $\mathbf{u}_2 \in \mathbf{C}^{1\times(n-z)}$. The goal is to show that the design specifications listed in (1) are met for Circuit 3 if the admittance Y of the passive controller (at frequency ω_0) is considered as

$$Y = (M + N\mathrm{i})^{-1} - W_{22} + W_{21}W_{11}^{-1}W_{12}.$$

For this choice of matrix Y, it follows from (18f) and (21b) that $\mathbf{u}_2$ is equal to $\mathbf{v}_2$. Then, it can be concluded from (18e) and (21a) that $\mathbf{u}_1 = \mathbf{v}_1$. Now, one can easily verify that the design specifications (1a)–(1d) correspond to the inequalities (18a)–(18d), respectively, which are assumed to hold. On the other hand, the design specification (1e) is satisfied in light of the relation (18e) and the equality

$$[\,i_1 \quad i_2 \quad \cdots \quad i_z\,] = v_1W_{11} + v_2W_{21} + v_{\mathrm{in}}W_{31}$$

[see (20)]. Hence, it only remains to show that matrix Y introduced earlier corresponds to a strictly passive network. This can be shown using Lemma 1 and Schur's complement formula in line with the argument pursued in the proof of necessity. The details are omitted for brevity. ■

Regarding the optimization problem proposed in Theorem 2, it is easy to observe that the constraints are all linear. Therefore, Theorem 2 states that Problem 2 is equivalent to an LMI feasibility problem, which can be handled efficiently using a proper software tool such as YALMIP or SOSTOOLS [22], [23]. This signifies that replacing switches with a passive network facilitates the circuit design at the cost of complicating its implementation in practice. In the case when it is strictly required to design a collection of switches, Theorem 2 is still useful. Indeed, since Circuit 2 is a special form of Circuit 3, the infeasibility of Problem 2 implies the infeasibility of Problem 1. As a result, one can regard the LMI problem proposed in Theorem 2 as a sanity test for checking the feasibility of Problem 1.

Assume that Problem 2 is feasible, and therefore, an admittance matrix Y (at frequency ω_0) can be obtained by solving the feasibility problem given in Theorem 2. The next step is to design a reciprocal passive network whose corresponding admittance transfer function at frequency ω_0 is equal to Y. To find such a network, note that the real part of Y is a positive definite matrix and that its imaginary part is symmetric. As a result, matrix Y can be expressed as

$$Y = T_1 + T_2\mathrm{i}$$

where T_1 and $T_2 \in \mathbf{R}^{(n-z)\times(n-z)}$ are both symmetric, and T_1 is positive definite. Define an admittance transfer function $Y(s)$ as

$$Y(s) = T_1 + \frac{1}{\omega_0}T_2 s, \qquad \forall\, s \in \mathbf{C}.$$

It is evident that $Y(\mathrm{i}\omega_0) = Y$. On the other hand, $Y(s)$ can be implemented by the parallel connection of two $(n-z)$-port networks: 1) a resistive network with the conductance matrix T_1 and 2) a reactive network with the susceptance matrix $(1/\omega_0)T_2$. Note that some ideal transformers might also be needed to realize $Y(s)$ due to the multiport nature of the network. One can refer to [1] and [2] for the detailed discussions on the realization of a given admittance matrix by passive elements.

C. Decoupled Passive Control Unit

The main issue with the admittance matrix Y obtained in Theorem 2 is that its corresponding passive network could potentially have several components (electrical elements), which may complicate its implementation. To circumvent this drawback, one can impose a sparsity constraint on Y to make it diagonal. Note that Circuit 3, under a passive control unit with a diagonal admittance transfer function, is equivalent to *Circuit 4*,

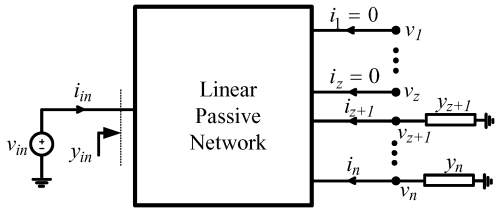

Fig. 7. Circuit 4 obtained from Circuit 1 by using a decoupled, linear, and passive control unit.

shown in Fig. 7. Alternatively, one can reason that Circuit 4 is obtained from Circuit 2 (as opposed to Circuit 3) by replacing the ideal switches with varactors. Define Problem 3 to be the same as Problem 2 but under the additional constraint of the diagonality of Y. It will be shown in the sequel that Problem 3 is nonconvex. However, there is a good heuristic method for this problem, as tested on several practical examples.

Theorem 3: Minimize the rank of the matrix

$$\begin{bmatrix} \bar{P} & I \\ I & P \end{bmatrix} \tag{28}$$

for vectors $\mathbf{u}_1 \in \mathbf{C}^{1\times z}$ and $\mathbf{u}_2 \in \mathbf{C}^{1\times(n-z)}$, symmetric matrices $M, N \in \mathbf{R}^{(n-z)\times(n-z)}$, and diagonal matrices $D_1, D_2 \in \mathbf{R}^{(n-z)\times(n-z)}$ that are subject to the constraints given in (18) and

$$D_1 \succ 0$$
$$M \succ 0$$

where P and $\bar{P}$ are provided in (13) and (29), respectively ((29) is shown at the bottom of the page). Problem 3 is feasible if and only if the value of the minimum rank is less than or equal to $2(n-z)$, in which case the feasible solution for the diagonal admittance matrix Y is as follows:

$$Y = D_1 + D_2\mathrm{i}.$$

Proof: When there is no diagonality constraint on matrix Y, a necessary and sufficient condition for the existence of a desirable network is provided in Theorem 2. Hence, it suffices to incorporate this extra constraint into the aforementioned condition. To this end, write Y as $D_1 + D_2\mathrm{i}$, where D_1 and D_2 are required to be diagonal. It results from (19) that

$$D_1 + D_2\mathrm{i} + W_{22} - W_{21}W_{11}^{-1}W_{12} = (M + N\mathrm{i})^{-1}. \tag{30}$$

Applying identity (16) to the aforementioned equation yields

$$D_1 + \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} = (M + NM^{-1}N)^{-1}$$
$$D_2 + \mathrm{Im}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} = -(M + NM^{-1}N)^{-1} \times NM^{-1}.$$

These equations can be written in the matrix form (31) (see equation at the bottom of the page) or equivalently $\bar{P} = P^{-1}$. On the other hand

$$\begin{bmatrix} \bar{P} & I \\ I & P \end{bmatrix} = \begin{bmatrix} I & P^{-1} \\ 0 & I \end{bmatrix} \begin{bmatrix} \bar{P} - P^{-1} & 0 \\ 0 & P \end{bmatrix} \begin{bmatrix} I & 0 \\ P^{-1} & I \end{bmatrix}. \tag{32}$$

In light of the equality $\bar{P} - P^{-1} = 0$ and the nonsingularity of P, it follows from the aforementioned equation that the rank of the matrix given in (28) is exactly equal to $2(n-z)$. So far, it is shown that the diagonality of matrix Y implies the aforementioned rank constraint. To prove the converse statement, notice that the condition $M \succ 0$ makes the Hamiltonian matrix P nonsingular (see the proof of Lemma 1). This, together with identity (32), implies that, if the rank of the matrix in (28) is less than or equal to $2(n-z)$, then the matrix $P - \bar{P}^{-1}$ must be zero. This result leads to (30), which is indeed a diagonality constraint on matrix Y. Moreover, one can easily replace the passivity constraint (17) given in Theorem 2 with the condition $D_1 > 0$ because the real part of matrix Y is equal to D_1. ■

Remark 1: Unlike Problem 2 that had a convex formulation, Problem 3 turned out to be a rank-minimization problem that is not convex. A question arises as to what makes Problem 3 hard. To answer this question, consider the special case when the circuit is resistive and when the controller to be designed needs to be resistive as well. This particular case makes all complex variables real valued, which will reveal later the design difficulties. Notice that, since each controllable port must be connected to a resistor, the following power constraints should be satisfied:

$$v_j i_j \leq 0, \qquad \forall\, j \in \{z+1, \ldots, n\}. \tag{33}$$

Given $j \in \{z+1, \ldots, n\}$, this means that one of the cases $v_j \leq 0, i_j \geq 0$ or $v_j \geq 0, i_j \leq 0$ must occur, which implies that there are two possibilities for the parameters (v_j, i_j). Hence, it follows from (33) that there are 2^{n-z} possibilities for the parameters $(v_{z+1}, \ldots, v_n, i_{z+1}, \ldots, i_n)$. As a result, the aforementioned power constraints correspond to a nonconvex feasibility region that is composed of an exponential number (2^{n-z}) of convex parts attached to each other at the origin. This highly nonconvex feasibility region is the source of difficulty in tackling Problem 3.

$$\bar{P} := \begin{bmatrix} D_1 + \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} & -D_2 - \mathrm{Im}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \\ -D_2 - \mathrm{Im}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} & -D_1 - \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \end{bmatrix} \tag{29}$$

$$\begin{bmatrix} D_1 + \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} & -D_2 - \mathrm{Im}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \\ -D_2 - \mathrm{Im}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} & -D_1 - \mathrm{Re}\left\{W_{22} - W_{21}W_{11}^{-1}W_{12}\right\} \end{bmatrix} = \begin{bmatrix} M & N \\ N & -M \end{bmatrix}^{-1} \tag{31}$$

D. Heuristic Method for Rank Minimization

Since the optimization problems given in Theorems 1 and 3 are associated with the rank constraints, the objective of this part is to study the rank-minimization problems. Consider a standard rank optimization problem in the form of

$$\begin{aligned} &\text{minimize } \operatorname{rank}(X) \\ &\text{subject to } \quad \mathcal{A}(X) = b \end{aligned} \tag{34}$$

where

X	an $n_1 \times n_2$ matrix decision variable (n_1 and n_2 are given numbers);
$\mathcal{A} : \mathbf{R}^{n_1 \times n_2} \to \mathbf{R}^m$	a known linear map;
b	a given vector in $\mathbf{R}^m$

It is known that the optimization problem (34) is NP-hard, in general. However, several heuristic methods have been proposed in the literature to relax the problem to a convex one, whose solution may be identical or near to that of the original problem [12], [21]. The heuristic method developed in the studies in [12] and [13] has been widely used in the literature. This method suggests solving the following optimization problem instead of (34):

$$\begin{aligned} &\text{minimize } \quad \|X\|_* \\ &\text{subject to } \quad \mathcal{A}(X) = b \end{aligned} \tag{35}$$

where $\|X\|_*$ denotes the nuclear norm of matrix X (defined as the sum of the singular values of X). The main advantage of this heuristic method is that the optimization problem (35) is convex, and thus, its global solution can be efficiently found.

An important question arises as to when will the solutions of optimizations (34) and (35) coincide. To answer the raised question probabilistically, represent the linear map $\mathcal{A}(X)$ in the matrix form as $A \times \operatorname{vec}(X)$, where $A \in \mathbf{R}^{m \times n_1 n_2}$ is a matrix and $\operatorname{vec}(X)$ is a vector obtained from X by stacking up the columns of X. It is shown in [14] that, as m goes to infinity, the probability that optimizations (34) and (35) have the same solution is equal to one if the entries of matrix A are independently sampled from a zero-mean unit-variance Gaussian distribution. In other words, the aforementioned heuristic method works almost always correctly for a standard rank-minimization problem whose linear constraints are randomly generated using a Gaussian probability distribution.

The rank-minimization problems given in Theorems 1 and 3 can be handled using the heuristic method discussed earlier. As a result, the nuclear norm of matrices (4) and (28) should be minimized in the related optimization problems, instead of their ranks. In case this heuristic method leads to a rank greater than one for the optimization problem in Theorem 1 or $2(n-z)$ for the optimization problem in Theorem 3, there are two possibilities: 1) Problem 1 (or Problem 3) is infeasible, and 2) the heuristic method fails to find a solution with the minimum rank. One can use the necessary and sufficient condition derived in [14] to see if case 1) takes place, although this may be complicated. Note that, since the optimization problems in Theorems 1 and 3 are highly structured (partially due to the presence of fixed elements 1 and I as well as the Hamiltonian matrix in the constraints), these optimizations may be far from being a Gaussian random instance of a rank-minimization problem. Therefore, they may not lie into the category of problems for which the aforementioned heuristic method almost always works correctly (note that the results developed in [14] are applicable to these optimizations because they can be transformed into the standard form (34) using the technique delineated therein).

An extensive simulation was done by the authors to test the efficiency of the nuclear norm heuristic method on different antenna problems. A number of important observations were made as follows.

1) The heuristic method works correctly all the time for the optimization problem in Theorem 3 if there are no constraints on $v_1, v_2, \ldots, v_z$, i.e., if all constraints are on y_{in}.
2) Some of the design specifications may be violated a little if the heuristic method is applied to the optimization problem of Theorem 3, with some constraints on the output voltages $v_1, v_2, \ldots, v_z$. For example, given an index $j \in \{1, 2, \ldots, z\}$, the real part of the obtained voltage v_j that is required to belong to the interval $[\operatorname{Re}\{v_j^d\} - \varepsilon_j, \operatorname{Re}\{v_j^d\} + \varepsilon_j]$ might lie a bit off this range.
3) The nuclear norm heuristic method often fails to obtain a satisfactory result when applied to Theorem 1.

It is shown in the Appendix that Problem 1 is NP-complete, and since an NP-complete problem is well understood to be very hard to solve, it is commonly believed that a convex heuristic method (such as the aforementioned one) often fails to find a satisfactory solution. This might be the reason for observation 3).

E. Design Simplicity Versus Implementation Complexity

It is desired to compare Circuits 2, 3, and 4 in terms of their design and implementation. To this end, the main properties of these circuits can be summarized as follows.

1) The implementation of a control unit for Circuit 2 requires only $n - z$ switches, but finding the on/off status of every switch to satisfy the design specifications is an NP-complete problem. As a result, the synthesis of such a circuit can be extremely difficult when the number of switches, i.e., $n - z$, is greater than 30 (because the discrete space of all switching combinations has 2^{n-z} elements, which is a very large set if $n - z > 30$).
2) The implementation of a control unit for Circuit 3 requires about $0.5(n-z)^2$ components (e.g., resistors, capacitors, and inductors). This may make the implementation of such a controller difficult for some applications. Nonetheless, the synthesis of a passive control unit can be converted to an LMI feasibility problem, which can be efficiently handled even when $n - z$ is on the order of several thousands.
3) The implementation of a control unit for Circuit 4 requires only $n-z$ components. Hence, the number of components in the controller grows linearly with respect to the number of controllable ports (i.e., $n-z$), which is a useful property for large-scale systems. Even though the synthesis of such a controller is tantamount to a rank-minimization problem, it may be solved using a heuristic method (as mentioned earlier), particularly when there are not so many constraints on the output voltages.

The aforementioned discussion leads to the conclusion that, since the synthesis of Circuit 2 is very difficult even for moderate-sized systems, it is preferable to deploy either Circuit 3 or 4. In the case when it is desired to design a control unit online (as demanded in antenna applications due to the periodic change of the design specifications), Circuit 3 is a more suitable choice

compared to Circuit 4. However, the implementation of Circuit 4 is much simpler than that of Circuit 3 for large-scale systems.

Remark 2: To reduce the implementation complexity of Circuit 3, it is preferable to use a small subset of the $n-z$ controllable ports, if possible. More specifically, it might be possible to satisfy the design specifications only by controlling a few of the controllable ports. Hence, one can take the following strategy: check whether a passive control unit can be designed for port $z+1$ to satisfy the design objectives (1); if not, verify the existence of a controller for ports $z+1$ and $z+2$; and continue this procedure up to the point where enough number of controllable ports are found whose passive control makes us meet the design specifications. This heuristic method can significantly reduce the implementation complexity.

F. Generalizations

Problems 1, 2, and 3 studied in this paper target a circuit synthesis, with the design specifications given in (1). However, the techniques developed here can be generalized to incorporate other types of design specifications. For example, assume that an output voltage v_p, where $p \in \{1,2,\ldots,z\}$, is required to be sufficiently weak, as demanded by antenna applications. This constraint can be formalized as $\|v_p\| \leq \tilde{\varepsilon}$, where $\|\cdot\|$ denotes the two norms and $\tilde{\varepsilon}$ is a given positive number. To account for this new design specification, the constraint

$$\|\mathbf{u}\mathbf{e}_p\| \leq \varepsilon$$

should be added to the optimization problem of Theorem 1. Likewise, the constraint

$$\|[\mathbf{u}_1 \quad \mathbf{u}_2]\mathbf{e}_p\| \leq \varepsilon$$

should be included in the optimization problems of Theorems 2 and 3. As another example, if one needs to design a control unit for Circuit 1 in the form of a decoupled *lossless* network, it suffices to replace the constraint $D_1 > 0$ with $D_1 = 0$ in the optimization problem of Theorem 3.

Unlike Theorems 1 and 3 that propose *minimization* problems, Theorem 2 offers a *feasibility* problem. In other words, there is no specific quantity in the feasibility problem of Theorem 2 that must be minimized (or maximized). This provides a degree of freedom in the underlying circuit synthesis. To be more precise, Theorem 2 can be employed to simultaneously solve Problem 2 and to minimize (maximize) some quantity of interest such as the consumed power at a specific port. This point will be illustrated in the next section through some simulations.

As another generalization, assume that the goal is to design a passive control unit with a prespecified structure. An example of this case is the filter shown in Fig. 4 whose control unit is structured in terms of the impedances Z_1 to Z_5. To handle this problem, it suffices to employ Theorem 3 after the following slight modifications.

1) Replace the diagonality requirement of the matrix variables D_1 and D_2 with a desired pattern condition on these matrices, e.g., certain entries of these matrices must be zero according to the desired structure of the control unit being designed.
2) Replace the condition $D_1 > 0$ with the general passivity constraint (17).

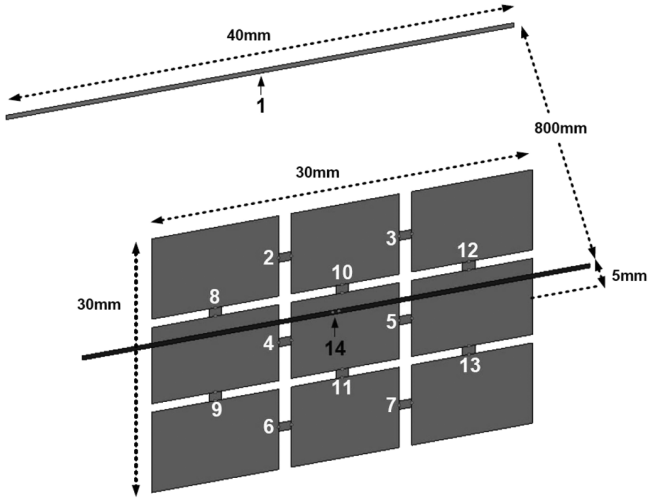

Fig. 8. Antenna problem studied in Example 1.

IV. Simulation Results

To illustrate the efficacy of the present work in the context of antenna design, note that most of the practical antenna problems deal with the optimization of the input impedance and/or the antenna gain via changing the geometry of the antenna. This is achieved in reality by means of inefficient heuristic algorithms. For instance, a PSO technique is deployed in [27] to optimize the antenna input impedance by varying its length, width, and feeding point. That algorithm was applied to a simple impedance matching problem with only three variables, which consumed more than 25 h to obtain the solution. This clearly shows that such algorithms are dramatically time consuming even for very small sized antenna problems. Two important practical examples will be studied in the sequel to demonstrate that more complicated antenna design problems with 12 and 90 variables can be solved on the order of seconds rather than hours using the method developed here.

Example 1: Consider the antenna configuration shown in Fig. 8, which consists of a transmitting dipole antenna (blue bar), a 3×3 array of metal plates (antenna parasitic elements), and a receiving dipole antenna located at the far field (green bar). There are 14 ports in this figure, which are as follows.

1) Port 1 acts as a receiving antenna sampling the radiation pattern of the transmitting antenna at a specific angle in the far field.
2) Ports 2 to 13 are intended to change the boundary condition of the transmitting antenna.
3) Port 14 corresponds to the transmitting antenna.

The objective is to find optimum impedance values for the parasitic elements such that the received power and the antenna input impedance satisfy a specific set of constraints. For this purpose, the circuit model of the antenna system is extracted at a desired frequency of 3.5 GHz (using localized differential lumped ports) by means of the EM software IE3D [24]. This model can be any of the circuits shown in Figs. 5–7, depending on how the impedances of the parasitic elements are designed. Note that n and z are equal to 13 and 1, respectively, in this example, and $v_{n+1} = v_{14} = 1$.

The three important goals in a typical antenna problem are the following: 1) received power maximization; 2) received power maximization under an input admittance constraint; and 3) input impedance matching. Tackling these problems is central to this example, which is carried out in the sequel.

TABLE I
MAXIMIZING THE RECEIVED POWER (EXAMPLE 1)

Objective function	Optimal value	Voltage at port 1	Directivity	Radiation efficiency	CPU time
$\mathrm{Re}\{v_1\}+\mathrm{Im}\{v_1\}$	0.0491	$-0.0126-0.0365$i	7.62dBi	84.72%	0.34sec
$\mathrm{Re}\{v_1\}-\mathrm{Im}\{v_1\}$	0.1423	$-0.0126+0.1297$i	6.81dBi	93.4%	0.55sec
$-\mathrm{Re}\{v_1\}+\mathrm{Im}\{v_1\}$	0.1902	$0.1536-0.0365$i	7.97dBi	85.41%	0.56sec
$-\mathrm{Re}\{v_1\}-\mathrm{Im}\{v_1\}$	0.2833	$0.1536+0.1297$i	8.17dBi	89.15%	0.63sec

TABLE II
MAXIMIZING THE RECEIVED POWER AFTER IMPOSING A CONSTRAINT ON THE INPUT IMPEDANCE OF THE ANTENNA (EXAMPLE 1)

Objective function	Optimal value	Voltage at port 1	Directivity	Radiation efficiency	CPU time
$\mathrm{Re}\{v_1\}+\mathrm{Im}\{v_1\}$	0.0432	$-0.0192-0.0240$i	7.34dBi	86.472%	0.78sec
$\mathrm{Re}\{v_1\}-\mathrm{Im}\{v_1\}$	0.0579	$-0.0192+0.0387$i	6.30dBi	90.15%	0.87sec
$-\mathrm{Re}\{v_1\}+\mathrm{Im}\{v_1\}$	0.0674	$0.0434-0.0240$i	6.56dBi	85.58%	0.86sec
$-\mathrm{Re}\{v_1\}-\mathrm{Im}\{v_1\}$	0.0821	$0.0434+0.0387$i	7.75dBi	89.3%	0.82sec

Considering the complex number v_1 as a real vector in $\mathbf{R}^2$, one can notice that the power at the receiving antenna is proportional to the two-norm of v_1 raised to the second power. Since the maximization of the two-norm of a quantity is normally a nonconvex problem, it is desired to maximize the one-norm of v_1, i.e., $|\mathrm{Re}\{v_1\}|+|\mathrm{Im}\{v_1\}|$. This suggestion is motivated by the close affinity between these two norms. Observe that the direct maximization of $|\mathrm{Re}\{v_1\}|+|\mathrm{Im}\{v_1\}|$ is again a nonconvex optimization problem. Nevertheless, one can alternatively perform four (convex) optimizations maximizing the quantities $\mathrm{Re}\{v_1\}+\mathrm{Im}\{v_1\}$, $\mathrm{Re}\{v_1\}-\mathrm{Im}\{v_1\}$, $-\mathrm{Re}\{v_1\}+\mathrm{Im}\{v_1\}$, and $-\mathrm{Re}\{v_1\}-\mathrm{Im}\{v_1\}$ and can then determine the maximum of the obtained solutions. Problem 2 is adopted to solve these optimization problems. The outcome of these convex optimization problems is summarized in Table I, which demonstrates that the optimal value of $|\mathrm{Re}\{v_1\}|+|\mathrm{Im}\{v_1\}|$ is equal to 0.2833, corresponding to an antenna directivity of 8.17 dBi and a radiation efficiency of 89.15%. It is interesting to note that this result is obtained by solving four convex optimization problems, each of which is handled by the software CVX [25] in a fraction of a second (the simulation was run on a computer with a Pentium IV 3.0 GHz and 3.62 GB of memory).

Now, assume that the objective is to maximize the power at the receiving antenna, which is subject to the constraint that the antenna input impedance is equal to the standard value of 50 Ω. As before, this power is proportional to the two-norm of the output voltage v_1 raised to the second power. The nonconvexity of the underlying problem suggests maximizing the closely related term $|\mathrm{Re}\{v_1\}|+|\mathrm{Im}\{v_1\}|$. Similar to the previous case, four convex optimization problems are solved, and the results are summarized accordingly in Table II.

As the last scenario, the goal is to find a diagonal matrix Y such that the antenna input impedance is matched with the value of 50 Ω. The heuristic method given in [13] was applied to Problem 3 to find the proper values for the diagonal matrices D_1 and D_2 (recall that $Y=D_1+D_2$i). An appropriate solution was found as

$$\begin{aligned} D_1 = \mathrm{diag}[&0, 0.0026, 0.0026, 0.0070, 0.0070, 0.0026, 0.0026,\\ &0.0138, 0.0134, 0.3252, 0.4268, 0.0136, 0.0123]\\ D_2 = \mathrm{diag}[&0, -0.0106, -0.0105, -0.0064, -0.0064,\\ &-0.0106, -0.0105, 0.0215, 0.0217, -0.0050,\\ &-0.0036, 0.0227, 0.0205] \end{aligned}$$

which corresponds to the antenna directivity of 3.55 dBi.

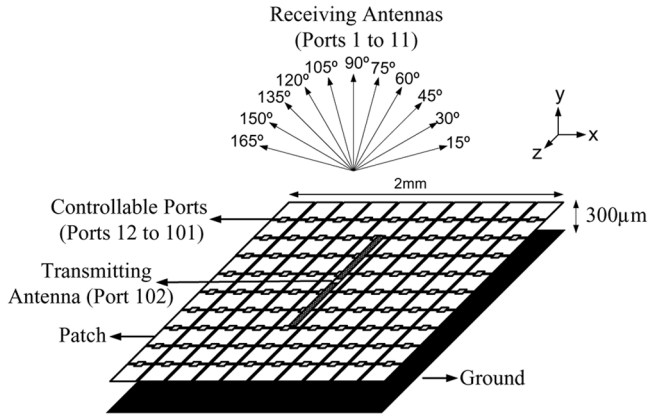

Fig. 9. Antenna system studied in Example 2.

Example 2: A general consensus in the field of antenna design is that a satisfactory beamforming making nulls at an arbitrary number of directions is possible only when a sufficient number of (antenna) active elements are exploited in such a way that the size of the antenna array becomes several multiples of the wavelength. Many works in the past decade, e.g., [28] and [29], have concentrated on designing passive array antennas that are capable of making a null only at one direction. For instance, the study in [29] presents such a design based on a genetic algorithm whose running time is reported to be more than four weeks. Using the techniques developed in the present paper, the goal of this example is to disprove the foregoing belief. To be more precise, for the first time in the literature, we wish to design an on-chip antenna system with only one active element (antenna element) of the size equal to one wavelength such that the radiation pattern makes nulls at many undesired directions. This antenna design is accomplished in a few seconds.

Consider the 2 mm $\times$ 2 mm antenna system shown in Fig. 9 consisting of a patch array with 90 controllable ports (shown by small squares), which is used for data transmission in the directions $15^\circ, 30^\circ, \ldots, 150^\circ, 165^\circ$. To study the programming capability of this antenna, a receiving antenna is placed at each of these directions in the far field (at the distance of 20 multiples of the wavelength from this transmitting antenna) with a length of 140 μm and a fixed terminal impedance of 50 Ω. The equivalent circuit model of this antenna configuration is extracted using the EM software IE3D [24], which consists of 102 ports, which are as follows.

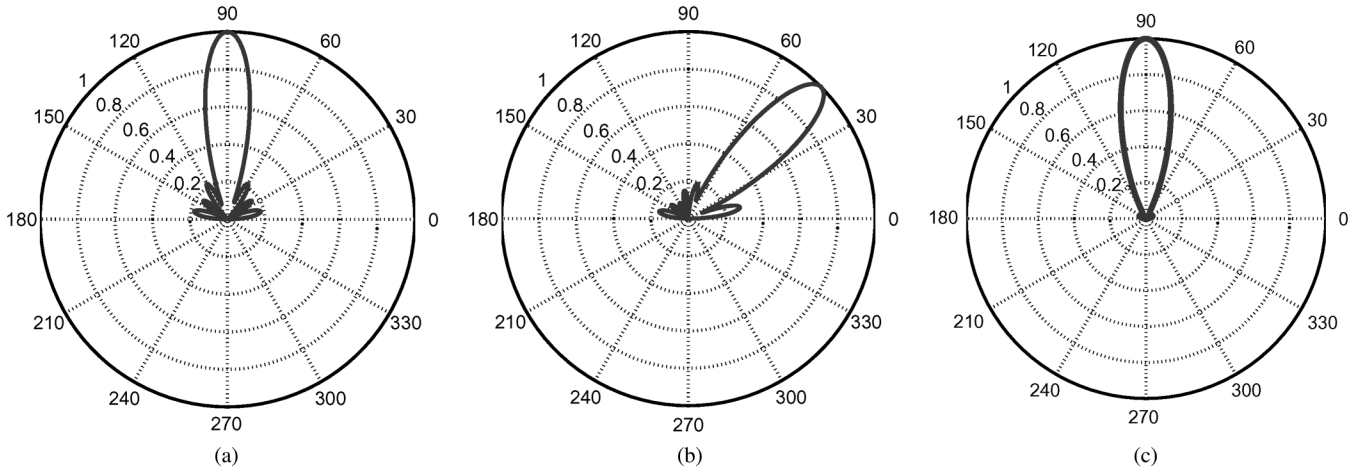

Fig. 10. (a) Radiation pattern obtained by maximizing the received power at the direction 90°. (b) Radiation pattern obtained by maximizing the received power at the direction 45°. (c) Radiation pattern obtained by maximizing the received power at the direction 90°, which is subject to the constraints $v_1 = v_2 = v_3 = v_4 = v_8 = v_9 = v_{10} = v_{11} = 0$ (Example 2).

1) *Receiving or sensing ports (ports 1 to 11)*: These ports are located in the far field to capture the radiated power at the angles $15°, 30°, \ldots, 150°, 165°$.
2) *Variable ports (ports 12 to 101)*: Every two adjacent patches in the X-direction are connected with a port, resulting in a total number of 90 ports, which are numbered from 12 to 101.
3) *Transmitting port (port 102)*: The transmitting port is located at the center of the transmitting antenna and is driven by a 300-GHz sinusoidal signal with a fixed amplitude of 1 V.

Three objectives will be pursued in this example as follows. Assume that the first objective is to transmit data at the direction 90° with the maximum power using a passive control of the antenna. This problem reduces to finding a passive controller for the antenna configuration that generates the maximum power for the output port 6. Using Theorem 2, this leads to the voltage $v_6 = 0.00303 - 0.002274\text{i}$. The corresponding radiation pattern of the antenna system is shown in Fig. 10(a). This figure shows that the antenna has an excellent beamforming capability. Indeed, while the goal was to maximize the power in one direction, the radiating power was greatly minimized in most of the remaining directions.

As the second objective, the intent is to steer the beam toward the direction 45°. Similar to the previous case, the point $v_3 = -0.00234 - 0.0030\text{i}$ is obtained with the radiation pattern shown in Fig. 10(b). The last objective is more interesting. We wish to transmit data to the direction 90°, with the maximum power subject to the constraint that a zero signal is sent to all of the directions (15°, 30°, 45°, 60°, 120°, 135°, 150°, and 165°). Theorem 2 can be exploited to show that this highly constrained pattern shaping is possible. The optimal value $v_6 = -0.000866 + 0.000589\text{i}$ is attained, and the corresponding radiation pattern is shown in Fig. 10(c). An implication of this pattern is that the technique developed in this paper has made it possible to design a wavelength-size antenna system with only one active element so that its proper control makes a null at many undesired directions while maximizing the power at a desired direction. The reader can contrast the patterns derived here with similar ones in the literature (such as the ones reported in [28] and [29]), which radiate a high power in almost all directions and make a null in at most one direction. Note that, despite the fact that the controllers designed in this example are not decoupled, one can verify that many elements of the obtained controllers are negligible, which facilitate their implementations.

V. Conclusion

This paper has studied a class of linear systems that appear in circuits, EMs, optics, etc. Given such a linear system, the objective is to design a controller for the circuit (system) such that some prescribed linear constraints on the input admittance and output voltages of the circuit are satisfied. It is shown that designing a switching controller for this circuit amounts to a rank-minimization problem, and it is indeed an NP-complete problem. Later on, the design of a passive controller is studied using the convex optimization theory. Since the implementation of a passive controller may be unacceptably complicated than a switching controller, the design of a simpler type of controller, named as *decoupled passive controller*, is also investigated. It is shown that this problem amounts to a rank-minimization one, which can be satisfactorily solved using a celebrated heuristic method. The results of the current work are developed based on available techniques in the control theory. As an important application, this paper has been exploited to design novel antenna systems with an outstanding performance.

Appendix

Consider an algorithm for a given decision problem that aims to find out whether the answer to this problem is "yes" or "no." The notion of time complexity was introduced in the literature to evaluate the efficiency of such an algorithm. Informally speaking, time complexity measures the number of machine instructions executed during the running time of the algorithm as a function of the size of the input. An efficient algorithm must run in polynomial time. For instance, if an algorithm needs an exponential number of iterations, then as the size of the problem increases, the running time of the algorithm astronomically grows. The class of NP-complete problems categorizes those problems that are believed to be extremely difficult to solve. Indeed, there is no known polynomial-time algorithm that is used to solve an NP-complete problem, and moreover, if an algorithm is discovered to solve an NP-complete problem in polynomial time, then

$$Y_s = \begin{bmatrix} \begin{bmatrix} \begin{bmatrix} 1 & -1 & 0 \\ -1 & 0 & 1 \\ 0 & 1 & -1 \end{bmatrix} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \begin{bmatrix} 1 & -1 & 0 \\ -1 & 0 & 1 \\ 0 & 1 & -1 \end{bmatrix} & \cdots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \cdots & \begin{bmatrix} 1 & -1 & 0 \\ -1 & 0 & 1 \\ 0 & 1 & -1 \end{bmatrix} \end{bmatrix} & \begin{bmatrix} \begin{bmatrix} \alpha_1 & \alpha_1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} \alpha_2 & \alpha_2 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \\ \vdots \\ \begin{bmatrix} \alpha_m & \alpha_m & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \end{bmatrix} \\ \begin{bmatrix} \begin{bmatrix} \alpha_1 & 0 & 0 \\ \alpha_1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} & \begin{bmatrix} \alpha_2 & 0 & 0 \\ \alpha_2 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} & \cdots & \begin{bmatrix} \alpha_m & 0 & 0 \\ \alpha_m & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \end{bmatrix} & \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \end{bmatrix} \mathrm{i} \tag{36}$$

the algorithm can be adapted to solve all NP problems in polynomial time [26]. It is desired to prove that the circuit switching problem posed in this paper (i.e., Problem 1) is an NP-complete problem. This is accomplished in the sequel.

Theorem 4: Problem 1 is NP-complete.

Proof: Assume that n can be written as $3m+2$ for some natural number m, and assume that $z = m+2$ (the technique being developed in the following can be adopted for other values of n). Recall that the present work considers output ports $\{1,2,\ldots,z\}$ as the ports of interest used in specifying the design objectives and ports $\{z+1,\ldots,n\}$ as the controllable ports connected to a control unit. To simplify the argument of the proof, assume with no loss of generality that ports $\{3k-2,3k|k=1,2,\ldots,m\}$ are the controllable ports, and the rest of the ports are the ports whose voltages are used in defining the design specifications (a renumbering of the output ports converts the problem to the conventional one considered here). Let the matrix Y_s have a particular form given by (36), in which $\alpha_1,\alpha_2,\ldots,\alpha_m$ are some arbitrary integers (see equation at the top of the page). It is worth mentioning that this type of Y_s corresponds to a lossless network. Impose the constraints

$$\begin{aligned} v_{3k-1} &= v_{\text{in}}, \qquad \forall k \in \{1,2,\ldots,m\} \\ v_{3m+1} &= v_{\text{in}}, \quad v_{3m+2} = -v_{\text{in}} \end{aligned} \tag{37}$$

on the output voltages. The goal is to show that Problem 1 is NP-complete even for the special networks of the form (36) under the aforementioned constraints. Given a natural number $k \in \{1,2,\ldots,m\}$, the conditions in (37) lead to the equations

$$\begin{aligned} i_{3k-2} &= (v_{3k-2} - v_{\text{in}})\mathrm{i} \\ i_{3k-1} &= (-v_{3k-2} + v_{3k})\mathrm{i} \\ i_{3k} &= (-v_{3k} + v_{\text{in}})\mathrm{i}. \end{aligned}$$

Since port $3k-1$ is not a controllable port, it follows from the design specifications in (1) that its current must be zero. In other words, $i_{3k-1} = 0$, or equivalently, $v_{3k-2} = v_{3k}$. On the other hand, the aforementioned equations yield that the switching condition $v_{3k-2}i_{3k-2} = 0$ is tantamount to the relation $v_{3k-2} \in \{0, v_{\text{in}}\}$. Thus, it can be concluded that

$$v_{3k-2} = v_{3k} \in \{0, v_{\text{in}}\}, \qquad \forall k \in \{1,2,\ldots,m\}. \tag{38}$$

Moreover, since ports $3m+1$ and $3m+2$ are not controllable ports, their current must be zero, which gives rise to

$$0 = i_{3m+1} = \sum_{j=1}^{m} \alpha_j v_{3j-2}.$$

Note that the equality $i_{3m+2} = 0$ also leads to the aforementioned constraint. By using (38) and by letting v_{in} be equal to one, the aforementioned equation can be interpreted as follows: given the integers $\alpha_1,\alpha_2,\ldots,\alpha_m$, is it possible to find a subset of these numbers with a zero sum? This problem is referred to as the *subset sum problem* and is known to be NP-complete [26]. This completes the proof. ■

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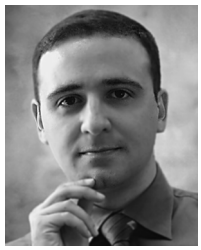

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