A Nonlinear Q-Switching Impedance Technique for Picosecond Pulse Radiation in Silicon

Peiyu Chen, *Student Member, IEEE*, M. Mahdi Assefzadeh, *Student Member, IEEE*, and Aydin Babakhani, *Member, IEEE*

***Abstract*— This paper presents a nonlinear Q-switching impedance (NLQSI) technique for picosecond pulse radiation in silicon. A prototype chip is designed with four NLQSI-based impulse generation channels, which can produce picosecond pulses with a reconfigurable amplitude. An on-chip impulse-coupling scheme combines the outputs from four channels and delivers the combined signal to an on-chip antenna. In addition, an asynchronous optical-sampling measurement system is used to characterize the radiated picosecond pulses in the time domain. The prototype chip can radiate 4-ps pulses with an SNR > 1 bandwidth of 161 GHz. Furthermore, pulse amplitude modulation is experimentally demonstrated. The prototype chip is fabricated in a 130-nm SiGe BiCMOS process technology with a die area of 1 mm^2.**

***Index Terms*— Impulse radiator, nonlinear circuits, optical sampling, picosecond pulse, pulse amplitude modulation, quality factor, SiGe BiCMOS.**

I. Introduction

TRADITIONALLY, signal generation in the millimeter-wave (mm-wave) and terahertz (THz) regimes is performed using continuous-wave (CW) or pulse techniques [1], [2]. As shown in Fig. 1, CW sources produce long pulses in time with a small bandwidth (BW), while pulse sources generate short pulses in time with a large BW. Recently, mm-wave and THz signal have been used in applications, such as high-resolution 3-D imaging [3], [4], biomedical sensing [5], high-speed wireless communication links [6], and broadband spectroscopy [7].

Over the past few decades, photonic techniques have been used for signal generation in mm-wave and THz regimes. These techniques include fsec-laser gated photoconductive antennas (PCAs), photomixing, and quantum cascade lasers [8]–[10]. In photonic-based solutions, laser sources are required, which makes the whole system bulky and expensive. Recently, fully electronic laser-free sources have been reported that produce CW signals in the mm-wave and THz regimes [11]–[18]. These sources are based on high-speed transistors that can achieve f_t (current gain cutoff frequency) of above 300 GHz and $f_{\max}$ (maximum oscillation frequency) exceeding 400 GHz [11], [19]. The majority of the work published on mm-wave and THz sources is based on CW techniques that are narrowband and contain only few frequency tones. Compared with these methods, far less research has been performed to produce broadband picosecond pulses in the mm-wave and THz regimes. It is important to note that the picosecond pulses discussed in this paper should have a large frequency spectrum, above 100 GHz. Pulse-shaping techniques, based on mixing harmonics and nonlinear transmission lines, are beyond this paper's scope [20]–[22].

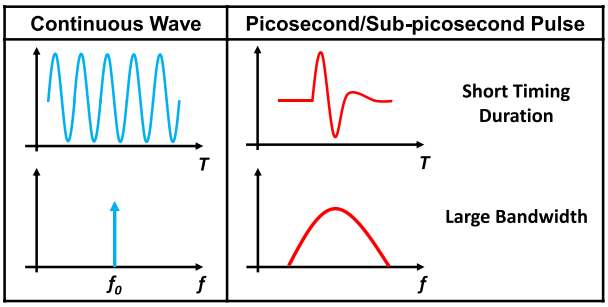

Fig. 1. Comparisons between CW and picosecond/subpicosecond pulse.

In 2014, a silicon-based digital-to-impulse (D2I) architecture was reported that radiated sub-10 ps impulses [23], [24]. This technique was based on switching a dc flowing through a broadband on-chip antenna, which results in converting a stored magnetic energy into a radiated picosecond pulse. In D2I, a pulse-matching circuitry was used to reduce the duration of the radiated pulse. Since then, arrays of D2I radiators have been published in the pursuit of generating short pulses with a large radiated power based on spatial power combining [25], [26].

Apart from the source technology, the accurate detection of picosecond pulses via electronic methods has been a major challenge for the circuits and microwave community. Over the past 20 years, researchers have been using electronic oscilloscopes to perform time-domain characterizations of picosecond pulses that are generated by silicon chips [27]. Unfortunately, the fastest off-the-shelf real-time oscilloscope has a BW of 100 GHz and a rise time of 4.5 ps (Teledyne Lecroy LabMaster 10 Zi-A Oscilloscope), which is not good enough to characterize sub-10 ps pulses [28]. In addition, in these methods, broadband calibrations of antennas/probes, waveguides, coaxial connectors, and coaxial cables are required, which makes the measurement process complicated and time-consuming [27].

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The authors are with the Department of Electrical and Computer Engineering, Rice University, Houston, TX 77005 USA (e-mail: peiyu.chen@rice.edu; assefzadeh@gmail.com; aydin.babakhani@rice.edu).

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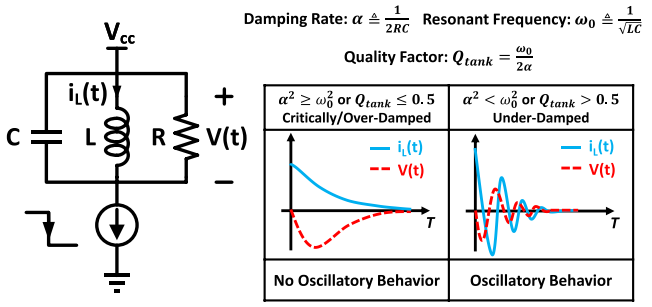

Fig. 2. Step response of a parallel *RLC* tank.

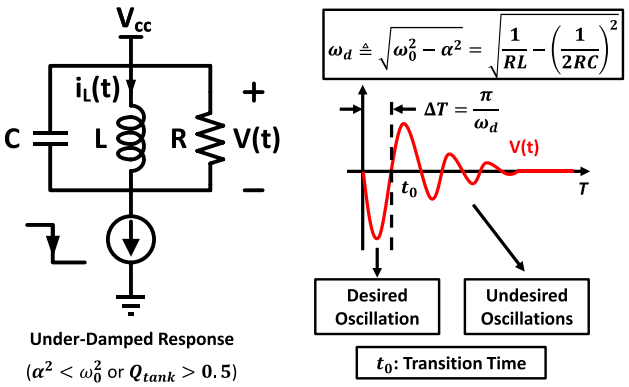

Fig. 3. Underdamped response of a parallel *RLC* tank.

In this paper, a novel circuit based on nonlinear Q-switching impedance (NLQSI) is proposed that produces picosecond pulses with a reconfigurable amplitude. A prototype chip is implemented that contains four NLQSI-based impulse generation channels and an on-chip impulse-coupling scheme, which combines the outputs of the four channels and delivers the combined pulses to an on-chip antenna. The chip is characterized with an asynchronous optical sampling (ASOPS) system that provides a measurement BW up to 4 THz. The time-domain measurements demonstrate that the prototype chip radiates 4 ps pulses with an SNR > 1 BW of 161 GHz. In addition, pulse amplitude modulation is experimentally demonstrated. The prototype chip is fabricated in a 130 nm SiGe BiCMOS process technology and occupies a die area of 1 mm^2.

This paper is an extension of [29] with further simulation analysis and measurement results. The remainder of the text is organized as follows. NLQSI technique is discussed in Section II, while Section III presents the design of the prototype NLQSI-based picosecond pulse radiator chip. The characterization results of the prototype chip are demonstrated in Section IV, including a brief introduction to the ASOPS time-domain measurement system used in this paper for picosecond pulses, as well as the measured NLQSI-induced tunable pulse amplitudes and measured pulse amplitude modulation. Conclusions are offered in Section V.

II. Nonlinear Q-Switching Impedance Technique

The idea of NLQSI originates from the step responses of a parallel *RLC* tank. In order to understand its mechanism, in this section, the step response of a parallel *RLC* tank is briefly reviewed and then the method of NLQSI is introduced.

A. Step Response of a Parallel RLC Tank

A parallel *RLC* tank, as shown in Fig. 2, has two types of step responses: overdamped/critically damped response and underdamped response.[1] The response of the tank depends on its damping rate and resonant frequency, which are defined as follows:

$$\alpha \triangleq \frac{1}{2RC} \tag{1}$$

$$\omega_0 \triangleq \frac{1}{\sqrt{LC}} \tag{2}$$

[1]A loss-less response is excluded from this discussion.

where R, L, and C are the resistance, inductance, and capacitance of the tank. Equivalently, the step response of a parallel *RLC* tank can also be determined by investigating the quality factor of the tank (Q_{tank}), which represents the ratio of the stored energy to the energy dissipated in a circuit. Q_{tank} can be expressed as follows:

$$Q_{\text{tank}} \triangleq 2\pi \frac{\text{maximum energy stored}}{\text{total energy lost per cycle at resonance}} = \frac{\omega_0}{2\alpha} = R\sqrt{\frac{C}{L}}. \tag{3}$$

To simplify the analysis, the current source is considered to have an ideal step response.

1) Underdamped Response ($\alpha^2 < \omega_0^2$ or $Q_{tank} > 0.5$): When the damping rate α is smaller than the resonant frequency ω_0, equivalently, Q_{tank} is larger than 0.5, the tank displays underdamped responses. In this case, the voltage across the tank, $V(t)$, and the current flowing through the inductor L, $I_L(t)$, both have exponentially decaying oscillatory behaviors. Analytical expressions of $V(t)$ and $I_L(t)$ can be obtained by solving the following differential equation:

$$LCI_L'' + \frac{L}{R}I_L' + I_L = 0 \tag{4}$$

with initial conditions of

$$I_L(0) = I_0 \tag{5}$$

$$V(0) = LI_L'(0) = 0 \tag{6}$$

where I_0 is the steady-state current flowing through the tank before switching off.

The underdamped response of the parallel *RLC* tank can be expressed as

$$I_L(t) = I_0 e^{-\alpha t}\frac{\omega_0}{\omega_d}cos\left(\omega_d t - \tan^{-1}\frac{\alpha}{\omega_d}\right) \tag{7}$$

$$V(t) = -LI_0 e^{-\alpha t}\frac{\omega_0^2}{\omega_d}\sin(\omega_d t) \tag{8}$$

where ω_d is the oscillation frequency, defined as

$$\omega_d \triangleq \sqrt{\omega_0^2 - \alpha^2}. \tag{9}$$

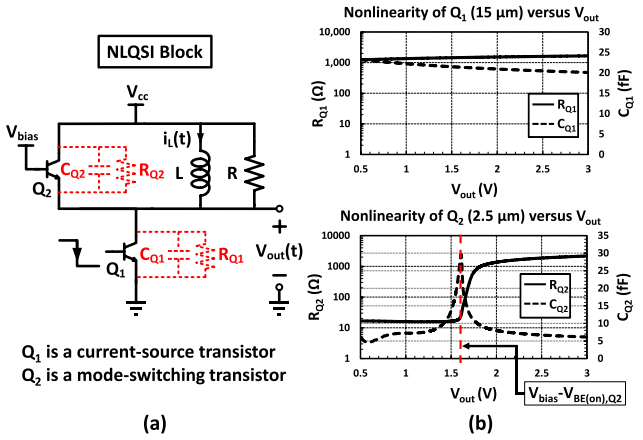

Fig. 4. (a) NLQSI block. (b) Nonlinearity of transistors Q_1 and Q_2 versus V_{out} when V_{cc} is 1.3 V and V_{bias} is 2.5 V.

Therefore, the oscillation period is $T_d = 2\pi/\omega_d = 2\pi/\sqrt{(\omega_0^2 - \alpha^2)}$. From (8) and (9), we can make an observation that the oscillation frequency increases by reducing the damping rate, which extends the timing duration of the decay.

2) Overdamped/Critically Damped Response ($\alpha^2 \geq \omega_0^2$ or $Q_{\text{tank}} \leq 0.5$): When the damping rate α is larger than or equal to the resonant frequency ω_0, equivalently, Q_{tank} is smaller than or equals 0.5, the tank presents overdamped or critically damped responses. The current flowing through the inductor L, $I_L(t)$, decays to zero exponentially but does not produce a large voltage response $V(t)$ across the tank. In this case, there is no oscillatory behavior in either the current or voltage responses.

B. Switching From Underdamped to Overdamped to Produce Short Pulses

To produce a large voltage response in a short time with minimal ringing, a parallel *RLC* tank is designed such that it can switch from an underdamped response to an overdamped response by switching the load resistance of the parallel tank, equivalently, switching the quality factor of the tank (Q_{tank}). In this case, when the falling edge of the excitation current is arrived, the tank behaves in an underdamped response, producing a half-cycle oscillation, which is the desired oscillation shown in Fig. 3. The duration of the first half-cycle is $\Delta T = (1/2)T_d = \pi/\sqrt{(\omega_0^2 - \alpha^2)}$, which can be as short as several picoseconds, according to simulations. The ringing, "Undesired Oscillations," also shown in Fig. 3, needs to be eliminated by forcing the tank to switch to and stay in an overdamped response by reducing the load resistance R such that $\alpha^2 > \omega_0^2$. In this switching event, Q_{tank} is decreased from Q_U that sustains an underdamped response to Q_O that supports an overdamped response. Therefore, there exists a Q-switching event around the transition time t_0, which is shown in Fig. 3.

C. NLQSI Block

1) Overview: Fig. 4(a) shows the reported NLQSI block for picosecond pulse generations. A bipolar transistor Q_1 acts as a current source. When the base node of the transistor Q_1 is applied to 0 V by a voltage falling edge, the parallel tank starts to behave the step responses. A bipolar transistor Q_2 monitors the output voltage $V_{\text{out}}(t)$ and autonomously changes the quality factor of the parallel *RLC* tank (Q_{tank}). Parasitic capacitance and resistance of transistors Q_1 and Q_2 play an important role in the performance of this NLQSI block. During the step responses, transistors Q_1 and Q_2 can be simplified by a parallel combination of R_{Q1} and C_{Q1} and that of R_{Q2} and C_{Q2}, respectively, as shown in Fig. 4(a). The proposed NLQSI block is nonlinear because these parasitic elements, especially R_{Q2} and C_{Q2}, vary significantly depending on the output voltage $V_{\text{out}}(t)$. Fig. 4(b) demonstrates the nonlinearity of these parasitic elements when V_{out} is swept from 0.5 to 3 V, V_{cc} is 1.3 V, and V_{bias} is 2.5 V. The values of V_{cc} and V_{bias} are chosen for the proper operation of NLQSI blocks, which will be discussed later. During the step responses, transistor Q_1 is OFF because its base node is set to 0 V. Therefore, transistor Q_1 has a little nonlinearity with V_{out}. However, transistor Q_2 turns OFF when V_{out} is larger than $V_{\text{bias}} - V_{\text{BE(ON)},Q2}$, which leads to the fact that transistor Q_2 dominantly contributes the nonlinearity of the NLQSI block and, therefore, transistor Q_2 is crucial in shaping the generated ultrashort pulses.

2) Q-Switching Mechanism: The Q-switching mechanism of the NLQSI block is as follows [Fig. 5(a)]: in the steady state, a dc flows through the inductor L and V_{out} equals V_{cc}. The tank is designed to have an overdamped response by biasing the transistor Q_2 to be ON. Stage I: When the current falling edge arrives, the tank behaves in an overdamped response, increasing V_{out}, and consequently, transistor Q_2 is turned OFF and Q_{tank} is increased so that it is larger than 0.5. Therefore, the first Q-switching event is triggered at the transition time t_1, and the tank behaves in an underdamped regime ($Q_{\text{tank}} > 0.5$). Stage II: In the underdamped response, the "desired oscillation" is generated until V_{out} drops below a certain value, which is when transistor Q_2 turns ON. The small ON resistance of transistor Q_2 (R_{Q2}) reduces Q_{tank}. Q_{tank} should be decreased enough to force the tank to switch to an overdamped response ($Q_{\text{tank}} < 0.5$). Therefore, the second Q-switching event happens at the transition time t_2. Stage III: The tank stays in the overdamped response, and V_{out} decays exponentially to V_{cc}, resulting in eliminating the undesired ringing. Eventually, the tank returns back to the steady state, where V_{out} stays at V_{cc}. The time-domain evolution of $Q_{\text{tank}}(t)$ is illustrated in Fig. 5(b). It will be shown later that the shape of the generated pulse is dependent on $Q_{\text{tank}}(t)$, which is affected by the bias voltage of transistor Q_2 (V_{bias}), emitter lengths of both the transistors Q_1 and Q_2, and the inductance of L.

3) Effects of V_{bias} of Transistor Q_2: V_{bias} of transistor Q_2 has significant effects on the performance of the NLQSI block. Fig. 6 shows the simulation results when V_{bias} is swept from 1.5 to 2.5 V. In this simulation, the emitter lengths of transistors Q_1 and Q_2 are 15 and 2.5 μm, respectively. $V_{\text{BE(ON)}}$ of transistor Q_2, $V_{\text{BE(ON)},Q2}$ is around 0.9 V. V_{cc} is 1.3 V.

As shown in Fig. 6(a), when V_{bias} remains below 2.1 V, which is smaller than the sum of V_{cc} and $V_{\text{BE(ON)},Q2}$, undesired

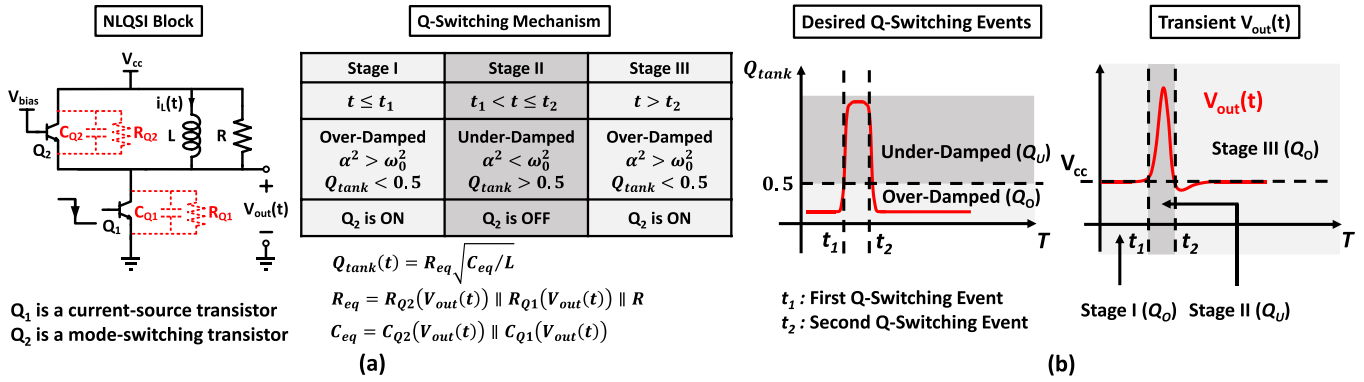

Fig. 5. (a) Summary of the Q-switching mechanism of the proposed NLQSI block. (b) Time-domain evolutions of Q_{tank} and V_{out} of the NLQSI block. Q_O is the quality factor that sustains the overdamped response. Q_U is the quality factor that sustains the underdamped response.

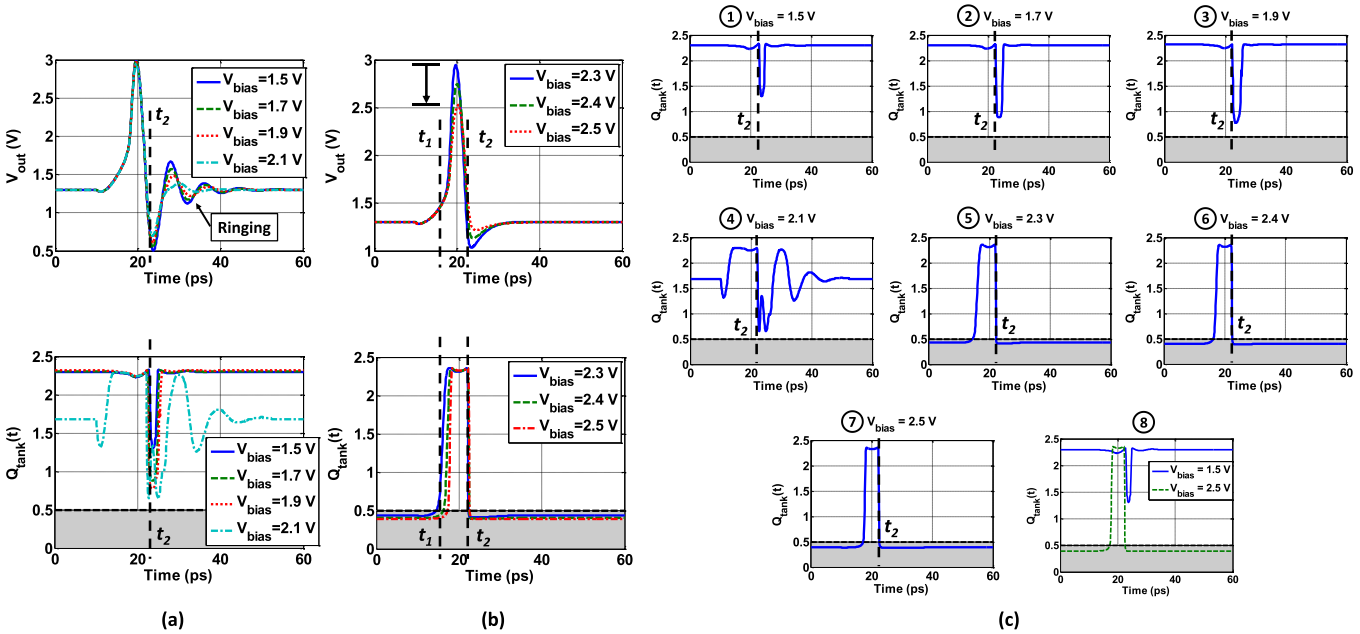

Fig. 6. Simulated effects of V_{bias} on the performance of NLQSI block. (a) Incorrect Q-switching mechanism. (b) Designed Q-switching mechanism. (c) 1–7: Simulated $Q_{\text{tank}}(t)$ in each V_{bias} condition and 8: comparison between the incorrect Q-switching mechanism and the designed Q-switching mechanism.

oscillations do not disappear after the transition time t_2. This is because transistor Q_2 turns OFF again and the tank stays in the underdamped condition, which is validated by studying the simulated time-domain evolution of $Q_{\text{tank}}(t)$, as shown in Fig. 6(c) (1–3). For the situations where V_{bias} is smaller than 2.1 V, Q_{tank} is always larger than 0.5, meaning that the tank stays in an underdamped response with a time-varying damping rate. At around the transition time t_2, Q_{tank} is reduced along with the decreasing V_{out}, but afterward it returns to a high level that sustains the ringing (undesired oscillations). Another observation from the simulation is that the amplitudes of the ringing decrease with increasing V_{bias}. This is due to the fact that, with increasing V_{bias}, the tank has a smaller Q_{tank}, equivalently a larger damping rate α, for a longer period of time, as shown in Fig. 6(c) (1–3). The amplitude of the ringing depends on the minimum value that Q_{tank} can reach after the transition time t_2. In all these cases, transistor Q_2 adds a very large OFF resistance to the *RLC* tank, and consequently, the tank has an almost identical Q_{tank} before the transition time t_2, which explains why the peak amplitudes remain almost constant. In summary, in situations where V_{bias} is smaller than the sum of V_{cc} and $V_{\text{BE(ON)},Q2}$, the underdamped response dominates the entire transient response.

When V_{bias} is larger than the sum of V_{cc} and $V_{\text{BE(ON)},Q2}$, for example, V_{bias} is in the range from 2.3 to 2.5 V, transistor Q_2 turns ON as long as V_{out} is smaller than or equals V_{cc}. Therefore, transistor Q_2 keeps turning ON after the transition time t_2 and forces the tank to remain in the over-damped condition, eliminating undesired ringing, as shown in Fig. 6(b). The simulated $Q_{\text{tank}}(t)$ also reflects that the designed Q-switching mechanism is achieved when V_{bias} is larger than $V_{\text{cc}} + V_{\text{BE(ON)},Q2}$ [Fig. 6(b) and (c) (5–7)]. In these situations, transistor Q_2 turns ON completely in the steady state and Q_{tank} is smaller than 0.5. When the current falling edge

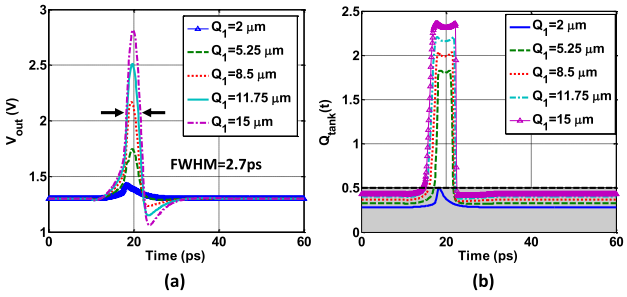

Fig. 7. Simulated effects of the emitter length of transistor Q_1 on the performance of NLQSI block. (a) Simulated time-domain waveform of the generated pulse. (b) Simulated $Q_{\text{tank}}(t)$.

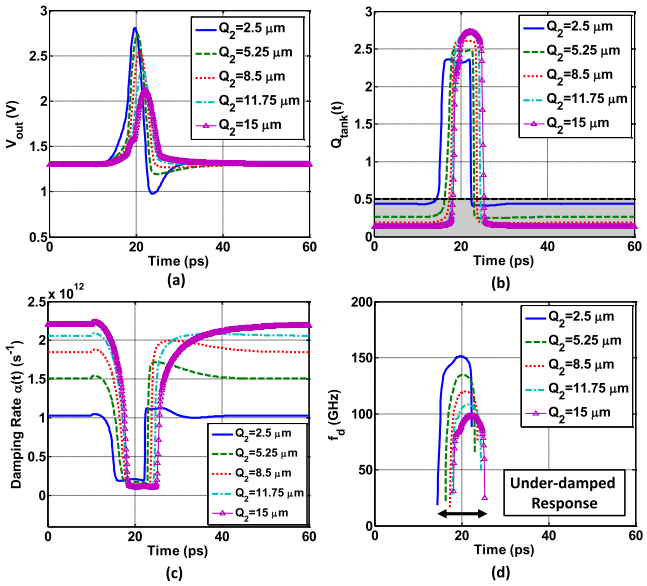

Fig. 8. Simulated effects of the emitter length of transistor Q_2 on the performance of NLQSI block. (a) Simulated time-domain waveform of the generated pulse. (b) Simulated $Q_{\text{tank}}(t)$. (c) Simulated damping rate $\alpha(t)$. (d) Simulated $f_d(t) = (1/2\pi)\sqrt{(\omega_0^2 - \alpha^2)}$.

arrives, the tank is in the overdamped response (Stage I), where V_{out} increases and turns OFF Q_2, boosting Q_{tank} to be larger than 0.5. The tank enters Stage II and has an underdamped response until around the transition time t_2, where V_{out} is smaller than $V_{\text{bias}} - V_{\text{BE(ON)},Q2}$ and transistor Q_2 is turned ON again. At this moment, Q_{tank} becomes smaller than 0.5, and the tank performs an overdamped response, switching from Stages II to III. Unlike the previously discussed cases ($V_{\text{bias}} < 2.1$ V), after the transition time t_2, Q_{tank} is always smaller than 0.5 and, therefore, the tank stays in the overdamped response (Stage III), completely eliminating the ringing. Therefore, a clean pulse is generated, compared with the previously discussed cases. With increasing V_{bias}, the first Q-switching event happens later and the tank stays in the overdamped response (stage I) for a longer period of time, causing more energy loss and therefore, reducing the peak amplitude of the generated pulse. The comparison between the $Q_{\text{tank}}(t)$ in these two cases ($V_{\text{bias}} = 1.5$ and 2.5 V) is plotted in Fig. 6(c) (8).

When V_{bias} is 2.1 V, as shown in Fig. 6(c) (4), the simulated $Q_{\text{tank}}(t)$ clearly reflects that this bias condition is in the transition to the proper Q-switching mechanism. In sum, when V_{bias} is larger than the sum of V_{cc} and $V_{\text{BE(ON)},Q2}$, transistor Q_2 is completely ON in the steady state, and the NLQSI block has a desired Q-switching mechanism to generate a clean picosecond pulse with tunable peak amplitude.

4) Choose Emitter Lengths of Transistors Q_1 and Q_2: The emitter lengths of transistors Q_1 and Q_2 have crucial effects on the performance of the NLQSI block. Under the proper bias condition ($V_{\text{bias}} = 2.3$ V), if the emitter length of transistor Q_1, $l_{e,Q1}$, is increased, the steady-state current flowing through the *RLC* tank is increased as well. Fig. 7(a) shows the simulation results where $l_{e,Q1}$ is swept from 2 to 15 μm. A step voltage is applied to the base of transistor Q_1 to mimic an ideal predriver stage. As expected, a larger transistor Q_1 generates a pulse with a greater peak voltage but the duration of the pulse becomes larger as well. In this simulation, by choosing a length of 15 μm for transistor Q_1, the full-width-at-half-maximum (FWHM) of the generated pulse becomes 2.7 ps. Fig. 7(b) demonstrates the simulated $Q_{\text{tank}}(t)$ with different $l_{e,Q1}$. Except for the case where $l_{e,Q1}$ is 2 μm, the NLQSI block has the proper Q-switching mechanism. With a larger transistor Q_1, the tank is in the underdamped response (Stage II) for a longer period of time, causing the duration of the pulse to be larger. In addition, when $l_{e,Q1}$ is increased, the tank switches from Stage I (overdamped response) to Stage II (underdamped response) earlier, causing less energy loss, and meanwhile, stronger energy $[E = (1/2)LI^2]$ is initially stored in the tank. As a result, the peak amplitude of the generated pulse is increased with $l_{e,Q1}$. In practice, a larger transistor Q_1 slows down the switching speed due to its large base capacitance, but this issue can be mitigated by designing a proper predriver stage with strong current-discharging capability. In this paper, transistor Q_1 is designed to have an emitter length of 15 μm, which is chosen as a compromise between the pulsewidth (FWHM) and the pulse amplitude.

For transistor Q_2, when its emitter length $l_{e,Q2}$ is increased, transistor Q_2 adds more parasitic capacitance and less parasitic resistance to the tank. Fig. 8 shows the simulated effects of $l_{e,Q2}$ on the performance of NLQSI block. With a larger transistor Q_2, the NLQSI block generates a wider pulse with a smaller peak amplitude, as shown in Fig. 8(a). Fig. 8(b) demonstrates that, with $V_{\text{bias}} = 2.3$ V, the NLQSI blocks with $l_{e,Q2}$ ranging from 2.5 to 15 μm, all have the designed Q-switching mechanism. Furthermore, a larger transistor Q_2 produces a larger Q_{tank} in Stage I (overdamped response) and a smaller Q_{tank} in Stage II (underdamped response). The relationship between the pulse peak amplitude and $l_{e,Q2}$ can be explained as follows. First, Fig. 8(c) shows that a larger transistor Q_2 causes more energy loss during the pulse generation period (Stages I and II). Second, with a larger transistor Q_2 turning ON in the steady state, less dc flows through the inductor L, and consequently, less initial energy $[E = (1/2)LI^2]$ is stored in the tank. As a result, these two effects cause that the peak and dip amplitudes of the generated pulse are decreased with a larger transistor Q_2.

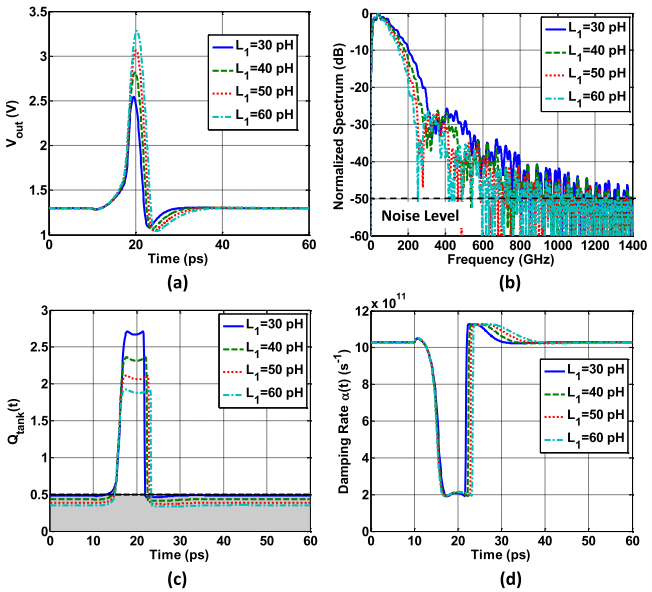

Fig. 9. Simulated effects of the inductance L on the performance of NLQSI block. (a) Simulated time-domain waveform of the generated pulse. (b) Simulated SNR > 1 BW of the generated pulse. (c) Simulated $Q_{\text{tank}}(t)$. (d) Simulated damping rate $\alpha(t)$.

Fig. 8(d) demonstrates that the simulated oscillation frequency $f_d = (1/2\pi)\sqrt{(\omega_0^2 - \alpha^2)}$ in the underdamped response (Stage II) is decreased with $l_{e,Q2}$, which explains the observation in Fig. 8(a) that the pulsewidth of the generated pulse is increased with $l_{e,Q2}$. In this paper, transistor Q_2 is designed to have an emitter length of 2.5 μm to enable Q-switching without degrading the pulse amplitude.

5) Inductance L: According to (8) and (9), the peak amplitude and the pulsewidth of the generated pulse are dependent on the inductance of L. Fig. 9 demonstrates the simulated effects of sweeping L from 30 to 60 pH with the proper bias condition of $V_{\text{bias}} = 2.3$ V. As expected, with the increasing L, the generated pulse has a larger peak amplitude but also a greater pulsewidth [Fig. 9(a)]. The effects of the inductor L can also be investigated in the viewpoint of $Q_{\text{tank}}(t)$. With the proper bias condition, the NLQSI blocks have the desired Q-switching mechanism. According to (1) and (3), a larger inductor L reduces Q_{tank} without changing the damping rate α. Fig. 9(c) and (d) validates this point and shows that a larger inductor L tends to provide the tank with a longer underdamped response (Stage II), which produces less energy loss in the pulse generation period. In addition, a larger inductor L stores more initial energy ($E = (1/2)LI^2$) in the steady state, and consequently, the peak and dip amplitudes of the generated pulse are increased with a larger inductor L. Equation (2) also indicates that, with a larger inductor L, the resonant frequency ω_0 of the tank is reduced. Because the damping rate α is independent of the inductance of L, according to (9), the oscillation frequency in the underdamped response is decreased with L, resulting in the increased pulsewidth.

The design strategy here is to maximize the SNR > 1 BW, because a broad detectable BW is crucial for spectroscopy and imaging applications. As shown in Fig. 9(b), the NLQSI block with a smaller inductor L produces picosecond pulses with a larger SNR > 1 BW. However, the actual measured SNR > 1 BW is also dependent on the sensitivity of the detector. If the peak amplitude of the generated pulse is very weak, the measured SNR > 1 BW will be smaller than the theoretical (simulated) value. Furthermore, practically, an inductor smaller than 35 pH is difficult to be implemented in the process used in this paper, because the parasitic effects of the neighboring routings are significant. Therefore, based on the above considerations, in this paper, the inductance of L is set at 40 pH.

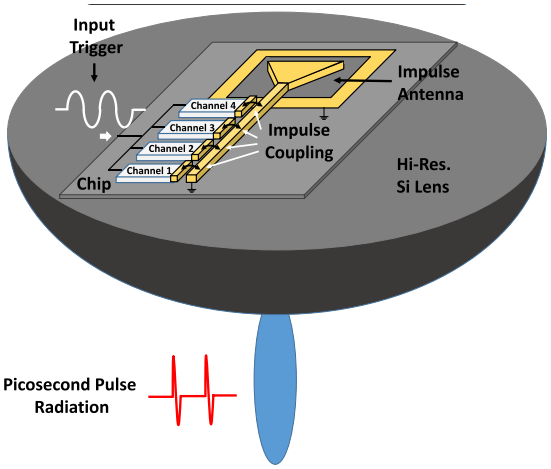

Fig. 10. System architecture of the radiating chip.

III. Circuit and Antenna Details

The NLQSI technique reported in this paper is implemented in a 130-nm SiGe BiCMOS process technology. In this section, first, an overview of the system architecture is presented. Second, an impulse-coupling scheme is introduced to resolve the issues caused by the transmission line effects in the NLQSI circuit. Third, the design details of the individual impulse generation channel and the four-way impulse combiner are presented. In addition, bias routings in the NLQSI blocks are specially designed. Finally, the design of the broadband on-chip antenna is discussed.

A. System Architecture

Fig. 10 shows the architecture of the radiating chip, which consists of four impulse generation channels. A trigger signal is fed to the chip and distributed to these channels through an H-tree distribution network. Each channel converts the input trigger into a picosecond pulse train with a repetition rate the same as the trigger. An impulse-coupling scheme is introduced to resolve the issues induced by the transmission line effects in implementing NLQSI blocks. Based on this scheme, a four-way microstrip-based impulse combiner is designed to combine the generated picosecond pulses from the four channels and feed the on-chip antenna. The four-way impulse combiner also enables pulse amplitude modulation by controlling the individual impulse generation channels. A highly resistive silicon lens is attached to the backside of

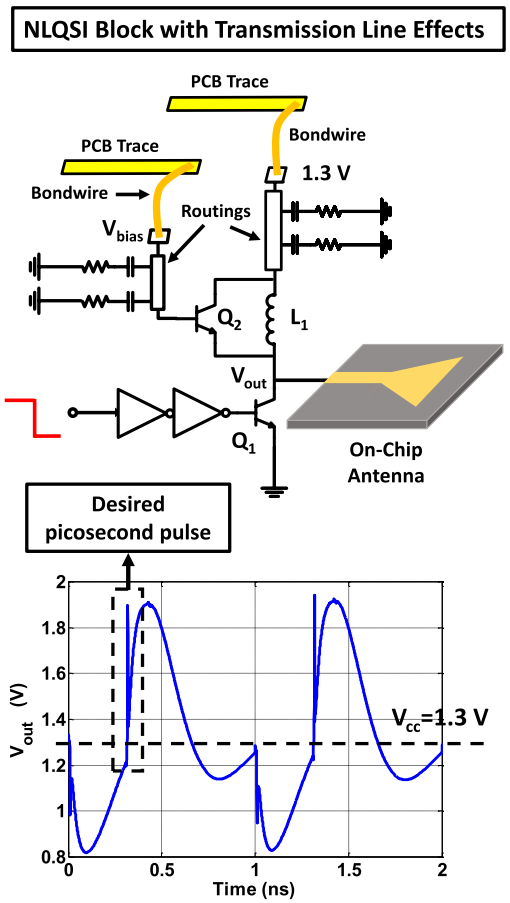

Fig. 11. NLQSI block with transmission line effects.

the radiator chip in order to increase the radiation efficiency and directivity of the on-chip antenna.

B. Impulse-Coupling Scheme

1) Transmission Line Effects in Implementing NLQSI Blocks: The chip uses on-chip metal routings, wirebonds, and PCB traces for biasing and power supply, as shown in Fig. 11. The transmission line effects of these wirings need to be carefully considered in the transient analysis. For stability purposes, De-Qing blocks, consisting of a capacitor and a resistor in series, are placed along the on-chip metal routings. As the supply current varies in a short period of time, the inductance of the metal routings adds a strong low-frequency ringing to the picosecond pulse at $V_{\text{out}}(t)$ (Fig. 11). Although the on-chip antenna is optimized for high-frequency radiation, the strong low-frequency ringing will be still radiated, which may cause interference with other low-frequency channels. Therefore, it is important to eliminate the low-frequency ringing before feeding the impulse to the antenna.

2) Impulse-Coupling Block: In this paper, an impulse-coupling block is introduced to isolate the input of the on-chip antenna from the strong low-frequency ringing caused by the transmission line effects of the supply wirings. Fig. 12(a) shows the NLQSI circuit with the impulse-coupling block, which is based on microstrip inductive coupling, consisting of two adjacent 50 μm long metal lines fabricated on the top metal layer AM, as shown in Fig. 12(b). Inductor L_1 is implemented by a metal line with a width of 4 μm, while inductor L_2 is implemented by another line with a width of 5 μm. The metal layer M3 is used as a ground plane. In order to increase the mutual coupling between the two metal lines, the spacing between them is set to 2.8 μm, which is the minimum value allowed by the DRC rules for the process technology.

A simplified equivalent circuit of the designed inductive coupler is shown in Fig. 12(c). The inductive mutual coupling dominates the coupling mechanism, as the parasitic capacitors between L_1 and L_2 are very small (less than 2 fF). The parasitic capacitors associated with the ground plane are omitted here. EM simulations show that the designed inductive coupler has a broadband performance. As shown in Fig. 12(c), L_1, L_2, and the inductive mutual coupling coefficient k are flat from 10 to 200 GHz. At 100 GHz, L_1 is 40 pH, L_2 is 37 pH, and k is 0.45.[2]

To perform impulse coupling in the NLQSI circuit, the inductive coupler is set to the following configuration: the collector node of transistor Q_1 is connected to Port 1, Port 2 connects with the V_{cc} of 1.3 V, the connection of Port 3 is changeable, which will be discussed later, and Port 4 connects with the load. The inductive mutual coupling and the small parasitic capacitors between L_1 and L_2 filter out the low-frequency ringing in the forward-coupling direction, which is from Ports 1 to 4. Fig. 12(d) shows the simulated output voltage of the NLQSI block with the introduced impulse-coupling block when Port 3 is grounded. At the antenna input node, the low-frequency ringing is filtered out and a clean impulse-like waveform is fed to the on-chip antenna. Compared with the generated impulse without the impulse-coupling scheme, as shown in Fig. 11, the peak amplitude of the coupled pulse at Port 4 is reduced by around 50% as expected. In addition, there are very few distortion effects induced by this impulse coupler. The small downward pulses at 0 and 1 ns, shown in Fig. 12(d), are produced by the rising edges of the converted 1 GHz square wave, which switch ON transistor Q_1. These "parasitic" pulses can be eliminated by turning ON the transistor Q_1 using a waveform with a slow rising edge, which, however, may limit the repetition rate of the generated pulse train.

C. Impulse Generation Channel

The schematic of an impulse generation channel is shown in Fig. 13(a). The input trigger is fed into a digital inverter chain through a one-to-four H-Tree distribution network. The input impedance of the digital inverter chain is designed to be 200 Ω, in order to reduce the reflections. The digital inverter chain converts the input sinusoidal trigger into a square wave, which switches transistor Q_1 in the NLQSI block. In order to switch off transistor Q_1 quickly, an 18 μm bipolar transistor Q_3 is added to provide an additional discharging path from the base node of transistor Q_1. The maximum trigger frequency is 1 GHz, which is limited by the BW of the digital inverter chain. V_{digital} of each impulse generation

[2]The coupling coefficient k is optimized to be broadband, which sacrifices the coupling strength as a cost.

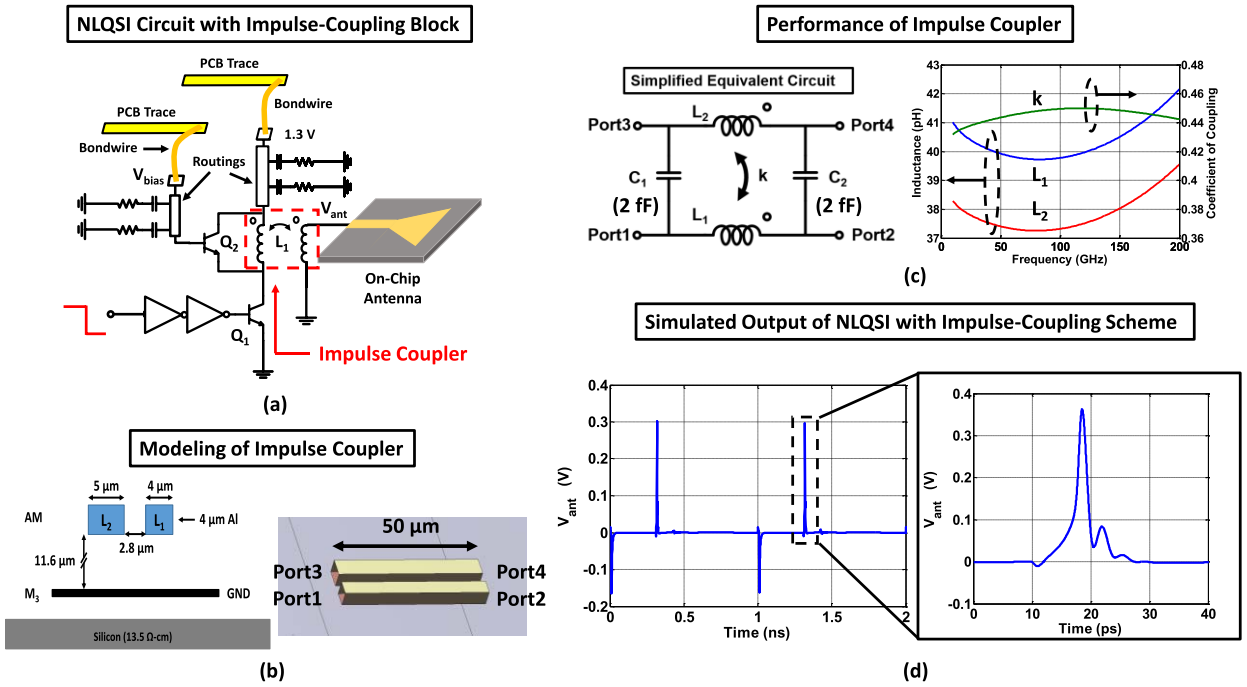

Fig. 12. (a) NLQSI circuit with impulse-coupling block. (b) Modeling of impulse coupler. (c) Performance of impulse coupler. (d) Simulated output of the NLQSI circuit with the impulse-coupling scheme.

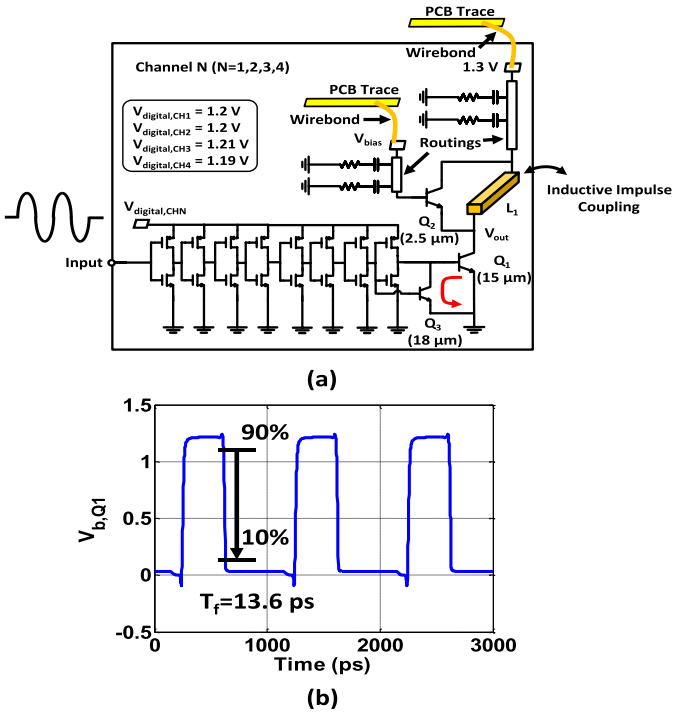

Fig. 13. (a) Schematic of an individual impulse generation channel. (b) Simulated transient voltage at the base node of transistor Q_1.

channel needs to be optimized, which will be discussed later. Fig. 13(b) shows the simulated transient waveform applied to the base node of transistor Q_1, which has a falling time of 13.6 ps.

D. Four-Way Impulse Combiner

The four-way impulse combiner designed in this paper consists of four impulse couplers stacked in series, as shown

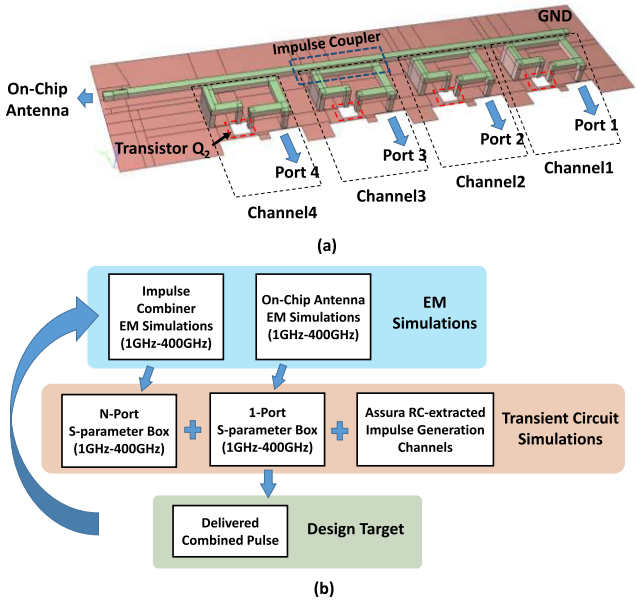

Fig. 14. (a) Impulse combiner. (b) Design methodology of the impulse combiner.

in Fig. 14(a). The spacing between the neighboring channels is identical. The second winding of the combiner connects with the on-chip antenna at one end and is grounded at the other. The collector nodes of transistor Q_1 in the four channels are connected to Ports 1–4, respectively. The routings in the NLQSI block in each channel are included in the EM simulations of the impulse combiner.

Fig. 14(b) illustrates the design methodology of the impulse combiner: the impulse combiner structure, with routings in the NLQSI blocks, is first simulated in a method of moments-based EM simulator (Mentor Graphics HyperLynx

Full-Wave Solver) in a wide frequency range from 1 to 400 GHz. The extracted S-parameters are then imported into Cadence Virtuoso as an N-port S-parameter box, which is connected with Assura-RC-extracted circuits of the impulse generation channels and an S-parameter box of the on-chip antenna. To investigate the performance of the designed impulse combiner, transient simulations are performed in Cadence Virtuoso to examine the combined pulse delivered to the on-chip antenna.

By switching on only one impulse generation channel at a time, the transient voltage at the antenna input is simulated and shown in Fig. 15(a). Compared with the simulation result shown in Fig. 12(d), the ringing effect in the coupled pulse is increased a little, which is mainly caused by the different port connection configuration from that in Fig. 12(a), equivalently, the different load impedance seen by the NLQSI block. The coupled pulses from Channels 1 and 2 are almost identical and their arrival times to the antenna's input port are equal. However, the pulses from Channels 3 and 4 have smaller peak amplitudes and arrive in different times at the antenna node. This is because the impulse combiner is not fully electromagnetically symmetrical among all the four channels. Channels 1 and 2 see a similar load impedance from the impulse combiner. The value of this impedance varies slightly for Channels 3 and 4.[3] Timing mismatch is more detrimental to the performance of the pulse combiner than the mismatch in the peak amplitudes because it will distort the pulse shape of the combined signal. In this design, the timing mismatch can be compensated by tuning the propagation delay of the trigger in each channel with varying the supply voltage V_{digital} of the digital inverter chain in each channel. The optimized V_{digital} values are: $V_{\text{digital,CH1}}$ is 1.2 V, $V_{\text{digital,CH2}}$ is 1.2 V, $V_{\text{digital,CH3}}$ is 1.21 V, and $V_{\text{digital,CH4}}$ is 1.19 V. Fig. 15(b) presents the aligned coupled pulses after adjusting the supply voltages of the digital inverter chains. The differences in their arrival timings are within 0.5 ps. With different ON–OFF combinations of the four channels, the combined pulse can have 16 peak amplitudes, which can be used for pulse amplitude modulation purposes.[4] The simulated peak amplitudes in these 16 combinations are shown in Fig. 16.

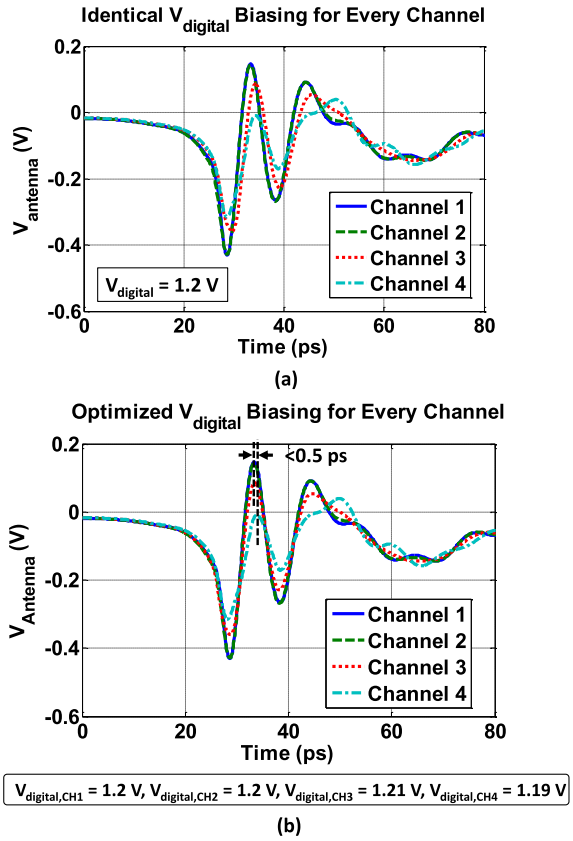

Fig. 15. Simulated coupled pulses from four channels with (a) identical V_{digital} biasing and (b) optimized V_{digital} biasing.

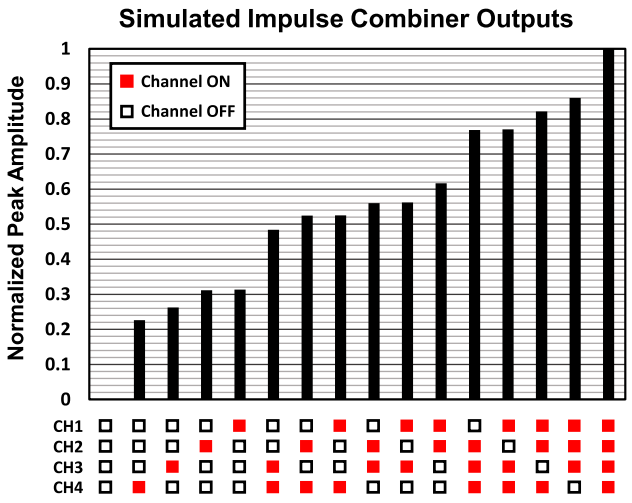

Fig. 16. Simulated pulse peak amplitudes of impulse combiner outputs in all 16 combinations.

E. Bias Routings in the NLQSI Block

Thin and long on-chip bias routings have significant parasitic effects in high frequency. These effects cause the bias nodes of circuit blocks to be no longer an ideal ground. To mitigate this problem, in this paper, two wide metal planes on M1 and M2 layers are used as V_{bias} and V_{cc} planes, respectively, which are placed directly beneath the ground plane (M3) of the impulse combiner, as shown in Fig. 17(a). The advantages of this design are as follows.

1) Self-inductance of a large metal plane is much smaller than that of a long and thin metal line.

2) Large distributed capacitance is formed between these layers and the ground plane. As a result, the two wide metal planes with the ground plane can be considered as two transmission lines with a small Z_0 ($\sqrt{L/C}$). With a modest length, the designed bias routing planes present a broadband low impedance at the bias nodes. Fig. 17(b) shows the impedance of the bias routings

[3]Even though channel 4 is closer to the antenna node than channel 3, with identical V_{digital}, the timing of the peak of the generated pulse from channel 4 can still be a little later than that of channel 3 because the generated pulses from these two channels have different pulse shapes.

[4]Pulse amplitude modulation is useful in high speed wireless communication link based on interleaving picosecond pulses with modulated peak amplitudes.

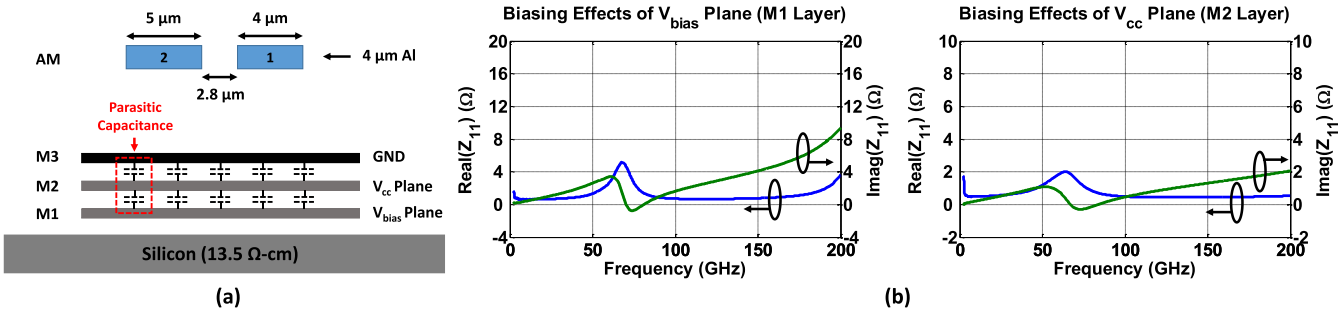

Fig. 17. (a) Biasing planes for V_{cc} and V_{bias} in NLQSI blocks. (b) Simulated impedance of the bias routings at V_{cc} and V_{bias} nodes in NLQSI blocks.

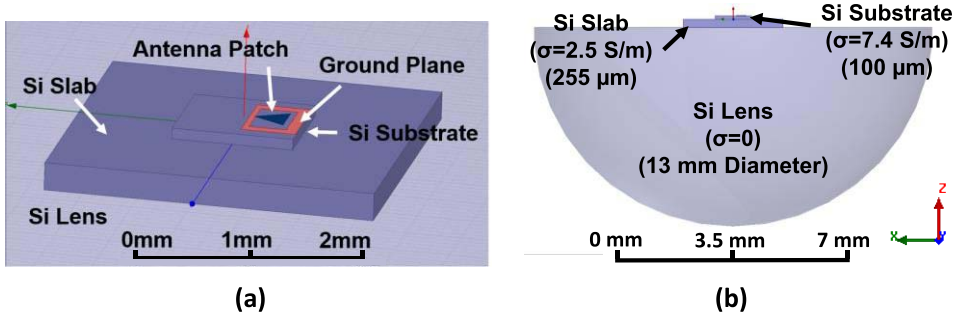

Fig. 18. Structure of the on-chip antenna used in the simulation. (a) Zoom-in view of the on-chip antenna. (b) Whole view of the EM simulation structure showing the attached silicon lens.

at the V_{cc} and V_{bias} nodes of NLQSI blocks from 1 to 200 GHz.

3) The ground plane on M3 isolates the impulse combiner from the bias routings, eliminating the undesired mutual couplings.

F. On-Chip Antenna

In this paper, a single triangular metal sheet on the top metal layer (AM), with a slot on the ground plane (M3) is designed to couple the radiation to the silicon substrate. The triangular shape is used to support broadband radiation [30]. For assembly purposes, a silicon slab is placed between the silicon chip and the silicon lens, as shown in Fig. 18(a). All these components are included in the EM simulations during the design phase; the geometric details are noted in Fig. 18(b). An FEM-based 3-D EM simulator, HFSS v13, is used to simulate the antenna in the frequency domain. The on-chip antenna has a relatively flat input impedance from 50 to 200 GHz [Fig. 19(a)]. The simulated radiation efficiency is shown in Fig. 19(b). It will be shown later that the measured radiated picosecond pulses have a peak frequency component around 54 GHz. At this peak frequency, the designed antenna has a 19% simulated radiation efficiency and a 16 dBi simulated peak directivity. The designed antenna has greater radiation efficiencies at higher frequencies, which compensates for the weak high-frequency components of the generated picosecond pulses. Simulated 2-D and 3-D radiation gain patterns at 54 GHz are presented in Fig. 19(c). The main lobe in the E-plane pattern is tilted, because the on-chip antenna is not symmetrical in the E-plane. A finite-difference time domain-based 3-D EM simulator, CST Microwave Studio 2015, is used to simulate the time-domain E-field waveforms of the radiated picosecond pulses. An ideal far-field E-field probe is used in the simulation to capture the radiated pulse waveform. As shown in Fig. 20, at the straight angle ($\theta = 180°$), the radiated waveform has a FWHM of 3.6 ps when V_{bias} is 2.3 V. The peak amplitude of the radiated pulse is reduced by 38% when V_{bias} is increased to 2.5 V. Compared with the simulated excitation signal at the antenna's input node, shown in Fig. 15, the additional ringing in the radiated pulse waveform is caused by the antenna's resonances [31].

IV. Chip Characterization

Conventionally, electronic oscilloscopes (real-time sampling or equivalent-time sampling) with antennas or probes are used to sample short pulses in time domain. As discussed in Section I, this method has major drawbacks. First, current off-the-shelf electronic oscilloscopes have the shortest rising time of 4.5 ps [32], which is not sufficiently fast to measure picosecond pulses accurately. Second, in this method, the picosecond pulses received by antennas/probes have to be transferred to electronic oscilloscopes through waveguides, coaxial cables, and coaxial adapters. Therefore, these blocks need to be accurately de-embedded by performing a broadband calibration, which is complicated, time-consuming, and prone to error [27].

In this paper, we built a time-domain measurement system based on ASOPS for characterizing the radiated picosecond pulses by the designed silicon chip. ASOPS has been historically introduced in the THz time-domain spectroscopy (THz-TDS), where ultrashort EM pulses are

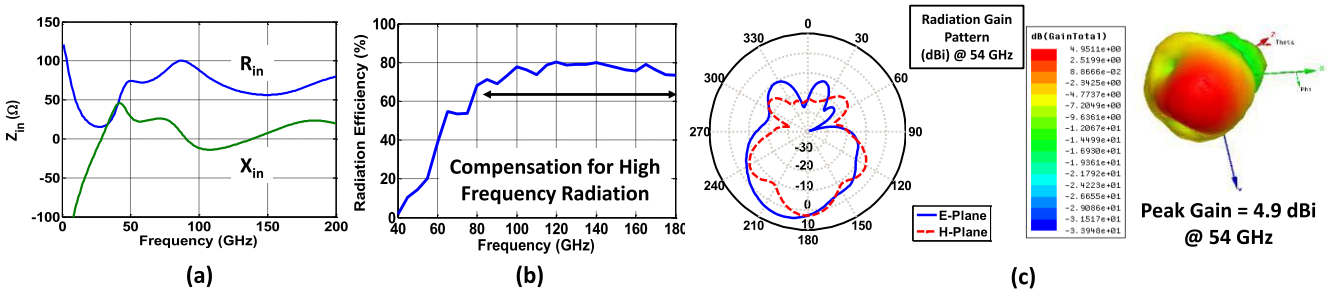

Fig. 19. Frequency-domain EM simulation results of the on-chip antenna using HFSS. (a) Input impedance. (b) Radiation efficiency. (c) Radiation patterns at 54 GHz.

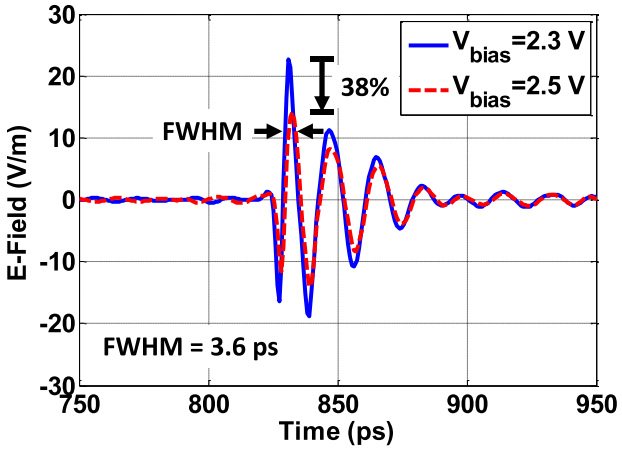

Fig. 20. Simulated time-domain waveform of the radiated picosecond pulse using CST Microwave Studio.

generated by the ASOPS system and are used to perform spectroscopy analysis of passive or active samples [33]. However, in this paper, the generated picosecond pulse is produced by the designed silicon chip rather than the ASOPS system, and this demands technical solutions to ensure that the sample (silicon chip) is synchronized with the ASOPS system. Additionally, in the conventional ASOPS-based THz-TDS, the repetition rate of the generated ultrashort pulse is close to the sampling rate. Instead, in this paper, the repetition rate (1 GHz) of the radiated picosecond pulse from the designed silicon chip is much higher than the sampling rate (50 MHz + 5 Hz) of the ASOSP system, which will be discussed later.

In this section, first, the ASOPS system is briefly reviewed. Second, the technical challenges of using this technique to characterize our chip are addressed. Finally, the measurement results are presented.

A. Overview of Asynchronous Optical Sampling

Fig. 21(a) illustrates the schematic of an ASOPS system. Two femtosecond laser sources generate a pump beam and a probe beam, respectively. The pump beam excites a PCA emitter that radiates a THz pulse, while the probe beam excites a PCA detector that samples the received THz pulse. The sampled data is then transferred to data acquisition electronics. The repetition rates of these two beams (f_{r1} and f_{r2}) are slightly different, which enables the PCA detector to sample

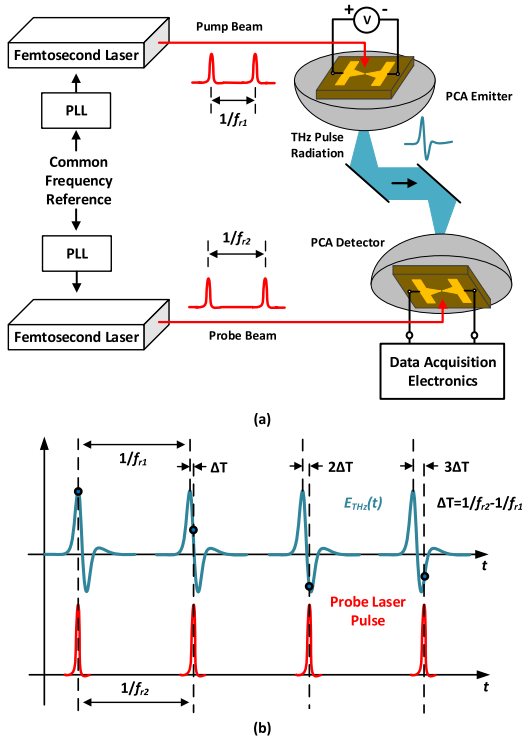

Fig. 21. (a) ASOPS system and (b) its sampling mechanism.

the entire pulse waveform quickly, as shown in Fig. 21(b). The two femtosecond laser sources are controlled by two phase-locked loops that share a common frequency reference for frequency stability purposes. A typical rising time of a PCA detector is of the order of 100 fs [34], [35], which is fast enough to measure picosecond pulses. In addition, because the PCA detector samples the THz pulse right at the antenna, calibration requirements are relaxed significantly compared with the conventional method of using electronic oscilloscopes.

B. Measurement Setup for Characterizing the Prototype Chip in the Time Domain

In this paper, we used a commercial ASOPS system (TAS7500TS) from Advantest Corporation. It is capable of measuring a 380 fs THz pulse with an SNR > 1 BW of

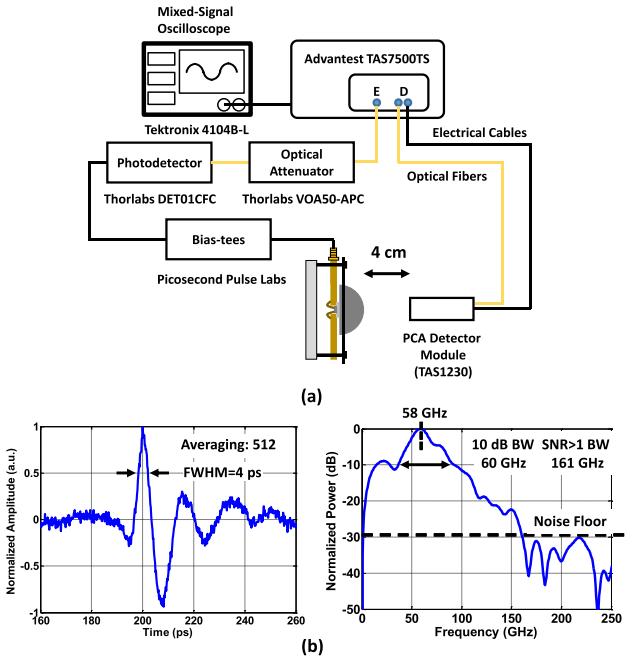

Fig. 22. (a) 50 MHz synchronization configuration and (b) measurement results.

more than 4 THz [29]. The f_{r1} and f_{r2} of this system are 50 MHz and 50 MHz + 5 Hz, respectively. According to the working mechanism of ASOPS, the prototype chip needs to be synchronized with the pump femtosecond laser.

1) 50 MHz Synchronization Configuration: To test this measurement technique, a straightforward synchronization configuration is first examined, as shown in Fig. 22(a). A photodetector is used to convert the 50-MHz pump laser into an electrical trigger, which is fed to the prototype chip. A PCA detector is placed in the far-field region. With the four impulse generation channels ON, the measurement setup captures a 4 ps (FWHM) radiated pulse. Its normalized power spectrum is obtained by performing discrete Fourier transform on the time-domain waveform. The measured radiated pulse has a peak frequency component at 58 GHz, a 10-dB BW of 60 GHz, and an SNR > 1 BW of 161 GHz [Fig. 22(b)]. It is necessary to note that the commonly used relation between pulsewidth (T_p) and BW, which is BW $= 2/T_p$, is not valid in this case, because the generated picosecond pulses are not obtained by modulating a sinusoidal carrier signal with a square wave.

2) Custom Synchronization Setup: One of the drawbacks of the TAS7500TS system is that the repetition rate of the pump femtosecond laser is fixed at 50 MHz. However, the prototype chip can radiate picosecond pulses with a repetition rate as high as 1 GHz. Therefore, another configuration is designed to generate an adjustable and synchronized trigger, as shown in Fig. 23(a). In the synchronization circuitry, a broadband divide-by-five frequency divider is used to extract a 10-MHz sinusoidal signal from the 50-MHz pump femtosecond laser. Then, an RF signal generator is locked with the 10-MHz signal and used to generate synchronized triggers with tunable frequencies. RF filters and low noise amplifiers are used in

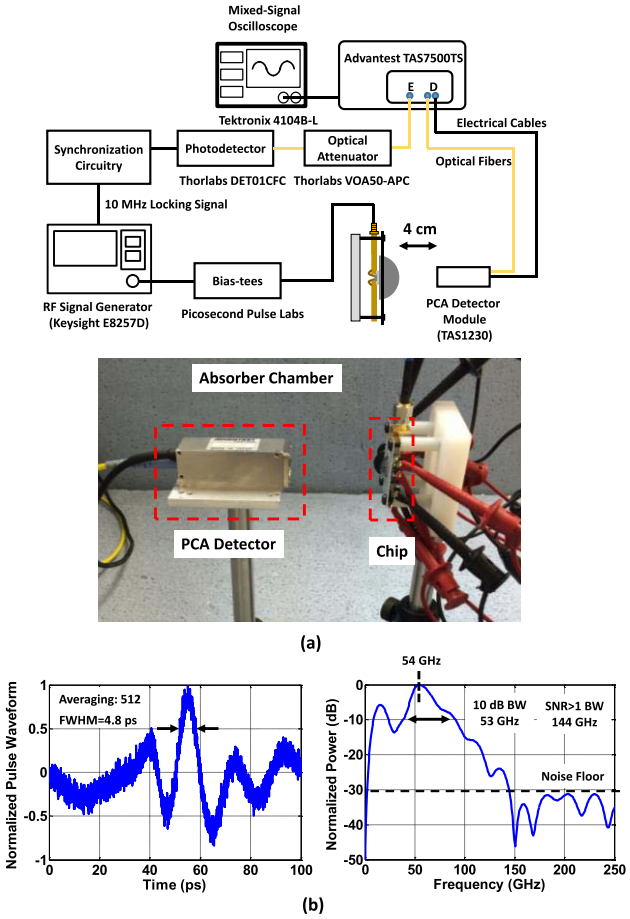

Fig. 23. (a) Custom synchronization setup and (b) measurement results with a 1-GHz trigger.

the synchronization circuitry to achieve a low-noise locking with the RF signal generator. Meanwhile, a PCA detector is placed in the far-field region. With a 1-GHz trigger, this measurement setup captures a 4.8 ps (FWHM) radiated pulse. Similar to the simulated result (Fig. 20), some ringing appears after the main pulse. The ringing before the main pulse is caused by the multiple round-trip reflections between the chip and the PCA detector. The maximum distance between them is 4 cm, limited by the low sensitivity of the PCA detector. Its normalized power spectrum has a peak frequency component at 54 GHz, a 10-dB BW of 53 GHz, and an SNR > 1 BW of 144 GHz [Fig. 23(b)]. Fig. 24(a) presents the radiated time-domain waveforms in different angles. This measurement shows that the pulse duration remains small in a wide range of angles. In Fig. 24(b), the measured radiation patterns of the peak-to-peak amplitude of the radiated pulse waveform are slightly tilted compared with the simulation results, which is mainly caused by the tiny misalignment of the silicon lens.

It is important to note that the Advantest TAS7500TS ASOPS system is designed for THz-TDS applications, which measures the changes caused by the sample under test. Therefore, the PCA detector and its internal amplifiers are not fully calibrated for their gains and distortion effects. As a result, all the reported time-domain waveforms and spectrums are normalized and the difference between the measured pulsewidth

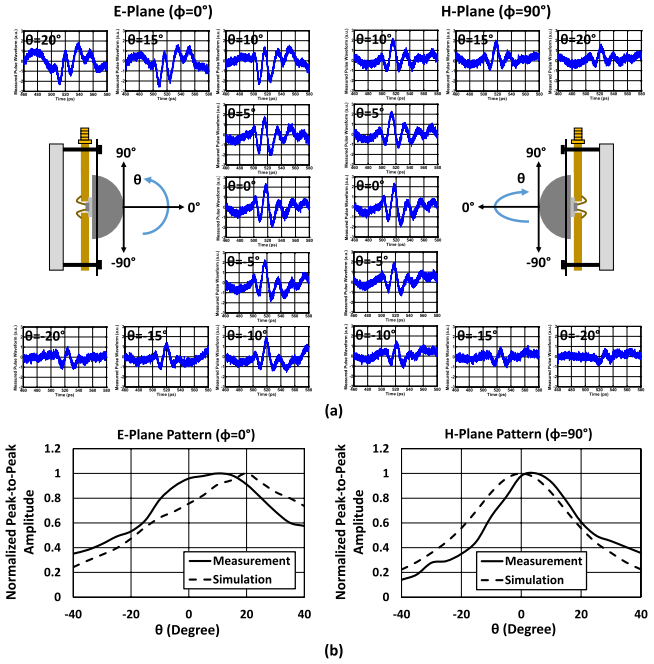

Fig. 24. (a) Measured time-domain radiation waveforms using a 1-GHz trigger at different angles. (b) Measured radiation patterns of the peak-to-peak amplitude of the radiated pulse waveform using a 1-GHz trigger.

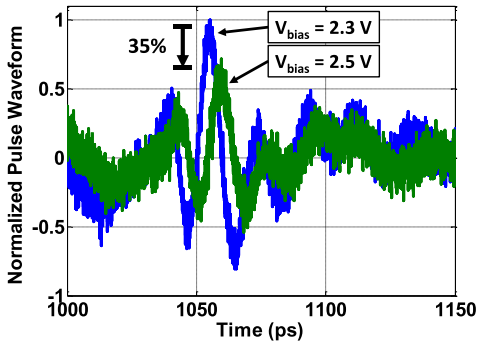

Fig. 25. Measured NLQSI-induced tunable pulse peak amplitudes.

of the radiated pulse and the simulated result is mainly due to the nonideality of the PCA detector. Radiated power characterizations cannot be performed using this system.

C. Demonstrations of NLQSI Effects on Pulse Amplitudes and Pulse Amplitude Modulation

Using the measurement setup shown in Fig. 23(a), pulse amplitude modulation is demonstrated. Fig. 25 shows the results of this measurement. As discussed in Section II, when the bias voltage of transistor Q_2 is set to 2.5 V, the peak of the measured radiated picosecond pulse reduces by 35% compared with that when V_{bias} is 2.3 V. This relative change[5] is close to the simulated value (38%) shown in Fig. 20.

The same setup is also used to measure pulse amplitude modulation by turning ON/OFF the impulse generation channels. Fig. 26 presents the measured peak amplitudes of the radiated combined pulses in all 16 combinations. Due to the

[5]Due to the non-ideality of the PCA detector and its internal amplifiers, it is accurate to perform relative change value comparisons.

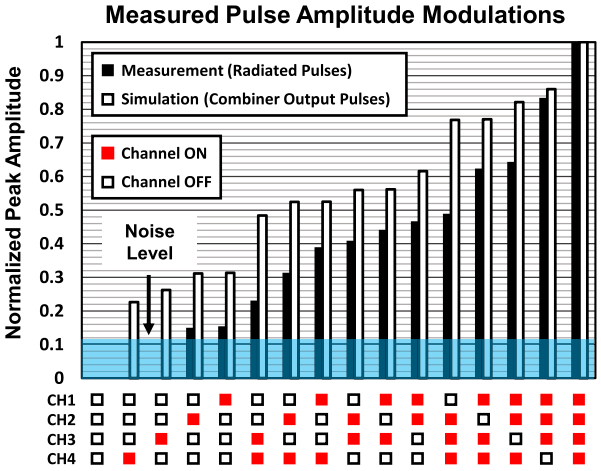

Fig. 26. Measured pulse amplitude modulations.

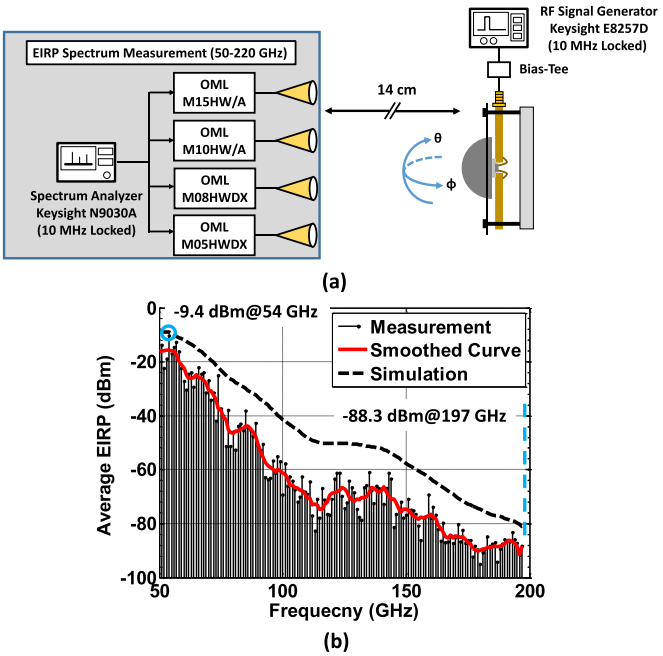

Fig. 27. (a) EIRP measurement setup and (b) measured average EIRP spectrum.

limited sensitivity of the measurement setup, the combined pulses of the first two combinations are too weak to be detected. The differences between the measured and simulated results are due to the nonidealities of the on-chip antenna and the PCA detector.

D. EIRP and Frequency-Domain Radiation Pattern

To characterize the equivalent isotropically radiated power (EIRP) spectrum, a frequency-domain measurement setup is utilized, as shown in Fig. 27(a). Four OML harmonic mixers and four standard-gain horn antennas are used to measure EIRP from 50 to 220 GHz. The RF signal generator provides a 1-GHz trigger for the prototype chip. Fig. 27(b) shows the measured average EIRP spectrum of the radiated picosecond pulse train with a 1-ns period. It has a peak frequency component at 54 GHz with an average EIRP

TABLE I
COMPARISON WITH STATE-OF-THE-ART PICOSECOND IMPULSE RADIATORS IN SILICON

	This Work	[26]	[23]	[13]	[14]	[4]
Architecture	Digital-to-Impulse (with NLQSI)	Digital-to-Impulse 4×2 Array	Digital-to-Impulse	VCO+Modulation	VCO+Modulation	Pulsed VCO
Pulse Duration (FWHM)	4 ps	5.4 ps	8 ps	36 ps	45 ps	60 ps
THz-TDS Characterization	Yes	Yes	No	No	No	No
Measured SNR>1 Bandwidth	161 GHz (Time Domain)	Approx. 980 GHz (Freq. Domain) *	Approx. 170 GHz (Freq. Domain) *	Approx. 30 GHz (Freq. Domain)	21 GHz (Freq. Domain)	Approx. 20 GHz (Freq. Domain)
Measured EIRP Spectrum	50-197 GHz	50-1032 GHz *	50-220 GHz *	79-109 GHz	251-272 GHz	20-40 GHz
On-Chip Impulse Combining	Yes	No	No	No	No	No
Impulse Amplitude Modulation	Yes	No	No	No	No	No
EIRP	-9.4 dBm @ 54 GHz (1GHz rep. rate) **	30 dBm @ 100 GHz (peak EIRP) ***	13 dBm @ 50 GHz (peak EIRP) ***	12 dBm @ 94 GHz (CW mode)	15.7 dBm @ 260 GHz (CW mode)	6.5 dBm @ 30 GHz (peak EIRP) ***
DC Power	170 mW	710 mW	220 mW	435 mW	800 mW	106 mW
Die Area	1 mm^2	2.4 mm^2	0.47 mm^2	6.16 mm^2 ****	2.3 mm^2	2.85 mm^2
Technology	0.13 µm SiGe BiCMOS	90 nm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	65 nm Bulk CMOS	0.13 µm SiGe BiCMOS

* The power level of the radiated pulse and the sensitivity level of the receivers in these two papers are different from this work.
** It is average EIRP value of a 4.8 ps pulse train with a 1 ns period.
*** Peak EIRP is the estimated CW-mode EIRP based on the measured average EIRP.
**** It includes the die area of a receiver.

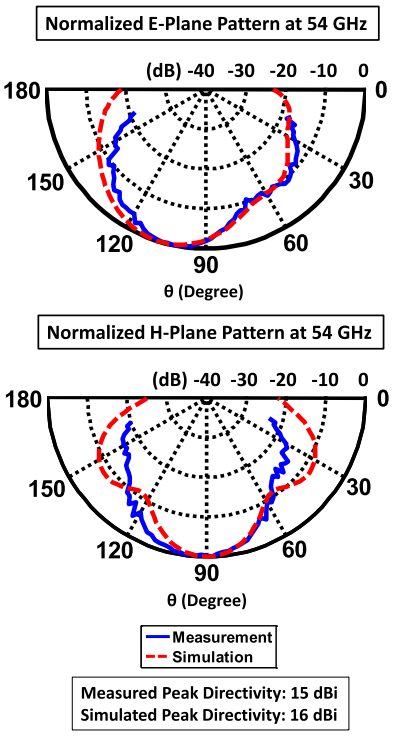

Fig. 28. Measured frequency-domain radiation patterns at 54 GHz.

value of −9.4 dBm, which is close to the simulated value. The measured and simulated EIRP spectrums have similar decay trends. However, in the mm-wave regime, the simulated EIRP values are larger than the measured results, which is mainly caused by the inaccurate extrapolated transistor models. The highest detectable frequency component is at 197 GHz, which is limited by the sensitivity of the measurement setup. Meanwhile, the peak frequency in the measured EIRP spectrum is identical to that obtained using the ASOPS system, as shown in Fig. 23. Compared with the measured power spectrum in Fig. 23, the decay rates after the peak frequency components differ in the two figures, which is due to the gain effects of the PCA detector and internal amplifiers in the ASOPS system.

Using the setup in Fig. 27(a), the radiation patterns at the peak frequency of 54 GHz are measured, as shown in Fig. 28. The measured main lobes are slightly tilted compared with the

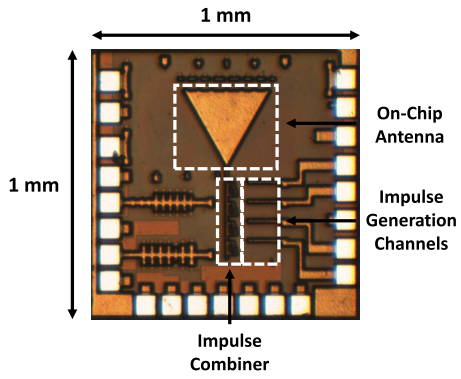

Fig. 29. Chip micrograph.

simulation results, which is due to the chip package and the tiny misalignment of the silicon lens.

Finally, the chip micrograph is shown in Fig. 29. The chip is fabricated in a 130-nm SiGe BiCMOS process and occupies a die area of 1 mm × 1 mm. The chip consumes a dc power of 170 mW.

V. Conclusion

In this paper, an NLQSI technique is reported for the generation of picosecond pulses with tunable peak amplitudes. A prototype chip is implemented that comprises four NLQSI-based impulse generation channels, an on-chip impulse combiner, and an on-chip antenna. In addition, an on-chip impulse-coupling scheme is introduced to eliminate the undesired ringing caused by the transmission line effects of the supply routings. The on-chip impulse combiner provides a single-chip solution for radiating picosecond pulses with amplitude modulation capability. For the first time, an ASOPS system is used to characterize the picosecond pulses directly radiated by a silicon chip in the time domain. Based on the measurements, the prototype chip radiates 4 ps pulses with an SNR > 1 BW of 161 GHz. The performance of the chip is compared with state-of-the-art picosecond impulse radiators in Table I.

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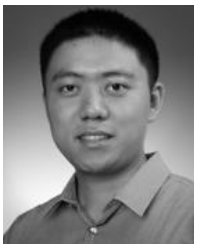

Peiyu Chen (S'14) received the B.Eng. degree (Hons.) in information engineering (optoelectronics) from Zhejiang University, Hangzhou, China, in 2012, and the M.S. degree in electrical engineering from Rice University, Houston, TX, USA, in 2015, where he is currently pursuing the Ph.D. degree.

His current research interests include innovative integrated circuit techniques in mm-wave and terahertz frequency regimes, measurement techniques for ultrafast electromagnetic waves, mm-wave 3-D imaging, and CMOS photonics techniques.

Mr. Chen was a recipient of the Best Student Paper Award (first place) in the 2015 IEEE Radio and Wireless Symposium and the Best Student Paper Award (second place) in the 2016 IEEE International Microwave Symposium.

M. Mahdi Assefzadeh (S'14) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 2011, and the M.S. degree in electrical engineering from Rice University, Houston, TX, USA, in 2014, where he is currently pursuing the Ph.D. degree.

Mr. Assefzadeh was the recipient of the Best Paper Award in the IEEE International Microwave Symposium 2014, the Best Paper Award in the IEEE Radio and Wireless Symposium 2016, and the 2nd Best Paper Award in the IEEE APS 2016. He was the recipient of the Texas Instruments Distinguished Fellowship in 2012. He was also the Gold Medal winner of the National Physics Competition in 2006 and the Gold Medal winner of the 38th International Physics Olympiad in 2007.

Aydin Babakhani (M'08) received the B.S. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from Caltech, Pasadena, CA, USA, in 2005 and 2008, respectively.

He was a Post-Doctoral Scholar with Caltech in 2009 and a Research Scientist at the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, in 2010. He is currently a Louis Owen Junior Chair Assistant Professor with the Electrical and Computer Engineering Department and the Director of the Rice Integrated Systems and Circuits Laboratory, Rice University, Houston, TX, USA.

Dr. Babakhani has won multiple Best Paper Awards including the Best Paper Award in the IEEE Radio and Wireless Symposium (RWS) in 2016 and 2015, the Best Paper Award in the IEEE International Microwave Symposium (IMS) in 2014, and the second-place Best Paper Awards in the IEEE APS 2016 and the IEEE IMS 2016. He was the recipient of a prestigious NSF CAREER Award in 2015, an Innovation Award from Northrop Grumman in 2014, and a DARPA Young Faculty Award (YFA) in 2012. He was the recipient of the Caltech Electrical Engineering Department's Charles Wilts Best Ph.D. Thesis Prize for his work on near-field direct antenna modulation (NFDAM). From 2006 to 2008, he was the Vice Chair of the IEEE Microwave Theory and Techniques Society Metro LA/SFV joint sections MTT-S Chapter 17.1. He was the recipient of the Microwave Graduate Fellowship in 2007, the Grand Prize in the Stanford–Berkeley–Caltech Innovators Challenge in 2006, Analog Devices Inc. Outstanding Student Designer Award in 2005, as well as Caltech Special Institute Fellowship and Atwood Fellowship in 2003. He was also the Gold Medal winner of the National Physics Competition in 1998 and the Gold Medal winner of the 30th International Physics Olympiad in 1999, in Padova, Italy.