

A Tunable Concurrent 6-to-18GHz Phased-Array System in CMOS

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Abstract — This paper presents a scalable phased-array receiver system that covers a tritave bandwidth of 6-to-18 GHz implemented in a 130nm CMOS process. The single receiver element with a 10-bit phase shifting resolution achieves a maximum phase error of 2.5° within a baseband amplitude variation of 1.5dB for an arbitrary target angle. This dense interpolation provides excellent phase error/offset calibration capability in the array. A 4-element electrical array pattern is measured at 6GHz, 13.5GHz and 18GHz, showing a worst case peak-to-null ratio of 21.5dB. The EVM and phase noise improvements of the array compared with the single receiver element are also shown.

Index Terms — Array signal processing, beam steering, CMOS integrated circuits, interference suppression, phased-array radars.

I. INTRODUCTION

Very-large-scale phased-array systems are used in many applications such as communications, radars, and radio astronomy, etc., where high-speed scanning and concurrent multi-beam operations are often needed [1][2].

Traditional phased-array systems are built with discrete modules often fabricated in compound processes. Besides the significant cost problem, the implementation difficulty is exacerbated on the system level due to issues such as signal distribution, phase mismatches, and reliability.

Recent advances in CMOS have enabled unprecedented integration levels, making it possible to implement a phased-array element on a single chip to form a scalable array system, where additional elements can be added with no extra overhead. In addition, CMOS supports high-density digital circuits, which provide calibration capability that ensures the array system performance for large number of elements.

We implemented a CMOS phased-array receiver capable of concurrently forming four beams at two frequencies within a tritave frequency from 6GHz to 18GHz. To the best of the authors' knowledge, this is the first multi-beam and multi-band CMOS phased-array receiver element.

This paper is organized as follows: Section II introduces the proposed phased-array system. The phase interpolation results are shown in Section III. Section IV demonstrates an effective calibration method for various phase errors and offsets in an array system. The measured electrical array patterns, EVM results, interference rejection, and phase noise improvement are presented in Section V.

II. PHASED-ARRAY SYSTEM AND RECEIVER ARCHITECTURE

Our proposed phased-array system is shown in Fig. 1. Antennas and a broadband GaN LNAs receive the incoming signal in the horizontal (HP) and vertical (VP) polarizations, which are then fed to the CMOS receiver. The receiver architecture [3] is shown in Fig. 2.

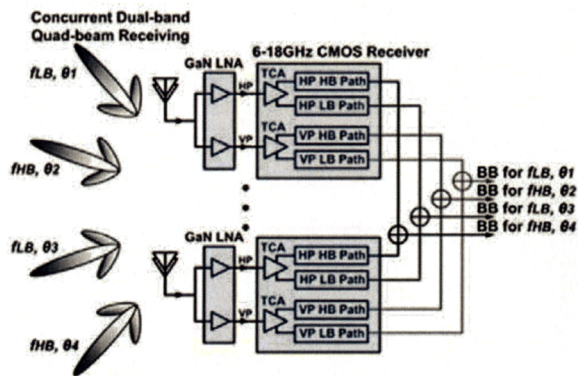


Fig.1. Proposed phased-array receiver system

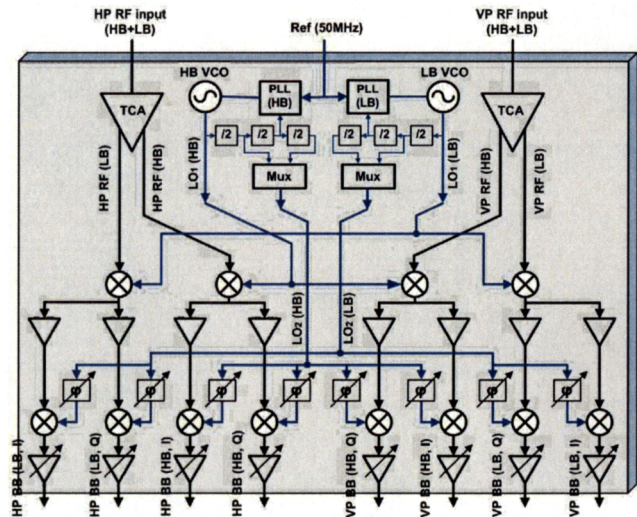


Fig.2. CMOS phased-array receiver architecture

A wideband tunable concurrent amplifier (TCA) splits the RF signal into low-band (LB) from 6 to 10.4GHz and high-band (HB) from 10.4 GHz to 18GHz. The LB and HB signals are separately down-converted by two mixers to IF and then

baseband. Both LB and HB paths have independent on-chip frequency synthesizers, which provide two local oscillator signals (LO₁ and LO₂) each. The phase shifting of the LO₂ signal achieved by a 10-bit interpolating phase rotator [4], which weights and sums I and Q components of the LO₂:

$$LO_2(t) = A \cdot \sin(\omega t) + B \cdot \cos(\omega t) \\ = \sqrt{A^2 + B^2} \cdot \sin(\omega t + \varphi), \quad (1)$$

where $\varphi = \text{atan}(B/A)$.

Baseband signals from different elements are eventually combined in current domain for beam forming. Fig. 3 shows the chip microphotograph.

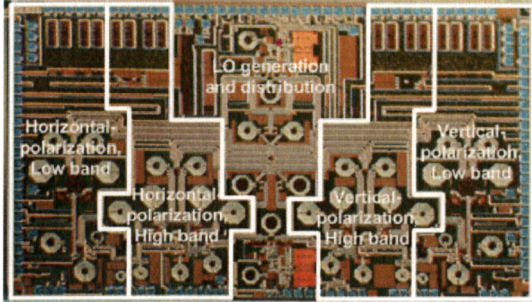


Fig. 3. Die photograph of the CMOS receiver with a chip area of 3.0mm×5.2mm, implemented in the IBM 8RF 130nm CMOS process

With the dual-polarization and dual-band architecture, the receiver is capable of forming four beams simultaneously at two different frequencies in the 6 to 18GHz bandwidth. In addition, the 1024 (10-bit) interpolation points provide the receiver with excellent phase rotating performance, which will be presented in next section.

III. PHASE INTERPOLATION PERFORMANCE OF THE RECEIVER

Phase rotating in all four quadrants has been measured at RF frequencies of 6GHz, 10.3GHz, 13.9GHz, and 18GHz. Fig.4 shows the measured phase and amplitude interpolation results for the baseband signal at an RF frequency of 18GHz.

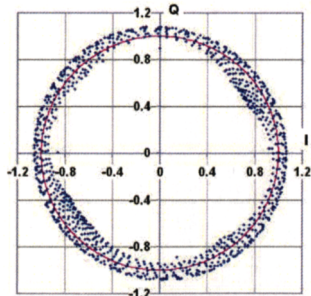


Fig. 4. Measured interpolated baseband signal (dots) and ideal baseband with 360° phase rotating (solid curve)

With a worst-case amplitude variation of 1.5dB, a maximum phase step of 3° is achieved at an RF frequency of 18GHz. This means that when the receiver is targeting an arbitrary angle in the full 360° range, the error will not exceed 1.5°. Table I summarizes the interpolating results in the tritave bandwidth.

TABLE I
SUMMARY OF PHASE INTERPOLATING RESULTS

	Max Phase Error	Max Amplitude Variation
RF=6GHz	2.5°	1.3dB
RF=10.3GHz	1.3°	1.0dB
RF=13.9GHz	1.4°	1.3dB
RF=18GHz	1.5°	1.5dB

IV. PHASE ERRORS AND OFFSETS IN PHASED-ARRAY SYSTEMS

A. Errors within a Single Receiver Element

There are two major types of phase interpolation errors in a phased-array element with LO phase shifting.

The first kind of error arises from practical limits on the LO I/Q signal phase and amplitude matching [5]. This error is exacerbated by inevitable mismatches in the LO networks.

Another type of error is the zero crossing distortion of the phase-shifted LO signal with excessive harmonics. I/Q-interpolating phase rotators are inherently dispersive systems, which offset the input by a constant phase shift instead of a constant group delay, shown in Fig. 5. The resulting zero crossing errors in the dispersed LO waveforms lead to baseband phase errors after downconversions by switching mixers.

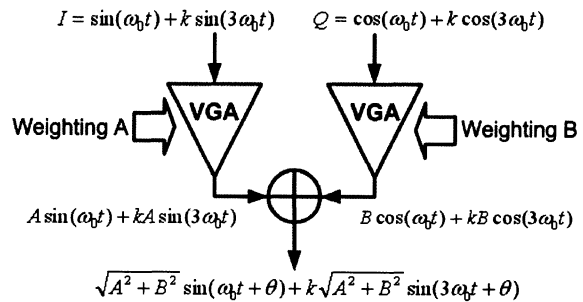


Fig. 5. The phase rotator causes waveform dispersion for the input quadrature signals with multiple frequency contents. $3\omega_0$ is assumed as the dominant harmonic for differential circuits.

However, dense phase interpolation can compensate both errors by choosing appropriate I/Q weightings. The measured phase errors before and after compensation are shown in Fig.6 and Fig.7 for the case of LO I/Q mismatch and the case of non-sinusoidal LO, respectively. Both cases are based on 360° full range interpolation with a phase step of 11.25°.

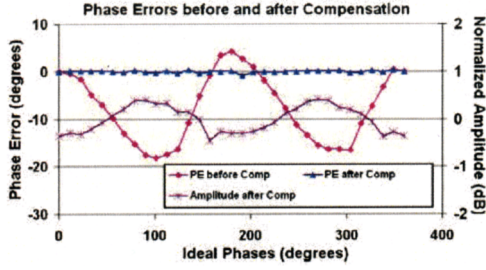


Fig. 6. Phase errors before/after compensation for the case of LO I/Q mismatch at f_{RF} of 10.4GHz. Within an amplitude variation of 0.45dB, a maximum phase error of 0.9° is achieved.

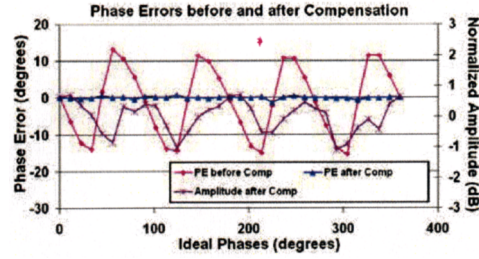


Fig. 7. Phase errors before/after compensation for the case of non-sinusoidal LO at f_{RF} of 10.4GHz. Within an amplitude variation of 1.09dB, a maximum phase error of 1.4° is achieved.

B. Offset Errors across Receiver Elements

In a phased-array system, delay offsets always exist in the RF feed paths and the reference clock distribution network. For narrowband system, these offsets can be approximated by phase shifts ζ_k and ψ_k in the normalized array pattern (AP) formula (2), assuming θ is the incident phase difference from the main lobe. Although deterministic, these offsets are generally hard to predict *a priori* and compensate off-chip, particularly in a very-large-scale array system.

$$AP(\theta) = \exp[i\delta_1] + \exp[i\delta_2] + \dots \exp[i\delta_N] \quad (2)$$

where $\delta_k = (k-1)\theta + \zeta_k + \psi_k$

Dense on-chip phase interpolation can easily compensate these two offsets by providing a phase shift to cancel the sum of ζ_k and ψ_k for the k th element. Fig. 8 shows the 4-element array pattern measured with/without offset calibration.

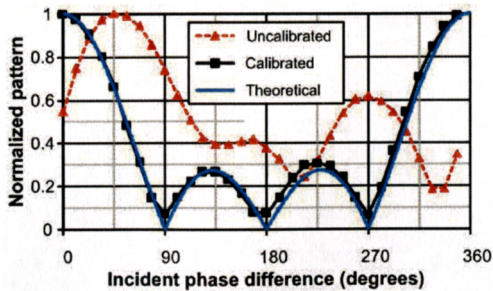


Fig. 8. Array patterns with/without calibration (f_{RF} =10.4GHz)

V. ARRAY MEASUREMENT RESULTS

Our 4-element phased-array system setup is shown in Fig.9. A 4-way power divider distributes the input signal into four RF feed paths. Discrete phase shifters are used to form the effective input wave front. A 50MHz synthesizer reference is sent to every element. The baseband output signals and their sum are monitored by a digital oscilloscope.

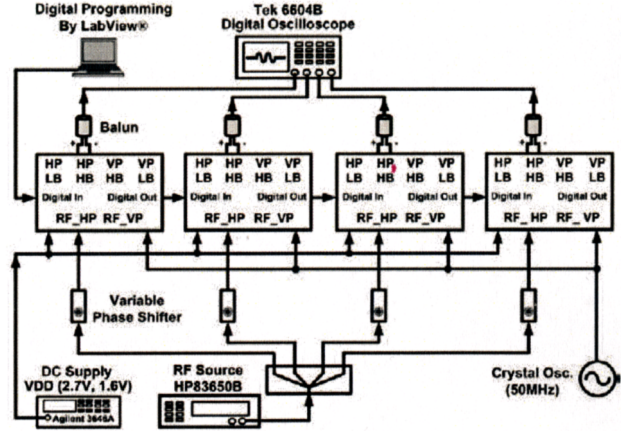


Fig. 9. Measurement setup for array performance characterization

A. Electrical Array Pattern Performance

Normalized electrical array patterns for beam forming at different incident angles have been measured for the RF frequencies of 6GHz, 10.4GHz, and 18GHz respectively, shown in Fig.10. The worst case peak-to-null ratio is 21.5dB. The measured array patterns closely match the ideal ones due to the aforementioned compensations and calibrations facilitated by dense phase interpolations.

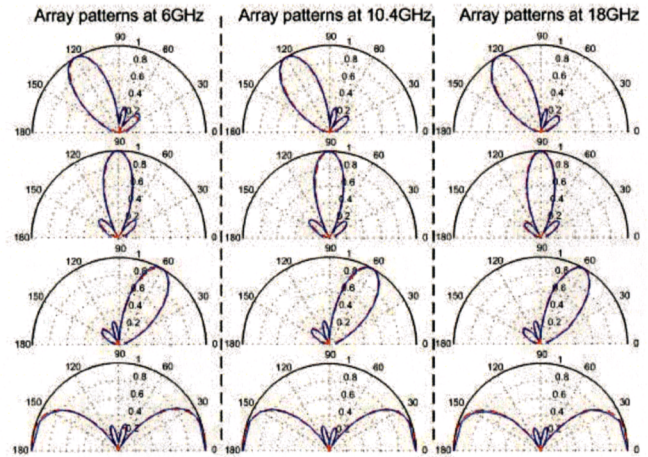


Fig. 10. The measured electrical array patterns (solid curves) versus the ideal array patterns (dash lines)

B. Array Error Vector Magnitude (EVM) Performance

A phased-array system has improved EVM results compared with a receiver element mainly for three reasons. First, the signal-to-noise-ratio (SNR) for the array increases by a factor of N (the number of array elements). Second, any low power interference with a different incident angle is attenuated due to the array spatial filtering property. Third, EVM caused by any LO uncorrelated errors, such as phase noises, in a receiver element will decrease by \sqrt{N} in the array.

The EVM for a 4-element receiver array has been measured and compared to the EVMs of the individual elements at different symbol rates, shown in Fig. 11, which validates the aforementioned improvements. Fig. 12 shows the measured array EVM when an in-band FM-modulated interference is applied at different incident angles. Significant rejection is achieved compared to a single receiver element when the interference is incident at an angle away from the main lobe. Fig. 13 shows the measured phase noise power spectral density decreases by 6dB in the 4-element array operation.

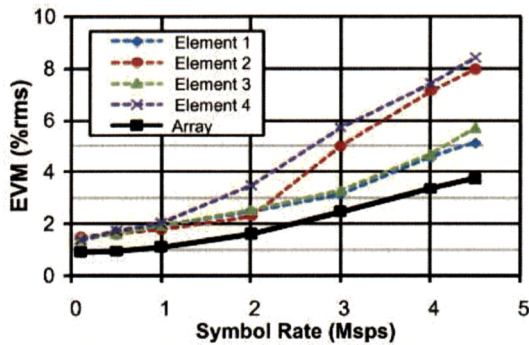


Fig. 11. Measured EVM for the 4 receiver elements and the 4-element phased-array at different symbol rates

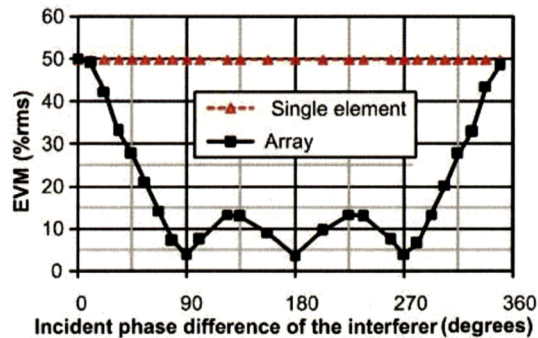


Fig. 12. Measured EVM for the phased-array compared with a receiver element when interference is incident at different angles

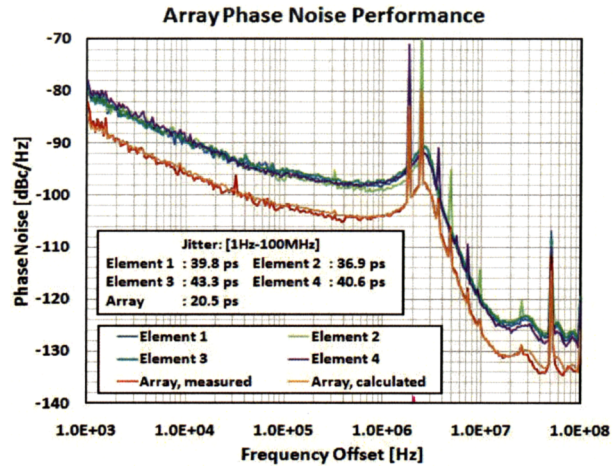


Fig. 13. Measured phase noise performance ($f_{RF}=7.5\text{GHz}$)

VI. CONCLUSION

In this paper, a 4-element concurrent dual-band quad-beam CMOS phased-array receiver system is presented. With a 10-bit LO phase shifting scheme, the receiver chip achieves dense phase interpolations, which facilitate calibrations on mismatches and offsets in the array system for performance optimization. Within the entire tritave bandwidth, the phased-array demonstrates excellent array patterns, EVM improvement, phase noise reduction, and interference rejection capability.

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