Multi-Order Transmission Line-Radial Stub Networks for Broadband Impedance Matching and Power Combining in a Watt-Level Silicon Power Amplifier

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***Abstract*— In this paper, multi-order, on-chip transmission line-radial stub ladder networks are designed to perform fundamental and harmonic impedance matching and power combining in a broadband silicon power amplifier. A 16-40GHz, 1W PA with integrated 50Ω output matching and power combining is designed in a 130nm SiGe BiCMOS process. The PA achieves a peak gain of 23.8dB and a maximum single ended output power of 30.6dBm with 21.9% power-added efficiency (PAE). On chip transmission line-radial stub-based matching and combing networks are designed and optimized for maximum efficiency to provide optimum load conditions at fundamental and harmonic frequencies and to combine the power of 16 separate amplifiers with minimized passive loss. Load pull simulations are performed in the frequency range considering load conditions up to the 5th harmonic. The simulated total loss from the output matching and the 16-to-1 combining network is less than 2.9dB in the entire frequency band.**

***Index Terms*—integrated circuits, BiCMOS, power amplifiers, radial stub, transmission line, broadband, power combining, SiGe, silicon.**

I. Introduction

Recent improvements in the performance of CMOS and BiCMOS process technologies has continued to promote the growth of mm-wave systems in silicon for wireless communication, radar, security screening, and medical applications. These systems require fully-integrated watt-level power amplifiers (PAs) in silicon. In addition to power requirements, several applications, e.g. broadband mm-wave wireless links, demand a stand-alone PA for the entire frequency range with a large bandwidth. To realize a high-power PA in silicon, broadband on-chip power combining and matching networks must be optimized for minimum loss while achieving a large bandwidth [1].

Integrating a PA in silicon significantly benefits from large-scale integration, low cost of fabrication, and co-integration with digital control circuits. However, as silicon processes are continuously evolving, tougher limits on low break-down voltage of the transistors, poor metal conductivity, and conductive substrate losses play critical roles as challenges toward an efficient PA. Because of these challenges, a single transistor in silicon cannot generate watt-level output powers. Hence, the solution is a low-loss on-chip combining network that can efficiently combine the power from several elements.

A fractional bandwidth near 100% for a PA requires broadband inter-stage and output matching and combining networks that usually result in a high loss from the large number of passive elements needed. Also, controlling harmonic impedances plays an important role in increasing the power-added efficiency (PAE) in Class-J power amplifiers [2]. Thus, novel architectures for broadband matching and combining networks are required to simultaneously provide optimum load conditions at fundamental and harmonic frequencies with minimum loss.

In this paper, a broadband 16-40GHz PA with 1W output power is designed that combines the power of 16 single-element PAs and achieves a peak power gain of 23.8dB with 21.9% PAE. Each amplifying element is equipped with broadband inter-stage and output matching networks that are based on transmission line-radial stub (TL-RS) ladder networks. Load-pull simulations are performed to find optimum load conditions at fundamental and harmonic frequencies. Broadband matching and combining networks are also optimized for minimum loss while satisfying matching goals.

The paper is organized as follows. Section II focuses on the architecture of the 16-element PA. Section III describes the design details for a single-element amplifier. Power combining and output matching networks and simulation results are explained in Section IV and Section V concludes the paper.

II. PA Architecture

The 130nm SiGe BiCMOS process technology used in this work has a 4μm top metal layer, an 11Ωcm substrate resistivity, and an f_T / f_{max} of 200GHz/290GHz. This process supports digital blocks in a 1.2V, 130nm CMOS. The collector-emitter breakdown voltage of the bipolar transistors is $\mathrm{BV_{CEO}} \approx 1.7\mathrm{V}$, which sets a limit on the available power from a single transistor. In this process, 10 parallel bipolar transistors with emitter length of 18μm can deliver 21dBm power in optimum matching conditions for a collector biasing of 1.6V and a base biasing of 0.82V. To compensate the

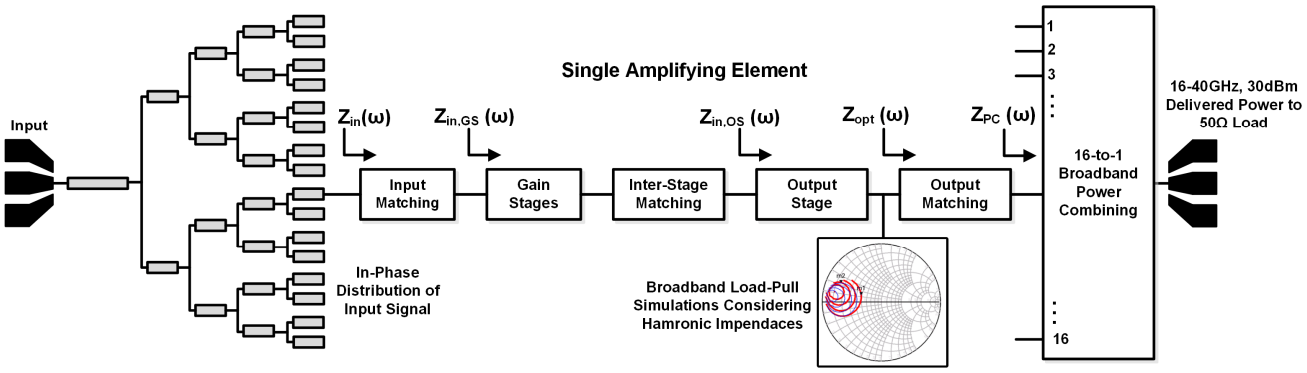

Fig. 1. 16-element PA architecture

overall loss from the output matching and power combining networks, in this design, 16 separate amplifiers was needed for a 30dBm output delivered power.

Fig. 1 shows the architecture of the full PA. First, the input signal is distributed by an equiphase dividing network and input matching is performed before the gain stages. Each amplifier branch consists of two gain stages that are optimized for high gain and connected by inter-stage matching networks. Afterwards, an output stage is optimized for maximum delivered power (P_{del}) and PAE based on load-pull results for load conditions up to the 5th harmonic. Next, a broadband output matching and a 16-to-1 power combining networks are designed to combine and provide optimum load impedances at the output of each transistor.

III. Design of a Single-Element PA

The output stage of each single-element PA consists of 10 parallel 18μm bipolar transistors. A gain of 8dB is achieved over the 16-40GHz bandwidth with unconditional stability (k-factor>1). Lower frequency stability is ensured by using stabilizing resistors at the base biasing branch of the bipolar transistors. The output power of each PA is optimized at 21dBm. Fig. 2 shows the simplified circuit schematic of the output stage along with load-pull simulations. Load-pull P_{del} and PAE contours for 16GHz, 28GHz, and 40GHz, and broadband termination goals is plotted for the entire band and shown in Fig. 2. For example, the maximum available PAE and P_{del} at 28GHz is 44% and 21.2dBm, respectively. A 5% mismatch tolerance is allowed for the optimum load conditions ($s_{11,opt}$) which corresponds to 4% error in PAE and 0.3dB error in P_{del}. In addition to load-pull simulations for fundamental frequencies, load impedances up to the 5th harmonic are also optimized for maximum PAE. Optimum harmonic terminations are shown in Eq. 1,

$$\begin{aligned} Im\{Z_{h2}\} &> 7\Omega, \\ |Im\{Z_{h2}\}| &> 5\Omega, \\ |Im\{Z_{h2}\}| &> 5\Omega, \\ |Im\{Z_{h2}\}| &> 5\Omega. \end{aligned} \tag{1}$$

Two cascaded gain stages with five parallel 18μm bipolar transistors precede the output stage. The combined gain from the two gain stages is 13dB. A 5th order TL-RS ladder network is designed for inter-stage matching.

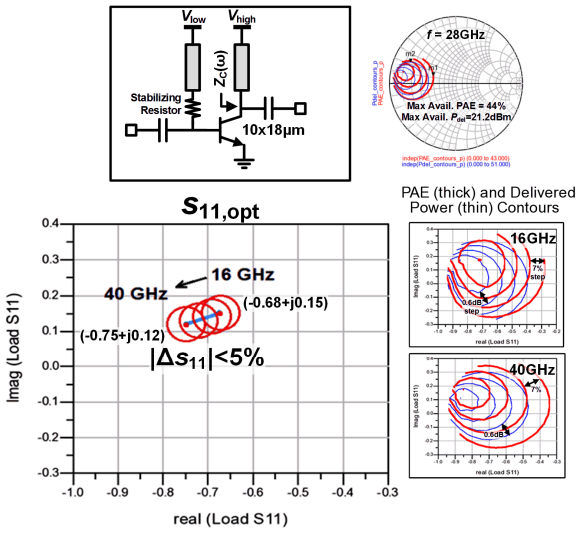

Fig. 2. Output stage load-pull simulations for 16-40GHz

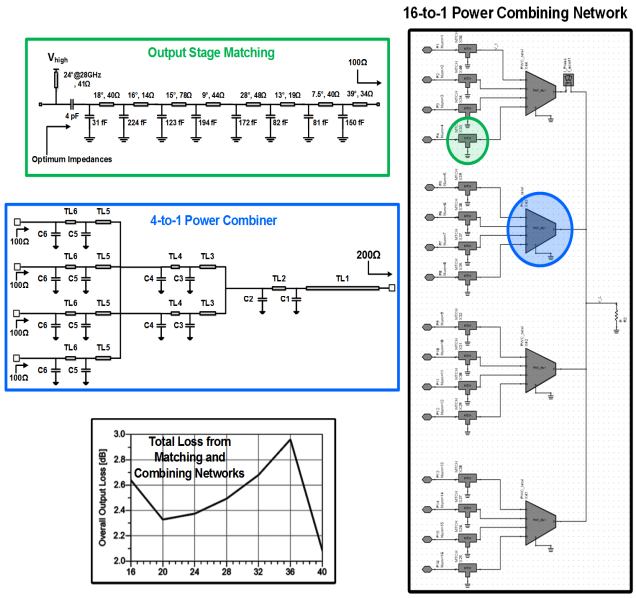

Fig. 3. Output stage matching and 16-to-1 power combiner

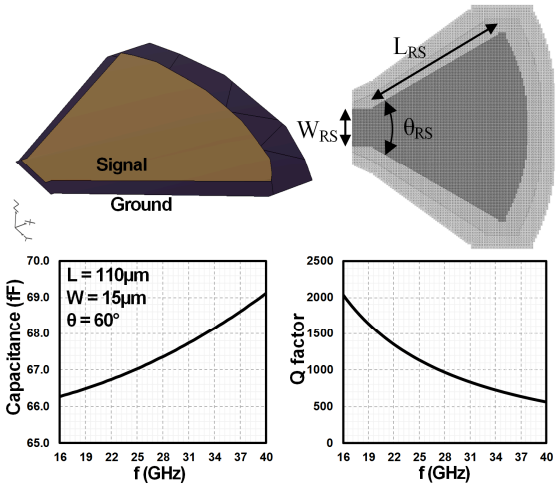

Fig. 4. An on-chip radial stub as a high frequency capacitor

IV. Output Matching and 16-to-1 Power Combining

Broadband output matching and power combining networks are required to achieve 1W delivered power with maximum efficiency over the entire frequency band. 8th-order transmission line-capacitor ladder networks are designed to satisfy broadband optimum load conditions at the output of each PA. In addition, a 16-to-1 output power combining network is designed and shown in Fig. 3, which consists of four separate 4-to-1 power combiners.

In this work, capacitors used in the ladder networks are realized using on-chip radial stubs. Fig. 4 shows the geometry of an on-chip radial stub made by the top metal layer (M6) and M5 for its ground shield, its capacitance and quality factor. High quality factor of the radial stubs at high frequencies significantly contributes to low insertion loss of the matching and combining networks, as well as satisfying harmonic load condition goals. Numerical optimization of the network parameters for optimum load conditions and minimum loss is performed using Keysight ADS software.

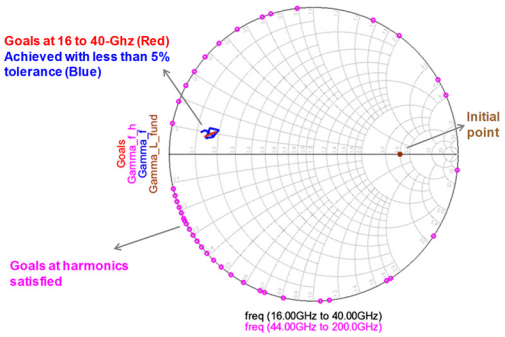

Fig. 5. Broadband termination goals achieved with a 5% mismatch tolerance

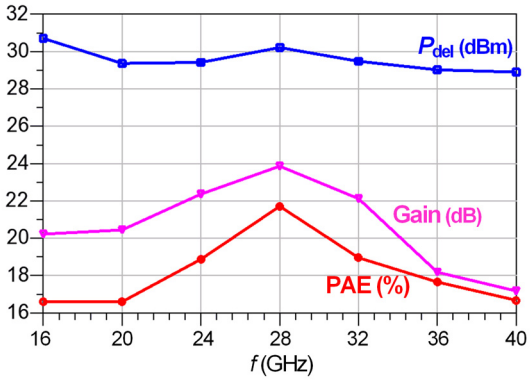

Fig. 6. PA simulation results in the entire frequency band

The overall loss from the output matching and the power combining networks is lower than 2.9dB in the entire frequency band. Simulation results representing the deisgned matching for the combined network of output matching and 4-to-1 combiner is shown in Fig. 5.

Final PA simulation results are shown in Fig. 6 for the entire frequency band. A peak PAE of 21.9%, a peak gain of 23.8dB, and a peak P_{del} of 30.6dBm are achieved.

V. Conclusion

Multi-order transmission line-radial stub networks are designed to perform fundamental and harmonic impedance matching and power combining in a broadband silicon power amplifier. A 1W, 16-40GHz fully-integrated PA is designed that combines the power of 16 single-element PAs. The full PA achieves a peak gain of 23.8dB and a maximum single-ended output power of 30.6dBm with 21.9% PAE. Load-pull simulations are performed for load conditions up to the 5th harmonic. The total loss combined from the output matching and 16-to-1 combining network is less than 2.9dB in the entire frequency band. Employing radial stubs as capacitors with high quality factors at high frequencies enables satisfying optimum load condition for fundamental and harmonic frequencies, simultaneously.

References

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