

Wireless Synchronization of mm-wave Arrays in 65nm CMOS

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Abstract — This paper presents the first wireless synchronization of a mm-wave array, eliminating the need for connecting wires between the array elements. Wireless injection locking is successfully demonstrated and a 3dB bandwidth of 400Hz at a carrier frequency of 50GHz is achieved (frequency stability of 8ppb). The chip includes two on-chip antennas, a power amplifier, a phase-shifter, buffer amplifiers, and a VCO. The chip is fabricated in a 65nm CMOS process and occupies an area of $1.7\text{mm} \times 3.8\text{mm}$.

Index Terms — Wireless synchronization, injection locking, spatial combining, on-chip antennas, mm-wave, CMOS.

I. INTRODUCTION

CMOS-based mm-wave transceivers have received wide attention in recent years. The promise of integrating mm-wave transceivers with low-cost commercial electronics opens up exciting opportunities in many industries such as automotive, medical and security. Both academia [1-2] and industry [3] have shown great progress in the development of mm-wave transceivers. Unfortunately, due to the lack of a locking mechanism, these transmitters were limited to single-chip operation while many applications can benefit greatly from having a multi-chip system with widely-spaced elements. A multi-chip system enjoys advantages of increased transmission power, higher pattern directivity and larger aperture size. The increased transmission power extends the maximum detectable range, while higher directivity increases the angular resolution in imaging radars.

In order to achieve coherency in a multi-chip system, traditional transmitters employ locking through a wired connection, either in the form of a PLL [9] for continuous-wave systems, or a digital trigger signal for pulsed systems [1]. Unfortunately, the wired connections limit the scalability of the array size and are not suitable for building a synchronous array of satellites, UAV or airborne devices. This limitation can be lifted by using a wireless locking signal. In [8], wireless locking was demonstrated through the injection of a free-space optical signal generated by a laser. However, due to the narrow beam width of the laser, the operation angle was extremely limited and the setup required high-precision alignment, making it unsuitable for low-cost, mobile applications. In contrast, mm-wave wireless locking exhibits wider operation angle. In [6], the authors demonstrated the possibility of generating a 1.875GHz

local clock signal using a 15GHz wireless signal. However, the range of operation was limited to a few centimeters, and no radiation or spatial combining was performed. In addition, the issue of self-oscillation in mm-wave locking caused by multi-path and direct feedback needs to be addressed.

In this work, for the first time, the authors present wireless synchronization of a mm-wave array with 8 parts-per-billion (ppb) frequency stability using wireless injection locking. In this design, multi-path feedback is mitigated through orthogonal Tx-Rx radiation efficiencies, and direct feedback is alleviated using orthogonal antenna polarizations. The proposed system enables rapid scaling of the size of an array by eliminating the need for wires to connect to the widely-spaced chips. In addition, the proposed methodology can be used to build an array on a non-planar substrate or on mobile platforms. The concept of the proposed design is illustrated below in Fig. 1.

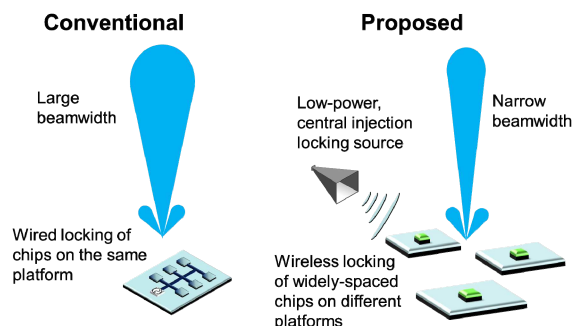


Fig. 1. Traditional wired locking on the same platform vs. proposed wireless locking of widely-spaced chips on different platforms.

II. CIRCUIT DESIGN

A. Architecture

The transmitter architecture is shown in Fig. 2. It consists of a patch antenna at the input that receives the wireless injection signal, a dipole antenna at the output that radiates the locked mm-wave signal, a four-stage power amplifier, a phase shifter, buffer amplifiers, and an injection-locked voltage controlled oscillator. In this design, 100GHz is used as the central injection locking frequency for the purposes of multi-path feedback rejection and higher antenna efficiency. The injected signal is received by an on-chip patch antenna and

amplified by a low noise amplifier by 2.3dB. The amplified signal is injected at the current source of a divider to produce a 50GHz reference signal. This signal is amplified by 12.5dB and passed through a phase-shifter to enable beam-steering. The output power of the phase shifter is amplified by an on-chip power amplifier to 7.8dBm and then coupled to the on-chip dipole antenna.

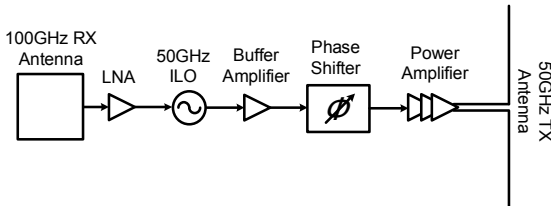


Fig. 2. Transmitter architecture.

B. Orthogonal Antenna Design for the Elimination of Self-Oscillation

As illustrated in Fig. 3, mm-wave signals suffer from multi-path feedback that lead to self-oscillation. We address this issue by designing Tx and Rx antennas that are orthogonal in radiation efficiencies. In this design, a dipole antenna with a total substrate thickness of 430 μ m is selected to radiate efficiently at 50GHz. As shown in Fig. 4, the radiation efficiencies peak at odd harmonics of 50GHz while suppressing most radiation at even harmonics. This is due to the TE surface waves being in phase with the space waves at odd harmonics while being out-of-phase at even harmonics [7]. A simplistic design in which the Tx and Rx antennas are identical would lead to maximum space wave coupling at the frequencies of operation, resulting in a system highly susceptible to multi-path feedback. Therefore, the Rx antenna should be designed to receive efficiently at even harmonics of 50GHz while rejecting incoming signals at odd harmonics. This is achieved by adding an M1 ground plane underneath the receiver antenna to change its effective substrate thickness to 8 μ m. As shown in Fig. 4, the Rx antenna receives efficiently at even harmonics of 50GHz, achieving orthogonality with the Tx antenna.

Direct feedback is another mechanism that causes self-oscillation when the output of the transmitting antenna is coupled to the input of the receiving antenna either through space waves or surface waves. If the feedback is strong enough, the receiver locks to its own transmitter instead of the external synchronization signal, as shown in Fig. 3. To alleviate this issue, a receive patch antenna is used in place of the dipole antenna. This reduces the direct coupling from the transmitter antenna due to the orthogonal polarization of the electromagnetic fields. The E-field of the receiver patch antenna is in the direction of the feed line and therefore perpendicular to that of the transmitter dipole. In addition, the patch antenna has

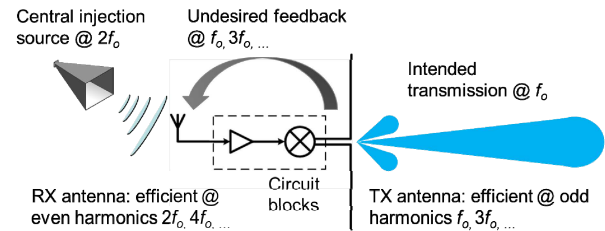


Fig. 3. Illustration of undesired feedback via multi-path.

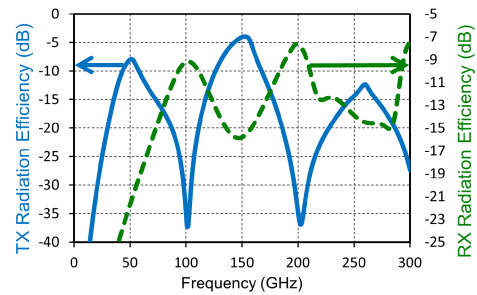


Fig. 4. Simulated radiation efficiencies of the Tx dipole (solid) and the Rx patch antennas (dashed).

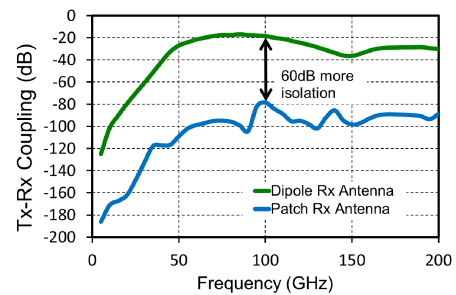


Fig. 5. Reducing the Tx-Rx coupling by using antennas that are orthogonal in polarization.

increased radiation efficiency because the metal loss is reduced. Based on the numerical simulations reported in Fig. 5, it is shown that by using a patch antenna instead of a dipole, the isolation is improved by 60dB at 100GHz. This technique ensures the locking stability of the transmitter system.

C. IL-VCO and LNA

The schematics of the injection-locked VCO and the LNA are shown in Fig. 6. The VCO operates from 51.3 to 52.1GHz and has an output power of -3.5dBm. The varactors are implemented by thin-oxide MOS devices that provide an approximate capacitance of 22fF with a quality factor of about 7. A single-ended LNA is conjugate-matched using single stub transmission lines. It amplifies the 100GHz wireless signal by 2.3dB and injects the signal at the current source of the VCO. A resistor is included in the path of the current mirror to form a high impedance path such that the injected power is directed towards the VCO.

D. Phase Shifter

In order to provide beam-steering, an active current-mode phase shifter with quadrature generation network is implemented, as shown in Fig. 7. A quarter-wave transmission line is used to generate the quadrature signal. In order to prevent reflections, both the I and Q signal paths are first matched to 100 using coupled transmission lines with $Z_0=100$. Then a 50 transmission line matches to the previous buffer amplifier, preventing any reflections at the split junction. The quadrature inputs are fed into the phase shifter, which takes the linear combination of two phases in the current domain. In this active phase shifter, the gain and phase are controlled by weights of each phase. The signal is attenuated by 3dB in this stage, which is compensated by subsequent amplification. Continuous phase-shifting is achieved by tuning analog voltages V_{b_0} , V_{b_90} , V_{b_180} , and V_{b_270} , as shown in Fig. 7.

E. Power Amplifier

The final stage of the transmitter is the four-stage amplifier shown in Fig. 8. The PA is designed with inter-stage matching using coupled transmission line stub structure. In order to improve the stability of the high-quality factor resonant structures, several measures are taken. First, a parallel RC tank is placed in series with the signal path that acts as a high-pass filter to improve stability in the GHz range. In addition, biasing resistors are used at the gate to reduce the quality factor. The PA achieves 11.5dB gain, 10.8dBm output power and 5.5% PAE.

III. MEASUREMENT RESULTS

The chip was designed and implemented using IBM's 65nm bulk CMOS technology. The size of the chip including the on-chip antenna and the bondpads is 1.7mm \times 3.8mm. The chip micrograph and the measurement setup are shown in Fig. 9. It consumes a total of 330mW. Measurements of the VCO were performed using OML's V-band harmonic mixer and standard-gain horn antenna WR-15 M15RH. The tuning voltage was varied from 0 to 1.6V, and the observed oscillation frequency ranged from 51.3 to 52.1GHz, demonstrating a tuning range over 800MHz. The maximum detectable distance between the chip under test and the receive horn antenna without lens was 100cm. Accounting for the respective mixer and cable losses of 40dB and 3.5dB, the calibrated received power was -51.5dBm. As a result, -5dBm radiated power was calculated using the Frii's formula.

In order to demonstrate wireless injection locking, an Anritsu 68369B signal generator was used in conjunction with Millitech's AMC-10-RFHB0 x6 multiplier and a

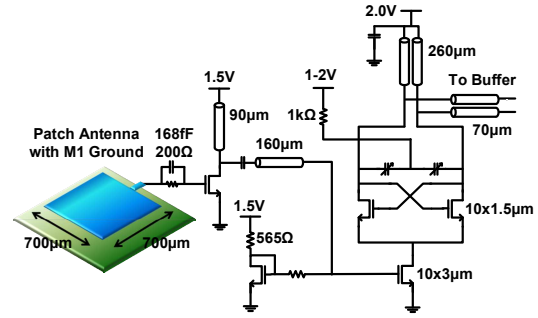


Fig. 6. Schematic of the injection-locked receiver (biasing not shown).

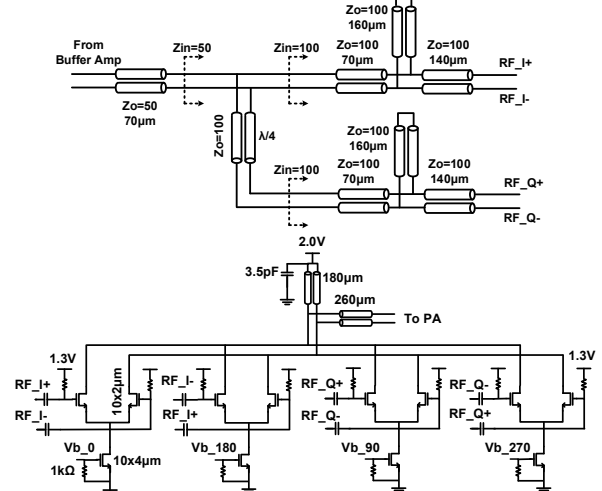


Fig. 7. Schematic of the quadrature generator and the phase interpolator.

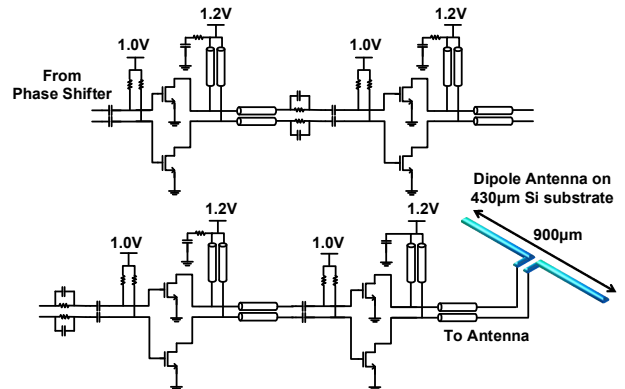


Fig. 8. Schematic of the 4-stage PA and the dipole antenna.

W-band, pyramidal horn antenna SGH-10-RO to inject the locking signal to the chip. The output power of the multiplier was 10dBm. The distance of the horn antenna and the chip was about 5cm. The simulated gain of the patch antenna at $(45^\circ, 0)$ is -7.7dBi. From the Frii's formula, the received power injected at the VCO is calculated to be -24dBm. Figure 10 shows the spectrum of the VCO in the free-running and injection-locked modes.

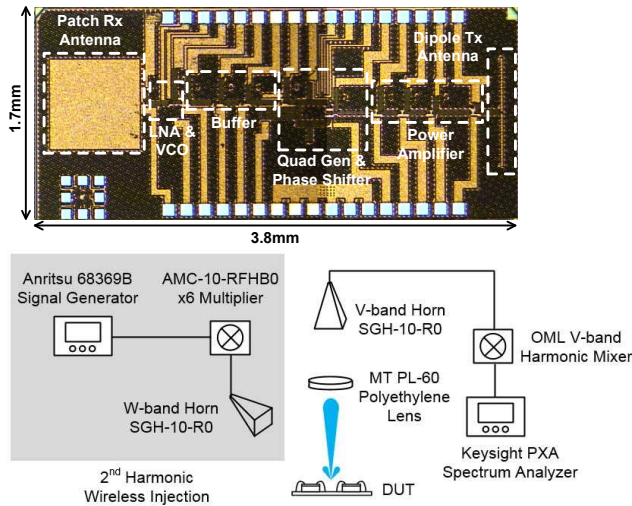


Fig. 9. Top: Chip micrograph. Bottom: Measurement setup.

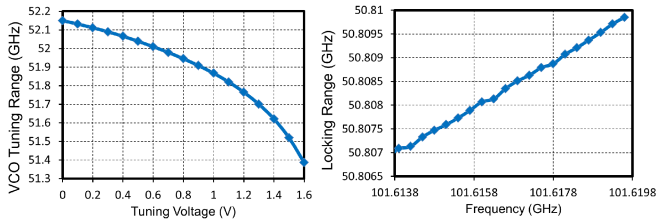
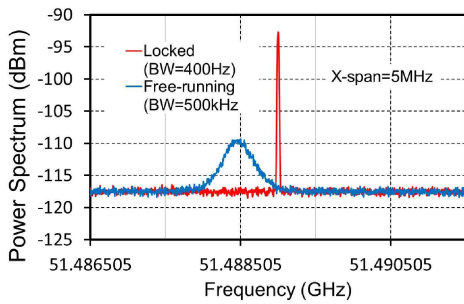


Fig. 10. Top: Spectrum of free-running vs. injection-locked transmitter. Bottom: VCO tuning and injection-locking range.

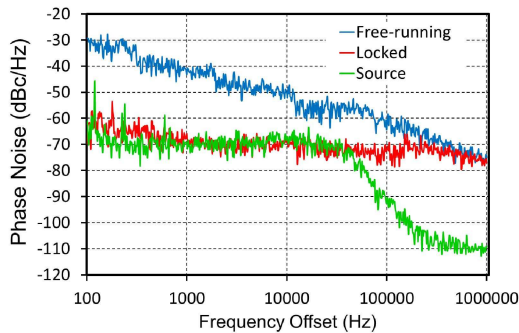


Fig. 11. Phase noise measurement results.

Based on this measurement, the 3dB bandwidths of the locked and unlocked signals are 400Hz and 500kHz, respectively. The VCO tuning range and the injection locking range are also shown in Fig. 10. The VCO

frequency is exactly half of the injected frequency, demonstrating successful wireless locking. The locking range of the transmitter is $>3\text{MHz}$. Figure 11 shows the phase noise measurements of the free-running transmitter, the locked transmitter and the signal generator. The phase noise is significantly reduced upon injection of the wireless signal, enabling rapid scaling of the transmitter array.

IV. CONCLUSION

In this work, wireless synchronization of a mm-wave array with 8ppb accuracy is reported for the first time. Wireless injection locking results in a 3dB bandwidth of 400Hz at a carrier frequency of 50GHz. The chip is implemented in IBM's 65nm bulk CMOS process and occupies an area of 6.5mm^2 . This work enables scaling an array without physical wires and may be used to lock transmitters that are not in proximity of each other.

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