A Wirelessly Powered Injection-Locked Oscillator with On-Chip Antennas in 180nm SOI CMOS

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Abstract — This paper presents a battery-less mm-sized wirelessly powered injection-locked oscillator with on-chip antennas in 180nm SOI CMOS. The chip harvests electromagnetic radiation from a continuous-wave source in the X-band using an on-chip antenna. In addition, the chip is equipped with a broadband injection-locking oscillator that locks to the frequency of the input and produces a synchronized signal at the half frequency of the input. The new signal is then radiated back using an on-chip dipole antenna. This architecture resolves the conventional self-interference issue in RFID sensors by separating the received and transmitted frequencies. In addition, the locking mechanism improves the phase-noise of the on-chip oscillator to -93dBc/Hz at 100Hz offset.

Index Terms — Wireless Power, Energy Harvesting, On-chip Antenna, Sub-harmonic Injection Locking, RFID, Battery-less Sensor.

I. INTRODUCTION

Recently, there has been a growing interest in Internet of Things (IoT), wireless sensor network (WSN), and implantable devices. In these applications, a battery-less, small footprint, low-cost microchip is important for the prevalence of the technology. Conventional battery-less sensors capture the electromagnetic energy with an external antenna and convert it to DC power. These sensors typically operate in the sub-gigahertz frequency regime and require large external antennas with an area exceeding ~10cm^2 area. This limitation severely limits the miniaturization of the device and causes complex packaging issues and increased cost. In order to shrink the size of the antenna and integrate it with the energy-harvesting circuits, the operation frequency must increase. In this paper, we report the first wirelessly powered injection-locked oscillator with on-chip antennas operating in the X-band. The integration of the antennas dramatically reduces the overall chip size to millimeter level.

In addition to integration of on-chip antennas, the reported chip uses a novel topology to improve the phase-noise and resolve the self-interference issue. In conventional RFID systems, frequency division or time division duplexing is applied to mitigate self-interference issue but, in these systems, the transmitted signal is not locked to the received signal [1-3]. Due to the free-running nature of the transmitted signal, the RFID reader should use a large measurement bandwidth, which increases the noise-floor and reduces the sensitivity of the measurement system. This issue can be resolved by using a PLL-based architecture, but this requires high power, and occupies a large area [4]. Other groups used the technique of injection locking with wired input [5] or large off-chip antennas to capture injection-locking signal [6-7].

The reported chip integrates a sub-harmonic injection locked block with on-chip antennas and energy-harvesting circuit to reduce the size of the entire system to 2.47 mm^2.

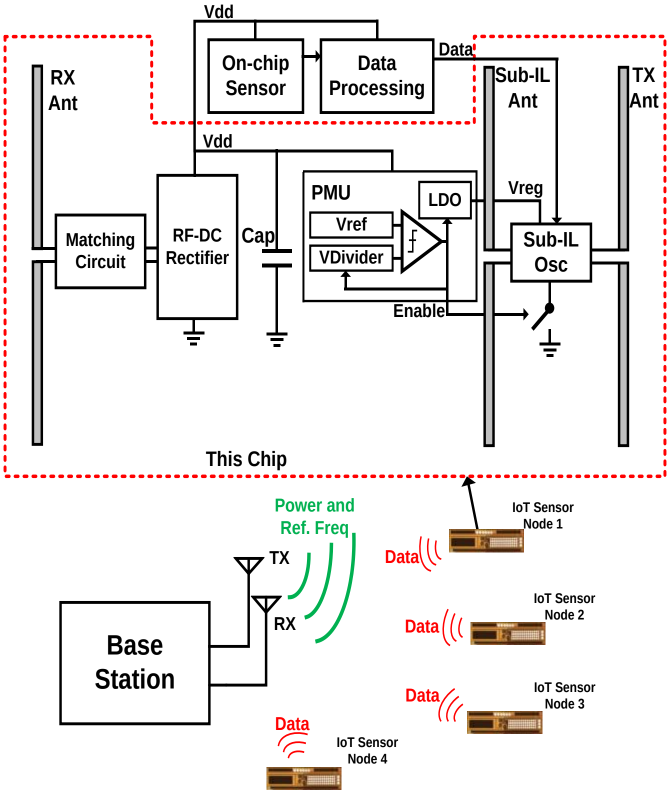

Fig. 1 IoT sensor network concept and block diagram of proposed chip for IoT sensor node.

II. BLOCK DIAGRAM AND DESIGN DETAILS

Figure 1 shows the block diagram of the reported chip for IoT sensor node. It consists of two RX and one TX on-chip antennas, a power-harvesting rectifier circuit, a power management unit (PMU), and a sub-harmonic injection-locked (Sub-IL) LC oscillator.

The on-chip antenna receives the incoming electromagnetic power, and feeds it to the power-harvesting rectifier circuits. The power is rectified and stored on the on-chip capacitor. The PMU unit continuously monitors the voltage on a storage capacitor and turns the transmitter circuit on after the chip scavenges and stores enough energy on the capacitor. When the voltage on the storage capacitor reaches 1.6V (Vhigh), the sub-harmonic injection-locked oscillator turns on and locks to the input signal, which can range from 8GHz to 10GHz. The oscillator generates a signal at half frequency (4GHz to 5GHz), and radiates it back using on-chip antennas. This event discharges the storage capacitor. When the capacitor voltage drops to 1.2V (Vlow), the PMU turns the oscillator off and chip enters the sleep mode. The PMU is composed of a voltage reference, a comparator, a divider and a Low Dropout Regulator (LDO). The whole PMU consumes less than 200nA in sleep mode. After enough energy is stored on the capacitor, the PMU enables the LDO and the sub-harmonic injection locked oscillator. The LDO generates a stable supply voltage of 0.8V for the sub-harmonic injection locked oscillator. At this supply level, the oscillator generates -25dBm power to TX on-chip antenna.

In this design, three on-chip dipole antennas with length of 3.8mm are utilized. The first RX antenna is used at the input of the rectifier, to harvest the incident RF electromagnetic power. By increasing the operating frequency, the antenna gain increases but the power conversion efficiency of the rectifier circuit drops. Considering this trade-off, an optimum operating frequency of 9GHz is achieved. To alleviate the matching issues at the input of the rectifier, a dedicated dipole antenna is used at the input of the rectifier and a second dipole antenna is connected to the input of the sub-harmonic injection-locking oscillator. The third dipole antenna is implemented at the output of the Sub-IL transmitter. The dipole antennas achieve a radiation efficiency of 5% at 4.5GHz and 21% at 9GHz.

The power-harvesting rectifier circuit consists of 10 Dickson stages. A 3.4nH inductor is used at the input to resonate with the dipole antenna and maximize the amplitude of the input voltage. To achieve a DC voltage of 1V on a 1.1nF MIM storage capacitor, a minimum input power of -16.1dBm is required. At this input power level, a conversion efficiency of 7% at 9GHz is achieved.

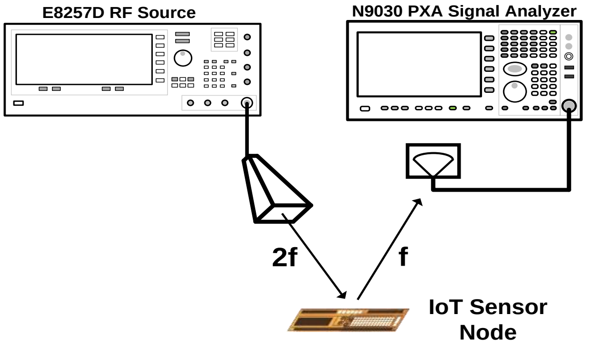

Fig.2 Wireless test setup.

III. MEASUREMENT RESULT

Figure 2 shows the measurement setup. A Keysight E8259D signal generator and a commercial MACOM PA transmit a 40dBm EIRP X-band signal through a horn antenna. The chip receives the signal and radiates back a locked signal at the half frequency. This signal is captured by a custom PCB-based antenna, which is connected to a Keysight PXA N9030A spectrum analyzer.

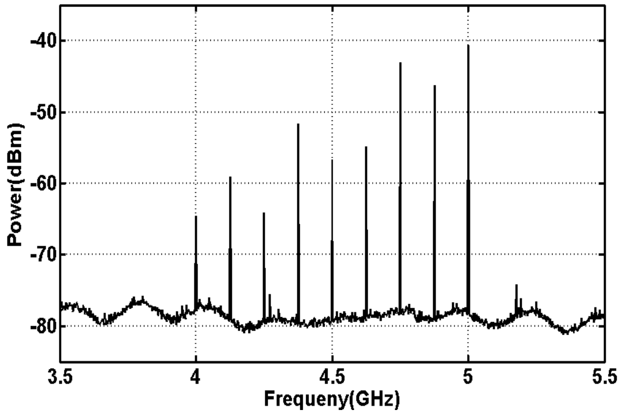

Fig.3 Wide frequency of operation in sub-harmonic injection locked mode. Input frequency is varied from 8GHz to 10GHz.

In this experiment, the chip is placed 1.5cm away from the TX horn antenna. At this distance, by using a source with an EIRP of 40dBm, the IL oscillator successfully locks to the input signal within a frequency range of 8-10GHz. This represents a locking range of 22% (shown in Figure 3).

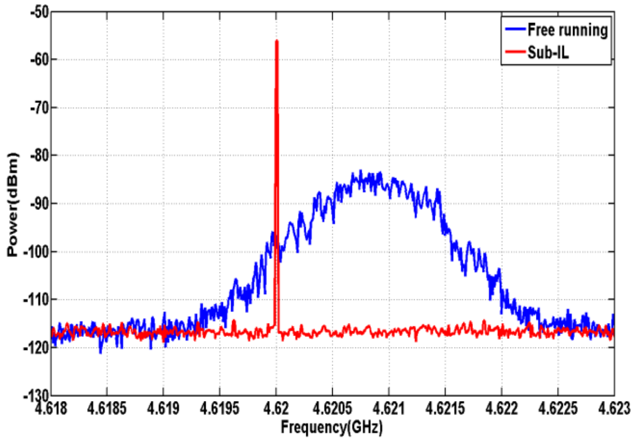

Fig.4 Spectrum of the radiated signal by the chip in both free-running and sub-harmonic injection locked modes.

Figure 4 shows the spectrum of the oscillator in free running and locked modes. Figure 5 shows the phase noise in the locked mode, which is about -93dBc/Hz at 100Hz offset. The phase noise follows the phase noise of the RF source at low offset. It flattens out at higher offset because of the limitation of the test instrument. At 8.9GHz, a maximum harvesting range of 4.2cm is achieved while the base station is transmitting 40dBm of EIRP.

Table I. Performance Comparison

	[1]	[3]	[4]	[6]	[7]	This Work
Process	90nm	65nm	90nm	130nm	250nm	180nm
RX Frequency [GHz]	45	71	0.902 to 0.928	0.918	0.45	**8 to 10**
TX Frequency [GHz]	60	79	2.405 to 2.475	0.306	0.9	**4 to 5**
Topology	FRLC	FRLC	PLL-based	ILRO	ILLC	ILLC
Wireless Test?	No	No	No	Yes	Yes	**Yes**
Measured Distance	N.A.	N.A.	N.A.	1.3m with 35dBm EIRP source	1.65m with 17.5dBm EIRP source	**4.2cm** with 40dBm EIRP source
Fully Integrated?	No (no ant)	No (only RX ant)	No (no ant)	No (off-chip ant)	No (off-chip ant)	**Yes**
Active Area	1.235mm^2	1.09mm^2	1.54mm^2	0.85mm^2	<1mm^2	**0.25mm^2**
Area with Antenna	N.A.	1.79mm^2 (only RX ant)	N.A.	>9.8cm^2	N.A. (est. 15cm monopole ant)	**2.47mm^2**
Phase noise	N.A.	N.A.	-93dBc/Hz @10kHz	N.A.	-99.1dBc/Hz @10kHz	**-93dBc/Hz @100 Hz**

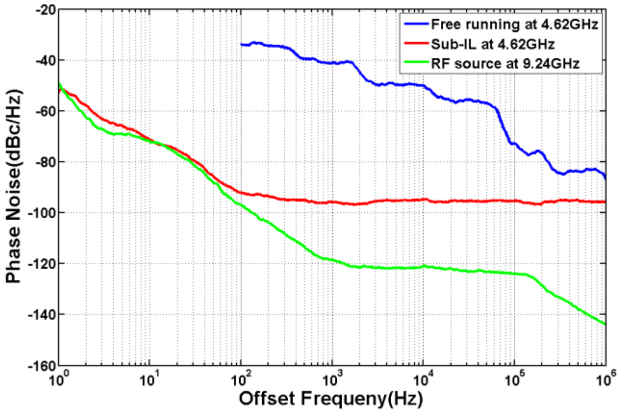

Fig.5 Phase noise log-plot of RF source, free-running and injection-locked LC oscillator. Phase noise of 9.24GHz is reduced by 6dB to make a fair comparison with the generated 4.62GHz locked clock.

The chip is fabricated in an 180nm CMOS SOI process and occupies an area of 3.8×0.65 mm^2, including the on-chip antennas and storage capacitor. The die photo of the chip is shown in Figure. 6.

IV. CONCLUSION

We present a 2.47mm^2 fully integrated wirelessly powered microchip that includes an energy-harvesting circuit, power management unit, sub-harmonic injection locked oscillator, and on-chip receiving and transmitting antennas. The chip achieves a maximum operating distance of 4.2cm, a locking range of 22%, and a phase noise of -93dBc/Hz at 100Hz offset.

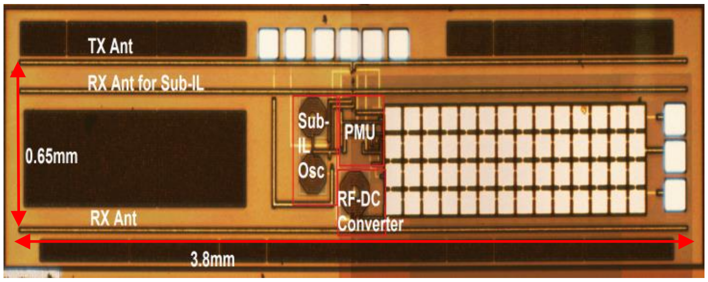

Fig.6 Die micrograph.

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