Picosecond Digital-to-Impulse Generator in Silicon

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***Abstract*—In this paper, a direct digital-to-impulse architecture is presented that generates impulses with a measured record pulse-width of shorter than 8psec and an output peak power of 6mW. It is shown that the timing of the generated impulses can be locked to the edge of an input trigger with a high timing accuracy. It is also shown that the peak amplitude of the impulses can be programmed. In addition to time-domain measurements, frequency-domain spectrum is measured from DC to 75GHz. At 75GHz, the generated impulses have a frequency stability of better than 4Hz at 20dB below peak. The impulse train also achieves a timing jitter of better than 240fsec. The chip is fabricated in a 130nm SiGe BiCMOS process.**

***Index Terms*—Direct Digital-to-Impulse (D2I) Architecture, Picosecond Impulse Generation, Terahertz, Millimeter-Wave, SiGe, BiCMOS, Silicon.**

I. Introduction

In the last decade, extensive research in generation and radiation of continuous-wave (CW) signals with silicon-based technologies have been introduced. Although these systems have achieved power generation at sub-THz frequencies, they have a limited bandwidth and cannot produce short pulses required for many applications such as broadband THz spectroscopy, high-resolution 3D radar imaging, high-speed wireless communication, and precision time/frequency transfer. The pulses must be short in time and have a large peak power. In a 3D imaging system, the pulse-width determines the depth resolution and the peak power limits the transmission range. To accomplish these requirements in silicon, a novel architecture is required to generate broadband, picosecond pulses.

Impulse generation techniques can be divided into two main categories. In the first category, a CW signal is generated on-chip and a switch is used to modulate the amplitude of the CW and convert it to a train of short impulses. The shortest radiated impulse reported with this method is 26psec, which was based on a noisy envelope of the radiated signal [1]. The second category is based on the technique of direct digital-to-impulse (D2I) radiation, which was introduced in [2-3], for the first time. In this technique, no on-chip oscillator was used. Instead, a fast trigger signal is generated and used to release the DC energy stored in a broadband on-chip antenna. In [2], radiation of 9-psec impulses using an on-chip differential inverted-cone antenna was reported. In [3], 8-psec impulses were radiated using an on-chip slot bow-tie antenna. The work in [2-3] was based on releasing the stored energy in an energized antenna structure. In [2-3], pulse-width and peak power of the radiation were limited to bandwidth, group delay variation, and inductance of the antenna.

In this work, a digital-to-impulse generator is reported in silicon that generates picosecond impulse signals delivered to a 50Ω-load based on a low-power digital trigger input. The impulse generator includes a fast trigger generation block, an edge-sharpening power amplifier, a cascode current-switch and an impulse matching network. This oscillator-less topology achieves a pulse-width of 8psec, a peak power of 6mW, and a repetition rate up to 10GHz. The generated impulses are locked to an external digital trigger with timing jitter of better than 240fsec. This low level of timing jitter along with the direct digital-to-impulse architecture, enables coherent combining from multiple chips.

II. Circuit Architecture

The block diagram of the impulse generator is shown in Fig. 1. A digital trigger signal with a rise time of 120psec is fed to the input of the circuit. A set of cascaded digital buffers reduces the rise time to 30psec and sends the signal to an edge-sharpening power amplifier (PA) for further amplification. The edge-sharpening PA sharpens the rise time to 20psec and amplifies the signal to drive the cascode current switch stage. A transmission line - capacitor based impulse-matching network is energized by storing a DC current. When the switch is turned off by the PA, the current stored in the pulse matching network generates picosecond impulses that are coherent with the input trigger. The broadband impulse-matching network is optimized to maximize the stored energy while minimizing the duration of each impulse and cancelling ringing. Fig. 1 shows the circuit schematic of the impulse generator.

The impulse generator has two modes of operation. In the first mode, a positive impulse is generated which is locked to the rising edge of the input trigger. In the second mode, a negative impulse is generated that is locked to the falling edge of the trigger. One or both of these modes can be activated by controlling the biasing node V_3. In addition, biasing node V_2 can be used to modulate the amplitude of the generated impulses.

A distributed network of capacitors at the biasing points ensures fast delivery of electrical charges to the base node of transistor Q_3. A cascode topology is selected for the current switch to avoid ringing in the signal caused by the

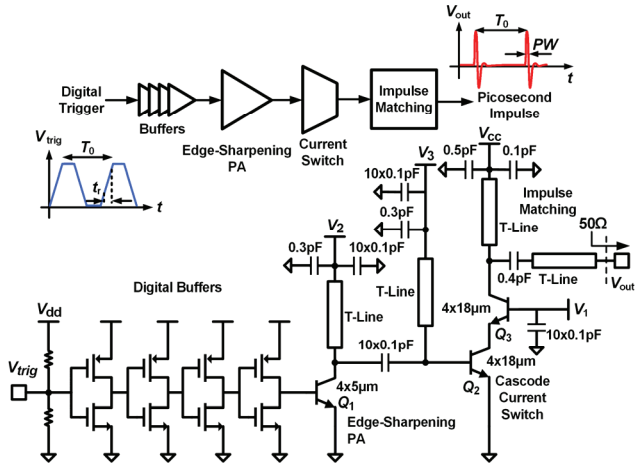

Fig. 1. Schematic of the digital-to-impulse generator

Miller effect. The matching transmission lines are fabricated using aluminum layers M6 and M7.

III. Measurement Results

The impulse generator is designed to deliver ultra-short impulses to a 50Ω external load. To perform time-domain and frequency-domain measurements, a GGB 67-GHz GSG-type probe is used to connect the output of the circuit to measuremnt equipment. The input trigger is fed to the chip via bond wires. The measurement set-up is shown in Fig. 2. To acquire time-domain waveforms, the probe is connected to an Agilent 86118A sampling head using a 1.85mm coaxial cable. Frequency-domain measurements are performed in two steps. First, DC to 50GHz frequency components are measured by directly connecting the output of the probe to input of an Agilent N9030A PXA analyzer. Second, the output of the probe is connected to a coaxial to WR-15 waveguide adapter and 50GHz to 75GHz components are measured by an OML WR-15 harmonic mixer and the signal analyzer. Fig. 3 shows the measured time-domain signal and frequency-domain power spectrum of the impulse generator with 3-GHz repetition rate.

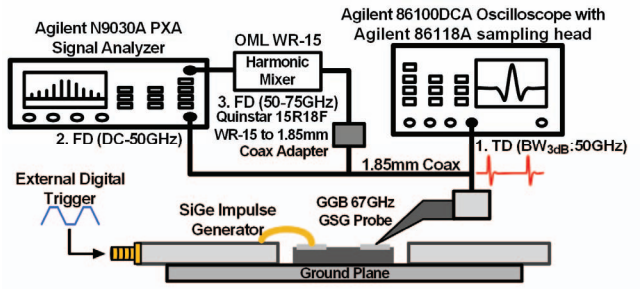

Fig. 2. Measurement set-up

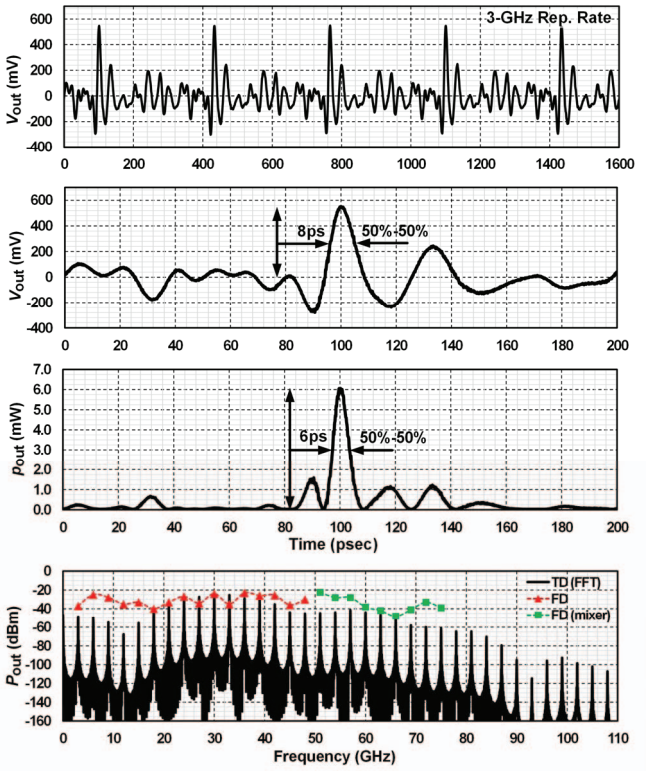

Fig. 3. Measured time-domain waveforms by the sampling oscilloscope (a 20-dB attenuation used for avoiding signal clipping in the oscilloscope is de-embedded). Output power spectrum calculated by both time-domain (TD) and frequency-domain (FD) measurements (the mixer loss is de-embedded in the 50GHz to 75GHz FD measurement)

To demonstrate amplitude modulation capability, the peak voltage of the output signal is modulated from zero to its maximum value using the node voltage V_2. Fig. 4 shows the peak amplitude against V_2. In this experiment, the shape of the measured waveform was not changed and only the amplitude was modulated.

The precision synchronization of the digital trigger with the generated impulses makes it possible to perform coherent combining with multiple chips. To demonstrate precision timing control of the generated impulses, the input trigger of the chip is delayed and the resulting delay in the impulse is measured. The digital trigger is provided by Tektronix

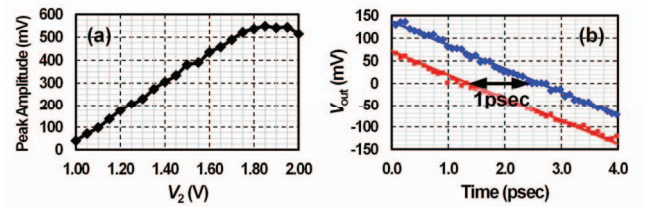

Fig. 4. (a) Modulation of the impulse peak amplitude (b) Two generated impulses delayed by 1psec

TABLE I
COMPARISON TABLE

	This work	[1] JSSC 2010	[2] RFIC 2014	[3] IMS 2014	[4] JSSC 2014
Shortest Pulse-Width	**8psec**	26psec	9psec	8psec	100psec
Pulse Peak Power	**7.8dBm**	N/A	7dBm (10dBm EIRP)	5dBm (13dBm EIRP)	4dBm/TX (array)
Phase Synchronization with an External Reference	**Yes**	No	Yes	Yes	No
Programmable Peak Amplitude	**Yes**	N/A	N/A	N/A	N/A
Time-Domain Measurements	**Yes (with locking)**	Yes (without locking)	Yes (with locking)	Yes (with locking)	No
Frequency-Domain Measurements	**Yes**	Yes	Yes	Yes	Yes
Pulse Generation Method	**Digital-to-Impulse**	Oscillator-based	Digital-to-Impulse	Digital-to-Impulse	Oscillator-based
Power Consumption	**140mW**	739mW	260mW	220mW	1.2W
Technology	**0.13µm SiGe**	0.13µm SiGe	0.13µm SiGe	0.13µm SiGe	65nm CMOS
Die Area	**0.38mm^2**	1.2mm^2	0.88mm^2	0.47mm^2	20mm^2

Arbitrary Waveform Generator AWG7000, which has a 1-psec resolution timing control for the digital trigger signal. Fig. 4 shows zoomed time-domain signals generated by two different delay values.

The timing jitter of the generated impulse train is calculated by the Agilent sampling oscilloscope 86100DCA. Fig. 5 shows an RMS jitter of 240fsec, which is measured by an averaging of 64. The measured RMS jitter with averaging of 128 and 256 is 210fsec and 140fsec, respectively. In addition to the timing jitter, the frequency stability of the generated frequency-comb is measured by the signal analyzer. Based on the measured spectrum, 99.8% of the power of the 75GHz frequency component is concentrated between frequencies 75,000,000,078Hz and 75,000,000,082Hz, which is only 4Hz (Fig. 5). This high level of frequency stability is essential in implementing precision frequency-domain spectroscopy systems.

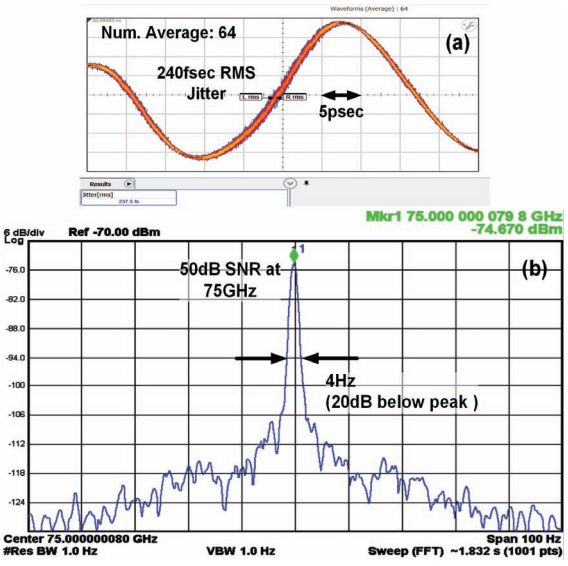

Fig. 5. (a) Jitter of the generated impulses (b) Un-calibrated power spectrum around 75GHz. 99.8% of the 75GHz tone power is confined in less than 4Hz frequency range

To the best of the Authors' knowledge, this is the first coherent impulse-generator chip that can generate and deliver high power sub-8psec impulses to a 50Ω load. Table I compares the specifications of the reported chip with the prior art. The chip was fabricated in a 130nm SiGe BiCMOS process technology. The size of the chip, including the pads, is 700µm × 550µm. A micrograph of the chip is shown in Fig. 6.

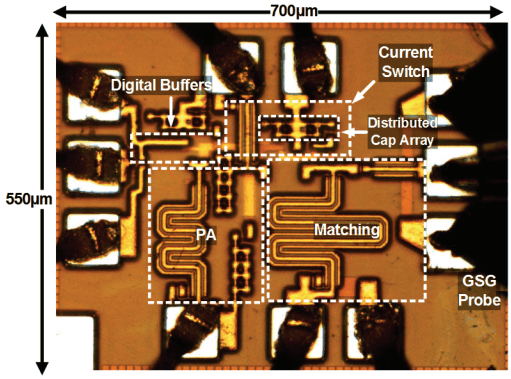

Fig. 6. Micrograph of the chip.

ACKNOWLEDGMENT

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