ELEC 422 **Fall 1997**
Handout # 1 September 2, 1997

VLSI Design I

Information Sheet

This is an introductory course on VLSI design. While the goals of the course are ambitious –covering the theory of VLSI design *and* successfully designing a chip– this could also be the most fun you ever had in any engineering course. Welcome!

Instructor:	Joe Cavallaro
Contact Info:	527-4719, cavallar@ece.rice.edu
Text:	Weste and Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley *VLSI Design I packet* (available at Rice Campus Store)
Time & Location:	Tuesdays and Thursdays 2:30-3:50pm, Abercrombie A126
Lab Assistant:	Suman Das, extension 2899, suman@ece.rice.edu

Course Outline

- Review of combinational logic, Introduction to CMOS circuit elements
- Sequential logic, clocking, finite state machines, PLA's
- Overview of MOS Transistor physics
- The CMOS process, layout design rules
- Hierarchical design, design capture and verification
- CMOS circuit design, fanning, clock distribution, I/O
- Circuit parameters, timing, and performance (delay/size/power)
- "Other" CMOS structures: BiCMOS, dynamic logic, ...
- Testing and testability

Grading

You will be evaluated based on homeworks (HW), a midterm test (MT) and the term project (TP). There is no final exam.

$$Grade = 0.5\,TP + \max\{(0.3\,MT + 0.2\,HW), (0.25\,MT + 0.25\,HW)\}$$

Other useful information

1. Students are **required** to enroll in Elec423 (VLSI Design II) during Spring 1998. This is due to contractual obligations with the MOSIS fabrication service, to provide a report on the success of the fabricated chip.
2. The chip fabrication project is a group effort. Students will work on the project in groups of three. However, each individual must have well-defined responsibilities within the group, to be reflected in the final project report.
3. The project is the defining core of this course. Short term goals and deadlines specified in the accompanying handout are intended to help you in project time management. Meeting these individual short term deadlines is mandatory.

4. Homeworks are designed to help you assimilate the material and also to prepare you for the design process in your project. Homeworks are not pledged, and you are encouraged to discuss the problems. You may help one another through a discussion of methods and approaches to solving the problems. However, the homework that you submit must be entirely your own product, in the sense that it should not, even in part, contain exact copies of (whole or part of) solutions from other students, or from previous year(s), or text, graphs, plots, tables, data and/or computer files taken from any source.
5. Handouts and on-line examples will be provided to assist you in learning the software tools needed for the homeworks (and project).
6. Late homeworks will not be accepted. Final design of the chip is due Tuesday December 10, and cannot be extended. Final project report is due later in the examination period.
7. The midterm exam will be scheduled to take place in mid November.
8. Office hours will be set for regular meetings of the research groups.

Supplemental Reading

1. Mead and Conway, *Introduction to VLSI Systems*, Addison Wesley
2. Peterson and Hill, *Introduction to Switching Theory and Logical Design*, John Wiley
3. Streetman, *Solid State Electronic Devices*

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