Elec 422: VLSI Design I

Notes on Decoder and ROM PLA Tools

Fall 1998, November 10, 1998

Use of MPLA to generate ROMS

You have used the *platool* shell script to design the PLA's in your projects. It uses the most recent PLA template, /usr/site/cad/lib/mpla/p-SCS3cisnew.mag. The final PLA generator, *mpla*, can be used to make simple decoders and ROMS as in the following example:

```
mpla -s SCS3cisnew decode.mpla
```

Note: Please use one of the SunOS Owlnet machines, for example great-gray.owlnet.rice.edu, for running platool and its associated component programs. There are difficulties in using machines running Solaris.

The output will be put in a file, *decode.mag*. The default PLA template p-SCS3cisnew.mag can be viewed through *magic*. Sections of it are assembled by *mpla* to form the layout. With this set of options there are no latches at the inputs or outputs and a combinational circuit is produced.

MPLA example for decoder

The following decoder is written as direct input to *mpla*. When we used *meg* for state machines with *platool* this file format was passed through the pipe between *eqntott* and *mpla*.

```
#
# Mpla input file
# 2 line to 4 line decoder
#
.na 2-4decode
.ilb msb lsb
.olb three two one zero
.i 2
.o 4
.p 4
00 0001
01 0010
10 0100
11 1000
.e
```

The .na command gives a name to the PLA. The .ilb command gives the *magic* labels for the inputs from left to right. The .olb command gives the *magic* labels for the outputs from left to right. The .i command lists the number of input signals. The .o command lists the number of output signals. The .p command lists the number of product terms, in this case four. The next four lines list the product terms with the inputs on the left and the outputs on the right, for example the line 10 0100 tells the PLA to output 0100 (decoded line two) when the input 10 (binary encoded two) is received. Finally, the .e command is a simple end of file command. Please note that the above syntax needs to be followed closely since *mpla* assumes that its input file was written automatically by *eqntott*. In particular, it has been noticed that extra "white space," such as blank lines and extra space between keywords, can cause input error messages.

On the following pages are a plot of the decoder and *irsim* input and output files.

```
| Irsim Test Vector for decode
| two to four line decoder generated by mpla

| Watch nodes
ana msb lsb three two one zero

| Since irsim needs a clock while the decoder is a combinational circuit,
| we will use a dummy clock signal just to keep irsim happy.
clock Vdd 1

|  cycle the input nodes "msb" and "lsb" through a sequence of 1s and 0s
V msb  0 0 1 1 0 0 0 0 1 0
V lsb  0 1 0 1 0 0 1 0 0 0

| Simulate the circuit for this sequence of inputs
R

| units: 100 tech: scmos
p GND Vdd 6_44_11# 4 3 18 -5
n 6_88_97# GND 6_44_11# 2 3 50 -6
n 6_120_97# GND 6_44_11# 2 3 66 -6
n 6_44_11# GND 6_222_239# 2 3 115 -3
p GND Vdd 6_44_27# 4 3 18 -13
n 6_88_97# GND 6_44_27# 2 3 50 -14
n 6_112_139# 6_44_27# GND 2 3 58 -14
p GND Vdd 6_44_43# 4 3 18 -21
n 6_80_139# 6_44_43# GND 2 3 42 -22
p GND Vdd 6_44_59# 4 3 18 -29
n 6_80_139# 6_44_59# GND 2 3 42 -30
n 6_80_139# GND 6_88_97# 2 3 42 -48
n 6_44_27# 6_208_215# GND 2 3 107 -11
n 6_120_97# GND 6_44_43# 2 3 66 -22
n 6_44_43# GND 6_190_239# 2 3 99 -19
n 6_112_139# 6_44_59# GND 2 3 58 -30
```

```
n 6_112_139# GND 6_120_97# 2 3 58 -48
n 6_44_59# 6_176_215# GND 2 3 91 -27
p GND Vdd 6_176_215# 4 4 89 -51
p GND Vdd 6_190_239# 4 4 97 -51
p GND Vdd 6_208_215# 4 4 105 -51
p GND Vdd 6_222_239# 4 4 113 -51
n msb 6_80_139# GND 2 3 40 -64
n lsb 6_112_139# GND 2 3 56 -64
p 6_80_139# Vdd 6_88_97# 2 5 46 -90
p 6_190_239# Vdd two 2 3 97 -78
p 6_112_139# Vdd 6_120_97# 2 5 62 -90
p 6_176_215# three Vdd 2 3 92 -85
p msb Vdd 6_80_139# 2 5 42 -101
p lsb Vdd 6_112_139# 2 5 58 -101
n 6_176_215# GND three 2 3 90 -107
p 6_222_239# Vdd zero 2 3 113 -78
p 6_208_215# one Vdd 2 3 108 -85
n 6_208_215# GND one 2 3 106 -107
n 6_190_239# GND two 2 3 97 -119
n 6_222_239# GND zero 2 3 113 -119
C one GND 33
C zero GND 29
C three GND 33
C two GND 29
C lsb GND 12
C msb GND 12
C 6_176_215# GND 42
C 6_190_239# GND 44
C 6_208_215# GND 42
C 6_44_59# GND 46
C 6_80_139# GND 45
C 6_44_43# GND 48
C 6_112_139# GND 47
C 6_44_27# GND 37
C 6_120_97# GND 43
C 6_222_239# GND 45
C 6_88_97# GND 43
C 6_44_11# GND 52
C Vdd GND 305
```

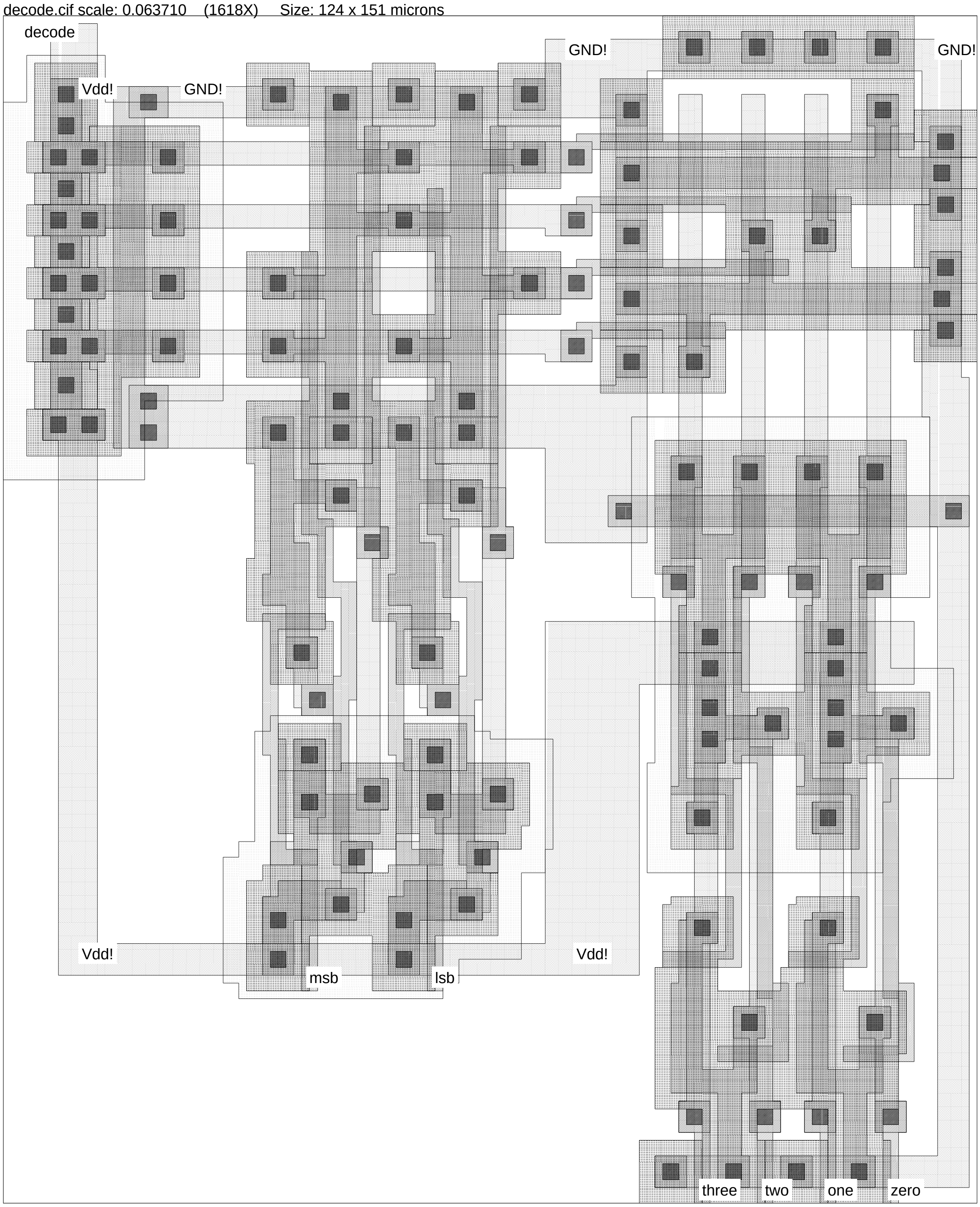

Figure 1: Magic layout of decoder circuit.

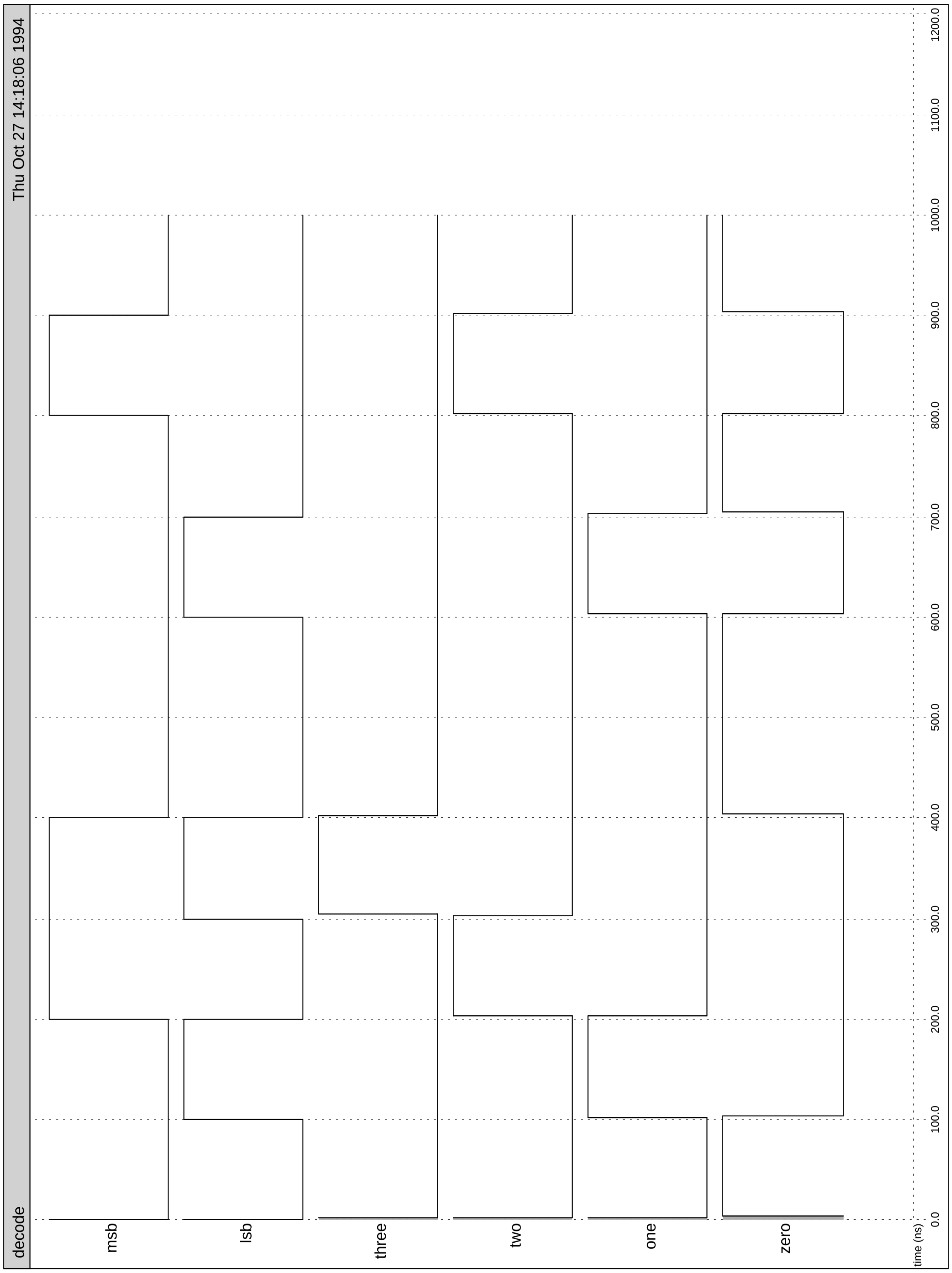

Figure 2: IRSIM simulation of decoder.