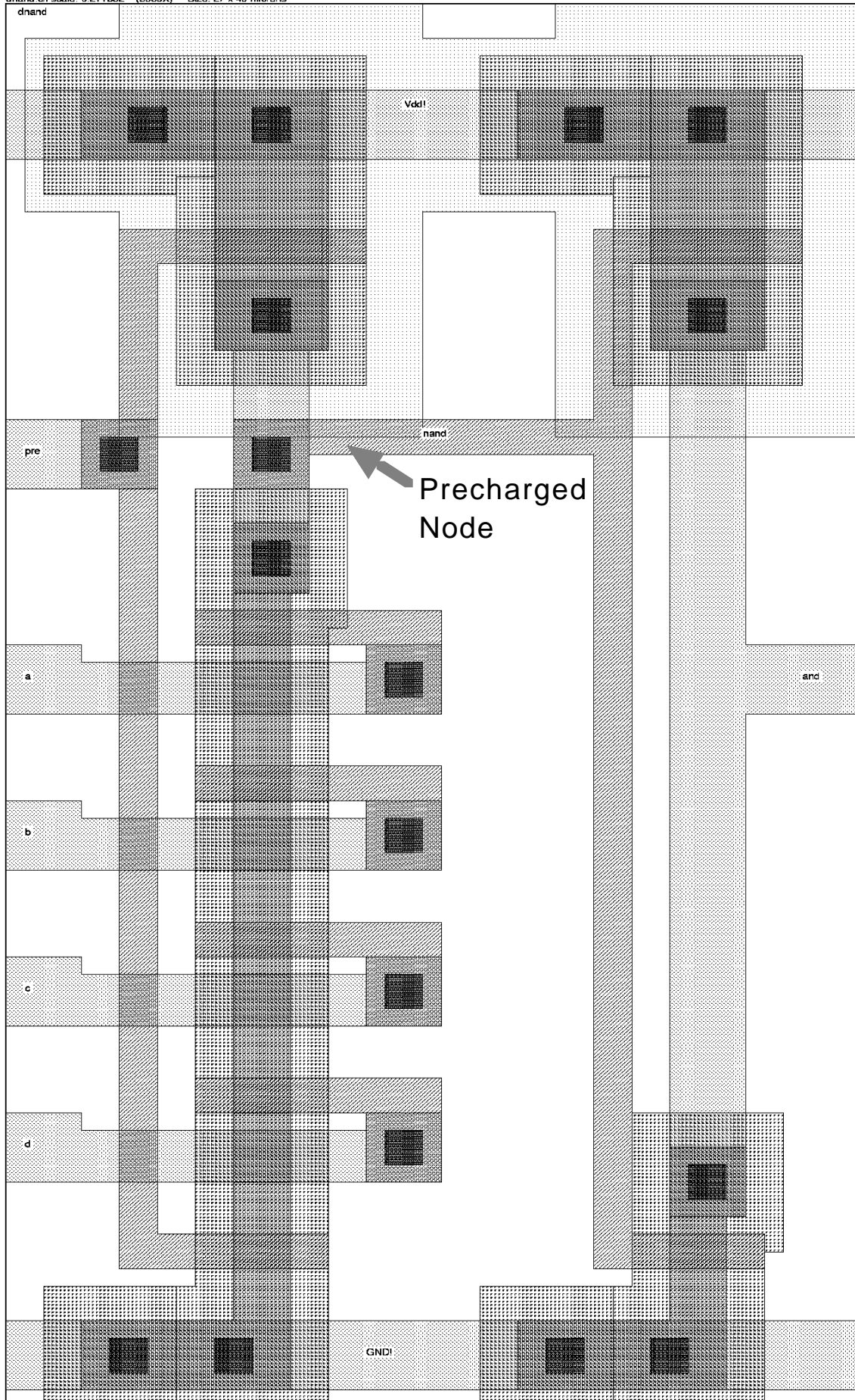


Elec 422 VLSI Design I -- Dynamic Domino AND Gate

dnand.cel scale: 0.211382 (5369X) Size: 27 x 49 microns



```

*** SPICE DECK created from dnand1.sim, tech=scmos
M1 1 4 5 3 CMOSP L=1.2U W=3.6U
M2 1 5 6 3 CMOSP L=1.2U W=3.6U
M3 5 7 8 2 CMOSN L=1.2U W=1.8U
M4 8 9 10 2 CMOSN L=1.2U W=1.8U
M5 10 11 12 2 CMOSN L=1.2U W=1.8U
M6 12 13 14 2 CMOSN L=1.2U W=1.8U
M7 14 4 0 2 CMOSN L=1.2U W=1.8U
M8 6 5 0 2 CMOSN L=1.2U W=1.8U
C9 6 0 19.0F
C10 5 0 23.0F
C11 1 0 25.0F
* GND      0
* Vdd     1
* NMOS    2
* PMOS    3
* CMOSN   2
* CMOSP   3
* pre     4
* nand    5
* and     6
* a       7
* 6_20_30# 8
* b       9
* 6_20_12# 10
* c      11
* 6_20_7# 12
* d      13
* 6_20_25# 14
.MODEL CMOSN NMOS LEVEL=2 PHI=0.700000 TOX=2.9700E-08 XJ=0.200000U TPG=1
+ VTO=0.5597 DELTA=9.3220E-01 LD=6.5780E-08 KP=7.8748E-05
+ UO=677.3 RSH=2.9330E+01 GAMMA=0.5743
+ NSUB=1.3430E+16 NFS=7.1500E+11 VMAX=1.8650E+05
+ CGDO=1.1472E-10 CGSO=1.1472E-10
+ CGBO=3.3855E-10 CJ=2.7107E-04 MJ=5.2656E-01 CJSW=1.5072E-10
+ MJSW=1.0000E-01 PB=9.1954E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 8.7580E-07
.MODEL CMOSP PMOS LEVEL=2 PHI=0.700000 TOX=2.9700E-08 XJ=0.200000U TPG=-1
+ VTO=-0.7595 DELTA=2.2970E+00 LD=1.1000E-09 KP=2.3440E-05
+ UO=201.6 RSH=8.4110E-01 GAMMA=0.3238
+ NSUB=4.2700E+15 NFS=6.4990E+11 VMAX=1.9020E+05
+ CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.3325E-10 CJ=2.9032E-04 MJ=4.5540E-01 CJSW=1.8518E-10
+ MJSW=1.0904E-01 PB=8.0729E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 8.5120E-07
*
* N81X SPICE LEVEL2 PARAMETERS --- AMI 1.2micron Run Feb. 1998
* derived from original LEVEL3 Parameters for spice3e1
*
*
* Elec422 SPICE EXPERIMENT TEMPLATE;
* -----

* Set BASIC VOLTAGE levels
*vdd <Vdd> <GND> dc 5

```

SPICE Input file
 for case all inputs
 low during
 precharge and
 evaluation.

```

vdd 1      0      dc 5
* set substrate voltages : P-sub = Vdd;  N-sub = GND
*vs1 <CMOSP> <Vdd> dc 0
vs1 3      1      dc 0
*vs2 <CMOSN> <GND> dc 0
vs2 2      0      dc 0

* -----

* Set other constant circuit inputs, for example b, cin:
*va  <a>    <GND> dc 0
va  7      0      dc 0
*vb  <b>    <GND> dc 0
vb  9      0      dc 0
*vc  <c>    <GND> dc 0
vc  11     0      dc 0
*vd  <d>    <GND> dc 0
vd  13     0      dc 0

* -----

* Set Circuit Input which will change, for example a:
* input pulse between node and GND (initially 0 ) of:
* pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
*vpre <pre> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
vpre 4      0      0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)

* -----

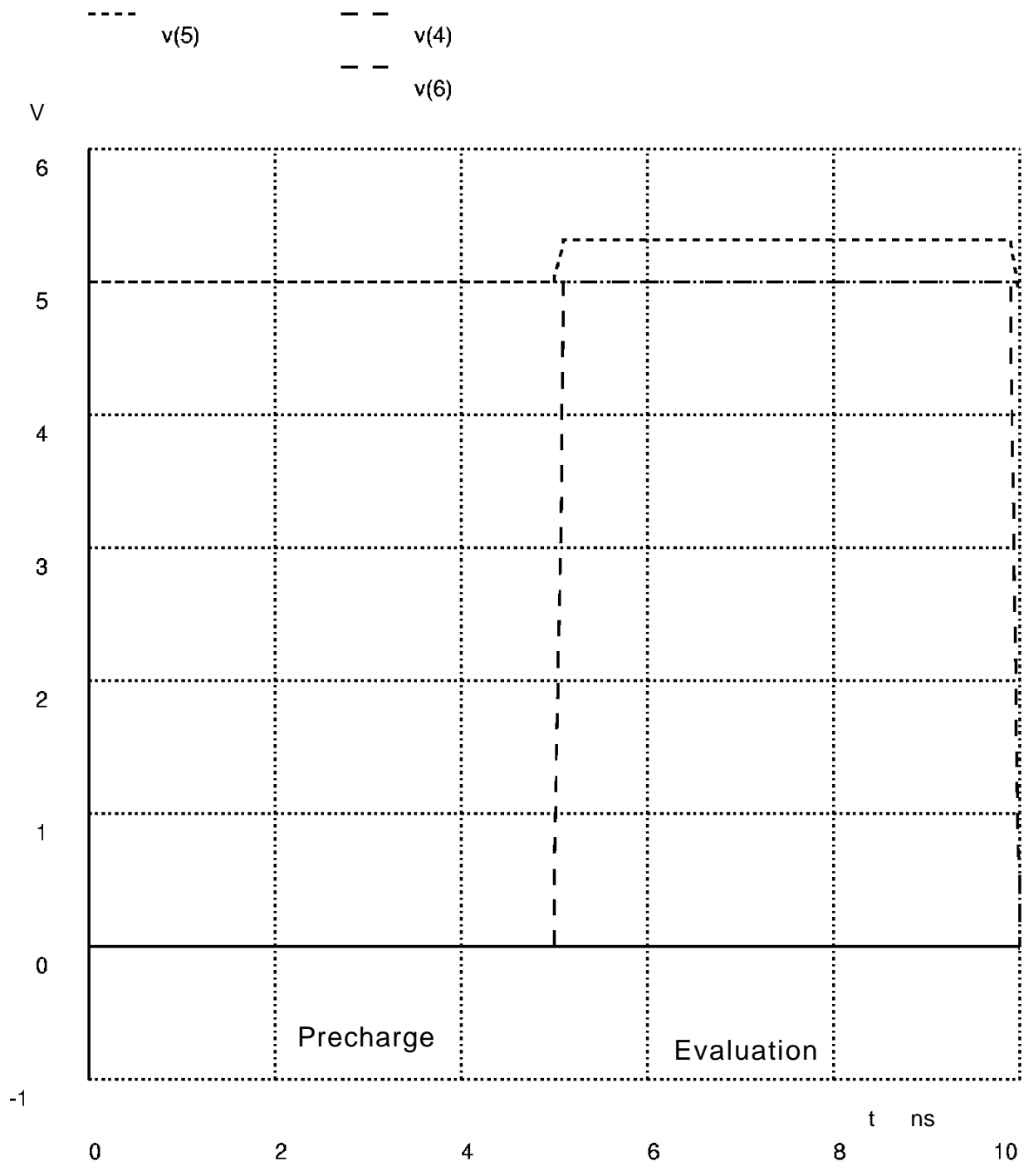
* Do analysis: give increments and total time for analysis.
.tran .1ns 10ns

* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages
*.plot tran v(<pre>) v(<nand>) v(<and>)
.plot tran v(4)      v(5)      v(6)

* set hcopydevtype=postscript

.end

```



```

*
* Elec422 SPICE EXPERIMENT TEMPLATE;
* -----

* Set BASIC VOLTAGE levels
vdd <Vdd> <GND> dc 5
* set substrate voltages : P-sub = Vdd; N-sub = GND
vs1 <CMOSP> <Vdd> dc 0
vs2 <CMOSN> <GND> dc 0

* -----

* Set other constant circuit inputs, for example b, cin:
* None here.

* -----

* Set Circuit Input which will change, for example a:
* input pulse between node and GND (initially 0 ) of:
* pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
vpre <pre> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
va <a> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
vb <b> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
vc <c> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
vd <d> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)

* -----

* Do analysis: give increments and total time for analysis.
.tran .1ns 10ns

* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages
.plot tran v(<pre>) v(<nand>) v(<and>)

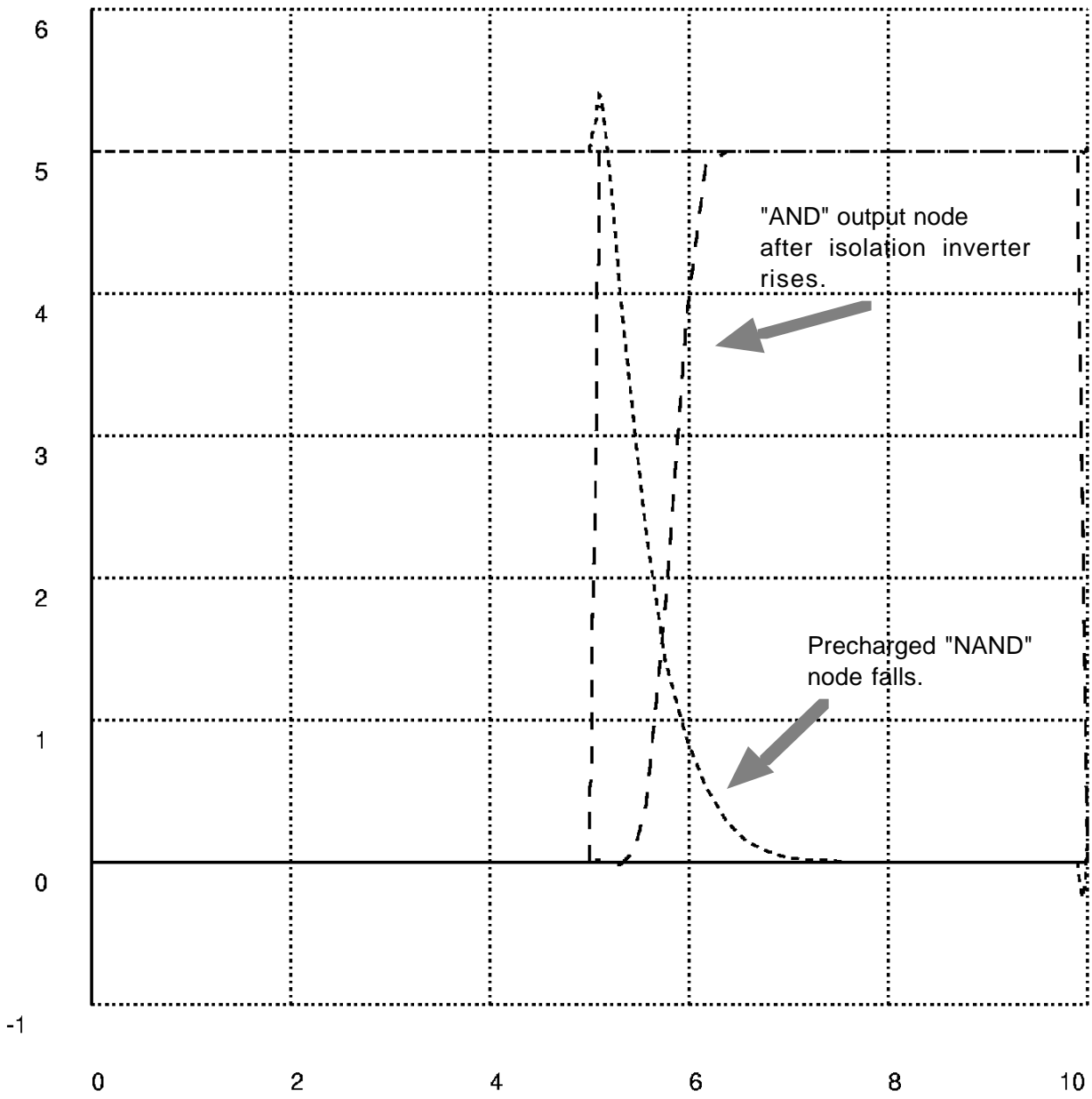
* set hcopydevtype=postscript

.end

```

All inputs high
during evaluation
phase.

----- v(5) - - - v(4)
- - - v(6)



```

*
* Elec422 SPICE EXPERIMENT TEMPLATE;
* -----

* Set BASIC VOLTAGE levels
vdd <Vdd> <GND> dc 5
* set substrate voltages : P-sub = Vdd; N-sub = GND
vs1 <CMOSP> <Vdd> dc 0
vs2 <CMOSN> <GND> dc 0

* -----

* Set other constant circuit inputs, for example b, cin:
vd <d> <GND> dc 0

* -----

* Set Circuit Input which will change, for example a:
* input pulse between node and GND (initially 0 ) of:
* pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
vpre <pre> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
va <a> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
vb <b> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)
vc <c> <GND> 0 pulse(0 5 5ns 0.1ns 0.1ns 4.8ns 10ns)

* -----

* Do analysis: give increments and total time for analysis.
.tran .1ns 10ns

* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages
.plot tran v(<pre>) v(<nand>) v(<and>)

* set hcopydevtype=postscript

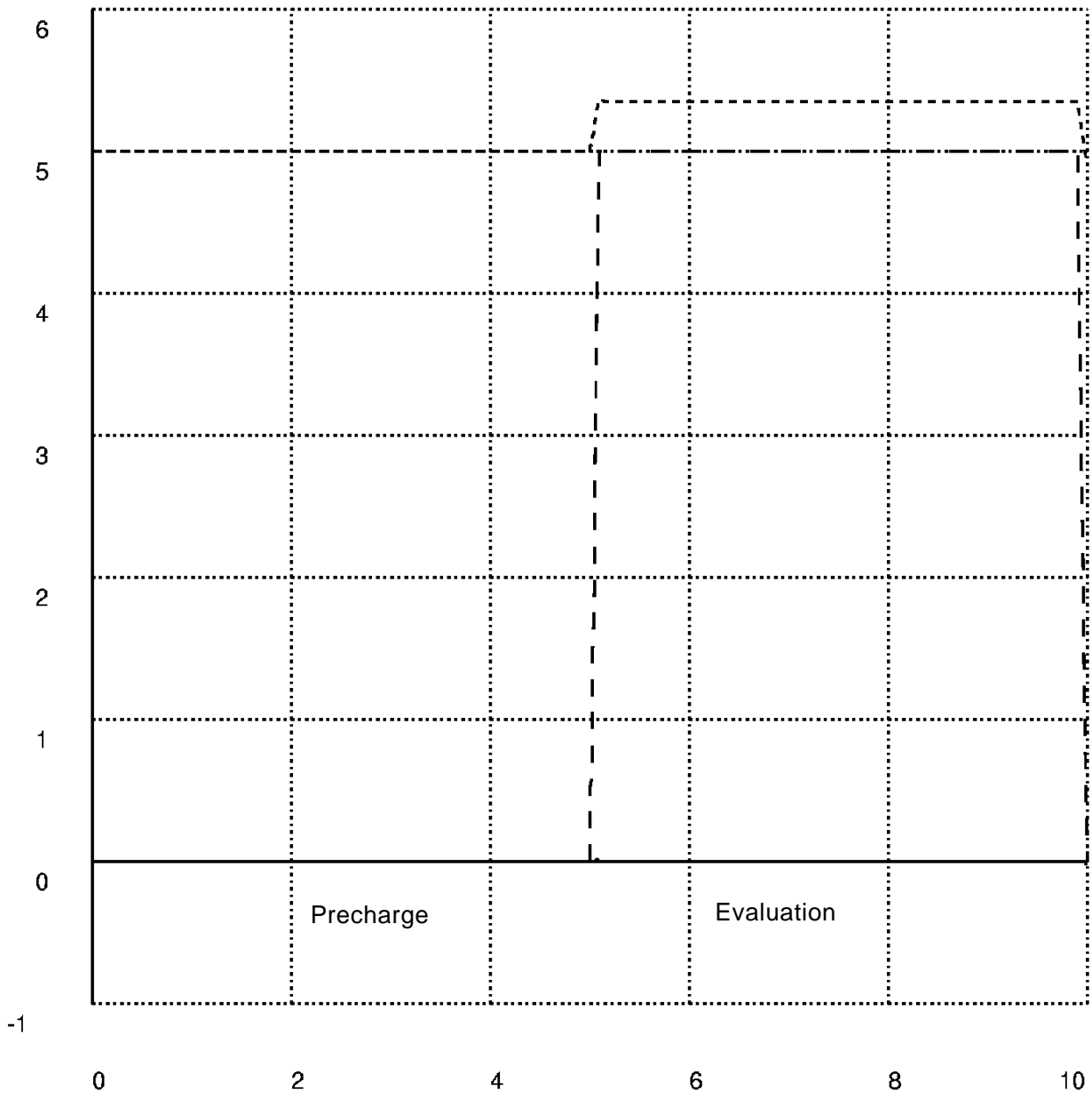
.end

```

Top three inputs, a,b,c, are high during evaluation. Input d remains low.

Possible charge sharing could occur.

----- v(5) - - - v(4)
- - - v(6)



| IRSIM Test Vector for domino dynamic nand

clock Vdd 1

ana pre a b c d nand and

V pre 0 1 0 1 0 1 0 1 0

V a 0 1 0 1 1 1 1 1 0

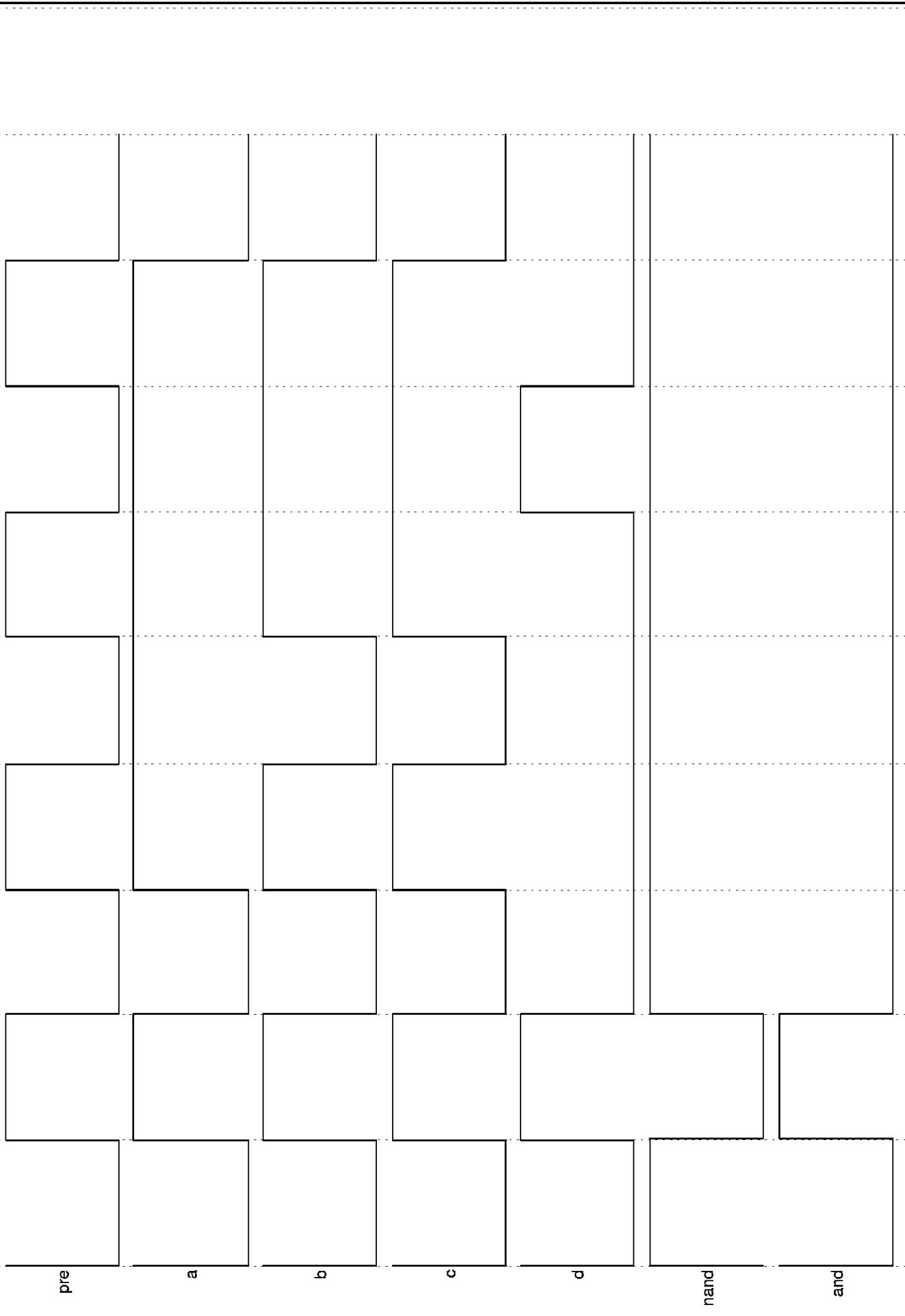
V b 0 1 0 1 0 1 1 1 0

V c 0 1 0 1 0 1 1 1 0

V d 0 1 0 0 0 0 1 0 0

R

Irsim test vector file



time (ns) 0.0 100.0 200.0 300.0 400.0 500.0 600.0 700.0 800.0 900.0 1000.0