Elec 422: VLSI Design I

Information on Old 2 Micron I/O Pads

Fall 1998, November 24, 1998

1 Mosis documentation on the 2 micron padframe

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*** NOTICE ***

These pads have been validated by the MOSIS System of USC/ISI. Any
modification of these pads by the user is done solely at the user's
risk.  Modified pads are not to be referred to as "MOSIS Pads" unless
prior agreement is obtained from USC/ISI.

MOSIS really intends that you use the complete (stuffed) digital or
analog pad frames without modification.  The individual pads and pad
frame subcells are supplied only as a courtesy to those who want to
build and verify their own custom pad frames.  These pads were not
designed to be interchangeable within the pad frame, rather, they were
optimized for power and size, and require intricate editing and
verification in different arrangements.);

                               TINYCHIP PADS SET

                             SCN (N-WELL) 2.0 MICRON

1. INTRODUCTION

This 2 micron SCN (N-well) TinyChip pads set was designed with the
MOSIS scalable CMOS design rules (Rev 6) at a lambda of 1.0 micron.
To use these pads, get the newest Magic technology file (dated on or
after than 1/19/93).  All pads are laid out on a lambda grid and are
designed for use with the 40PC22X22 Standard Frame.


2. CONTENTS OF THE DIGITAL PADS SET

 * List

blank.CIF balnk with only bonding metals
gnd.CIF internal GND power supply - not connected to pad GND
vdd.CIF internal Vdd power supply - not connected to pad Vdd
in.CIF input pad - a derivative from I/O pad
io.CIF input/output pad
out.CIF output pad - a derivative from I/O pad
cg.CIF GND Bottom Left corner pad
CG_r.CIF GND Bottom Right corner pad
cv.CIF Vdd Top Left corner pad
cv_r.CIF Vdd Top Right corner pad
40pc22x22_stuffed.CIF   contains a complete io pad ring layout in size
                        2220x2250 um
```

* Description

The single most important pad in this pad set is the IO pad. From this tri-state I/O pad we derived the IN pad and the OUT pad. A circuit diagram for this tri-state I/O pad is given below. Connecting ENABLE to GND will turn this I/O pad into an input pad. Connecting ENABLE to Vdd will result an output pad.

ESD protection is done with
  (1) Thick-Field Oxide transistor of size W/L= 600/3 microns,
  (2) 150 ohms N_diffusion resistor/diode, and
  (3) Tri-state output drivers as pair of diode clamps.

* Circuit Diagram

```
                                                             +------+
                                                        +----| PAD |
                                                        |    +------+
                                                      +-+       |
                          Vdd                         |         \
                      +---------+                     +-+       / 150 ohm
                      |         |                       |GND    \
                  |+--+         +--+|  ENABLE                   |
              +--0||               ||0---------         Vdd     |
              |   |+--+         +--+|                    |      |
              |       |         |                    |+--+      |
              |       +---------+-------------------0|| P       |
              |       |         |                    |+--+      |
      ENABLE  |   |+--+         +--+| ENABLEbar          |      |
     ---------|---||               ||0--+------          +------+
              |   |+--+         +--+|   |                |      | IN_unbuffered
              |       |         |       |            |+--+      |
              |       +---------+-------|------------|| N     +---+
              |       |         |       |            |+--+    |   |
        OUT   |   |+--+         +--+|   |                |     \ /
        ------+---||               ||---+              GND      0
                  |+--+         +--+|                           | INbar
                      |         |                             +---+
                      +---------+                             |   |
                         GND                                   \ /
                                                                0
                                                                |
                                                               IN
```

* Size

These pads should fit into the standard frame 40PC22x22 with mirroring. They can also be used for other MOSIS standard frames. io, in, out, Vblank, vdd, and gnd has none-well maximum bonding box (MBB) of 200x210 microns each. The well MBB is 210x218 microns. The stuffed frame has a non-well MBB of 2220x2250 microns. There are 9 pads on each edge plus 4 corners used as Vdd and GND pads. The top edge has a

GND pad in the middle and its 2 corners are Vdd pads, while the bottom edge has a Vdd pad in the middle and its 2 corners are GND pads. This gives 3 Vdd and 3 GND pads total.

3. CONTENTS OF THE ANALOG PADS SET

* List

```
gndN.CIF internal GND power supply - not connected to pad GND
vddN.CIF internal Vdd power supply - not connected to pad Vdd
analogN.CIF             analog input/output pad
llN.CIF GND Bottom Left corner pad
urN.CIF Vdd Top Right corner pad
40pc22x22_stuffed_analog.CIF   contains a complete io pad ring layout in size
                        2220x2250 um
```

* Description

ESD protection is achieved by two lateral PNP parasitic transistor in N-well

(1) reverse biased diode connected to Vdd when a positive ESD stress is applied.
(2) PNP transistor from GND to input when a negative ESD stress is applied.

4. SIMULATION and MEASUREMENT

Both pad set have been fabricated by MOSIS for verification, but only pads in digital set are simulated and measured. Their result are listed as follows:

* Delay

OUTPUT Driver Load (SIMULATED)

	10pF	30pF	50pF
rise time	8ns	21ns	30ns
fall time	7ns	17ns	25ns

OUTPUT Driver Load (MEASURED)

	no load	10pF	22pF	47pF
prop. delay (0 to 1)	8.6ns	10.8ns	13.0ns	18.5ns

INPUT Driver Load (SIMULATED)

load: load: load:
INbar/IN INbar/IN INbar/IN

```
0.5/1pF 1/2pF 2/4pF
prop/rise/fall prop/rise/fall prop/rise/fall
signal signal delay/time/time delay/time/time delay/time/time
------ ------ --------------- --------------- ---------------
PAD INbar 1.1/3.9/2.0 1.6/5.5/3.0 2.2/8.5/4.5
INbar IN 2.2/3.0/2.2 2.2/5.0/3.5 3.8/8.5/6.5

 * DC Current Capability

Maximum current :: 11 mA per I/O pad with 50pF loading

 5. Magic CIF input

In Magic, Berkeley's layout editor, use ":cif is lambda=1.0(nwell)"
to specify the appropriate CIF input style before using ":cif read
..." command.
```

2 Use of I/O Pads with magic

Copy the magic files from /usr/site/cad/lib/magic/scmos to your directory. You may want to make them read-only. The full set of magic files is:

File name	Function	Quantity	Pin location
frame_v4.mag	Stuffed Top level pad frame	1	
V4_cg.mag	Corner GND pad to power padframe	1	25
V4_cv.mag	Corner Vdd pad to power padframe	1	15
V4gnd.mag	GND pad to power chip internals	1	10
V4vdd.mag	Vdd pad to power chip internals	1	30
V4_cg1.mag	Corner GND pad to power padframe	1	35
V4_cv1.mag	Corner Vdd pad to power padframe	1	5
V4io.mag	Input/Output Pad for signals	34	All others

where "frame_v4.mag" is the top level cell in the 40 pin stuffed padframe. Except for the six power and ground pads, all the pads are of type "V4io" which is a bi-directional pad. The "Enable" connection on each of the I/O pads will need to be tied to either Vdd (output) or GND (input).

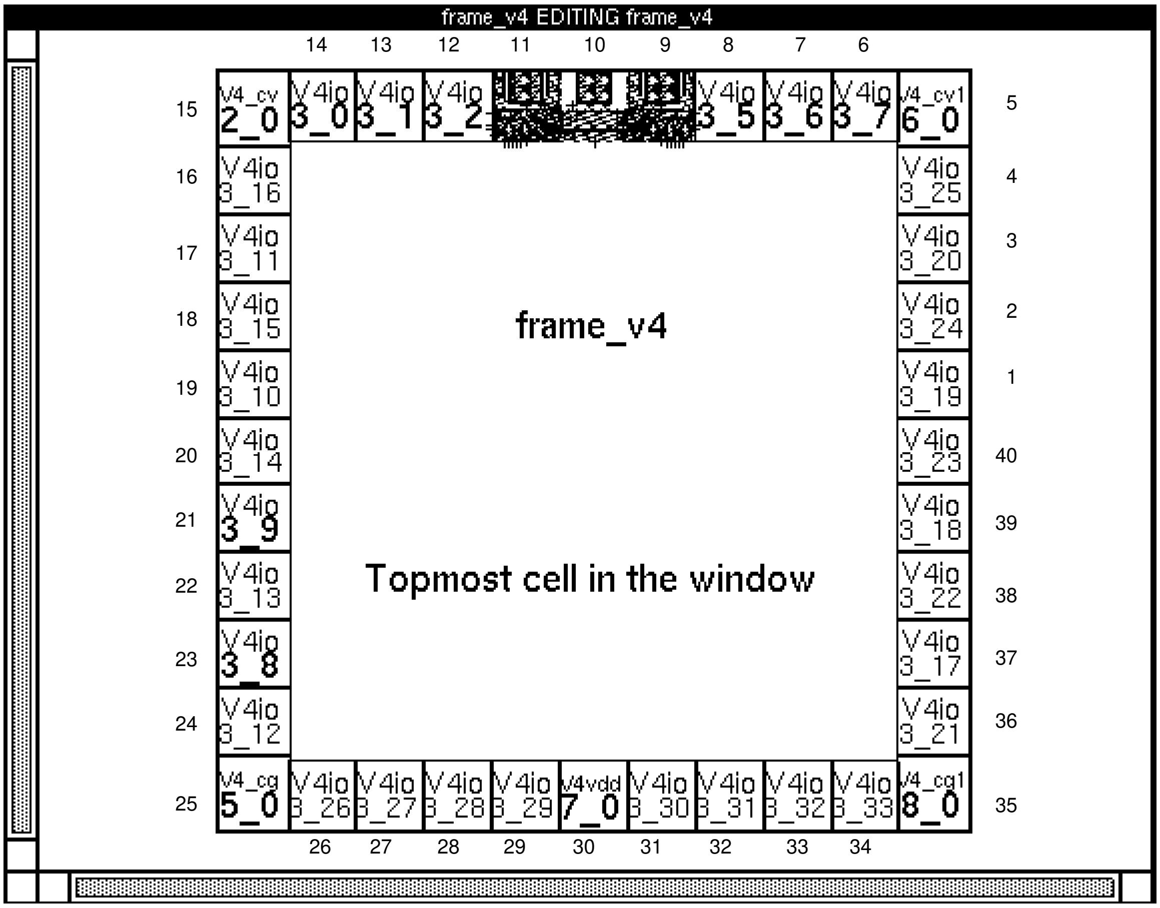

Figure 1: Xwindow dump of frame_v4 MOSIS padframe showing location of Pin 1.

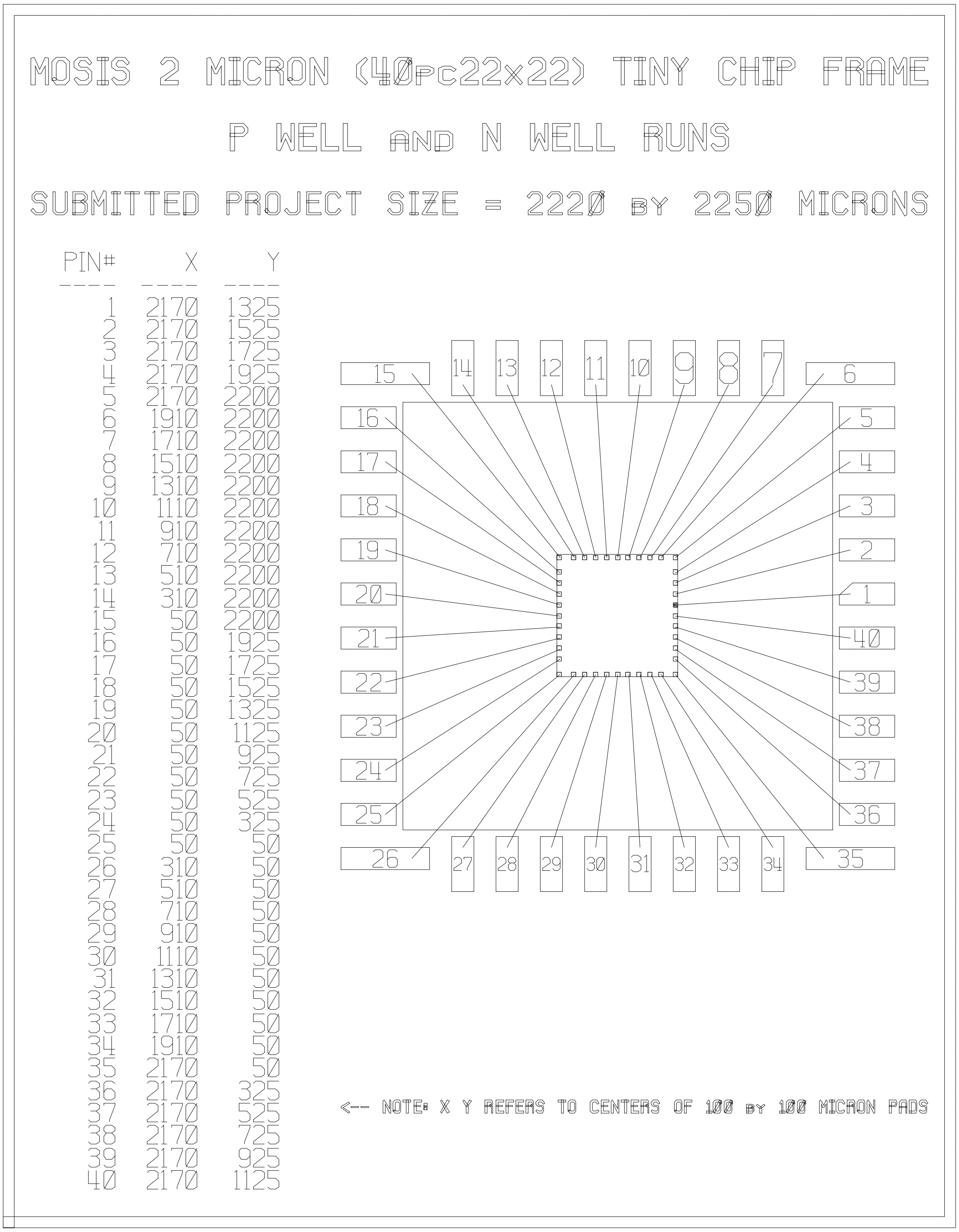

Figure 2: Location of I/O pads around perimeter of padframe.

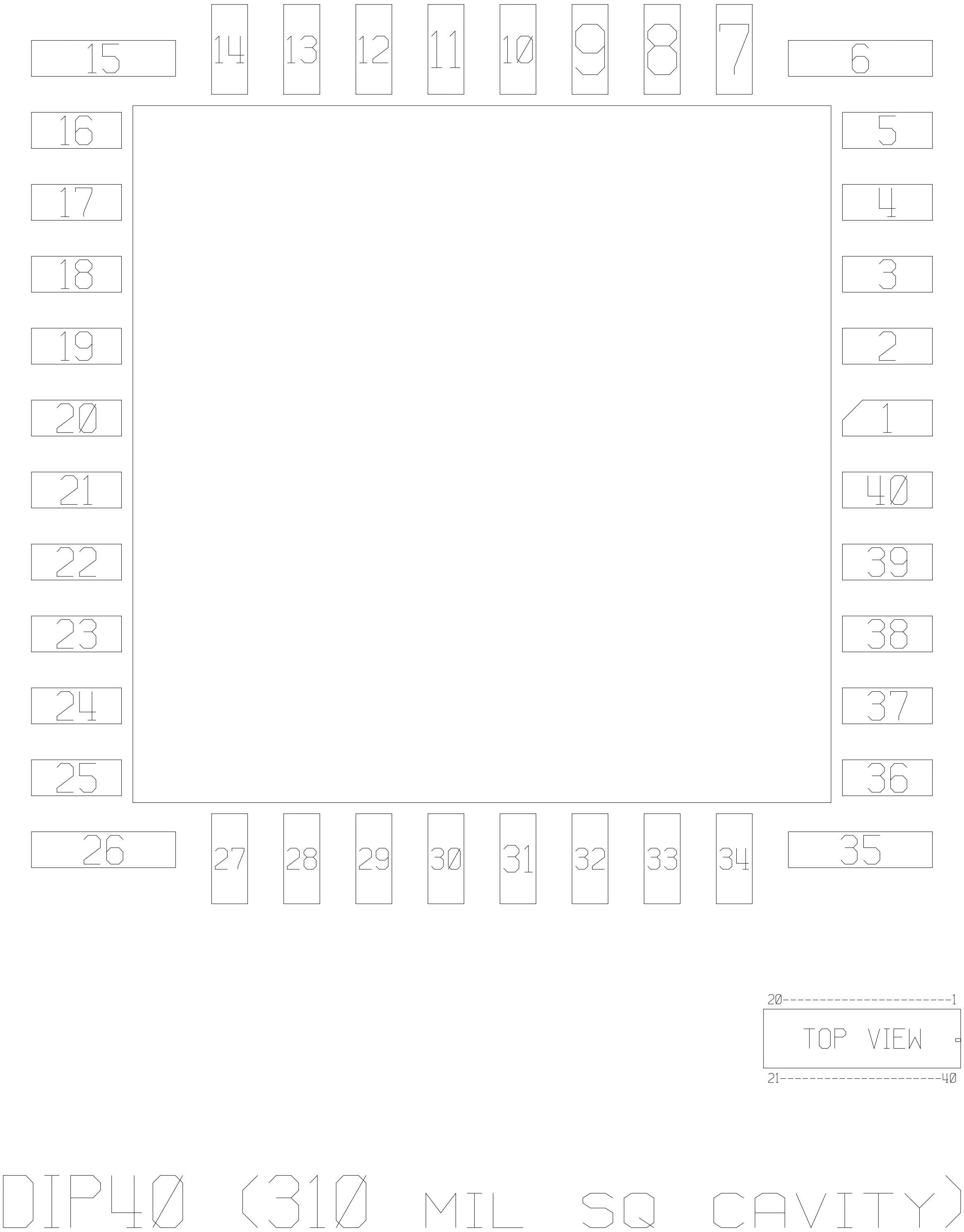

Figure 3: Bonding map and DIP pin assignment.

3 Detail of V4io input/output pad

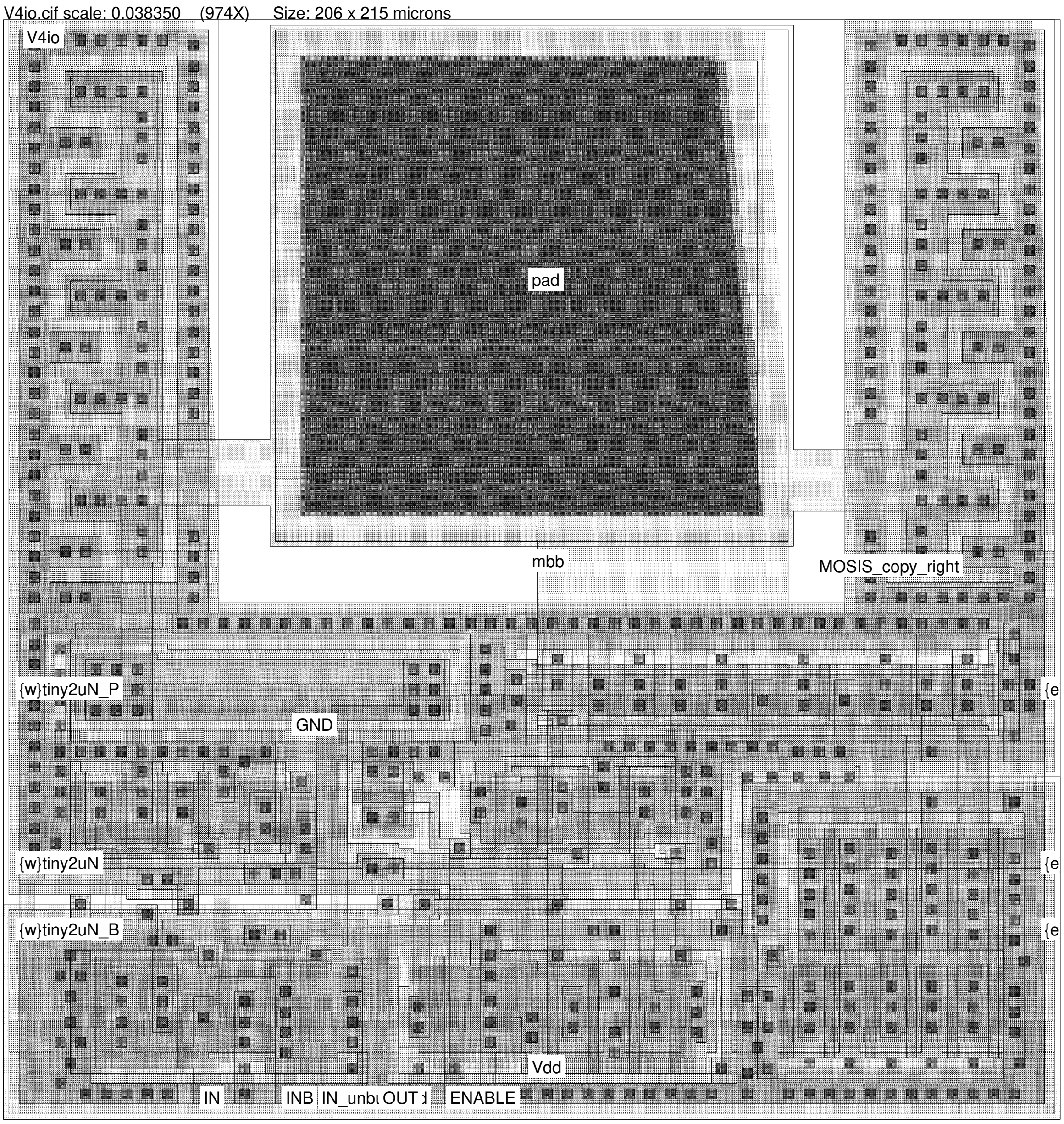

Figure 4: Layout of main I/O pad, V4io.

3.1 Netlist sim file for V4io

```
| units: 100 tech: scmos
n 6_156_290# GND pad 2 6 90 168
n 6_156_290# pad GND 2 6 98 168
n 6_156_290# GND pad 2 8 106 166
n 6_156_290# pad GND 2 8 114 166
n 6_156_290# GND pad 2 8 122 166
n 6_156_290# pad GND 2 8 130 166
n 6_156_290# GND pad 2 8 138 166
n 6_156_290# pad GND 2 8 146 166
n 6_156_290# GND pad 2 8 154 166
n 6_156_290# pad GND 2 8 162 166
n 6_156_290# GND pad 2 8 170 166
n 6_156_290# pad GND 2 8 178 166
n INB GND IN 2 12 1 141
n INB IN GND 2 12 9 141
n INB GND IN 2 12 17 141
n INB IN GND 2 10 25 143
n pad GND INB 2 16 33 142
n pad INB GND 2 9 41 141
n ENABLE 6_114_288# GND 2 8 57 149
n ENABLE 6_156_290# 6_170_282# 2 12 83 141
n ENABLE 6_170_282# 6_156_290# 2 13 91 141
n OUT 6_156_290# GND 2 12 99 142
n OUT GND 6_156_290# 2 12 107 142
n 6_114_288# 6_156_290# GND 2 11 115 143
p INB Vdd IN 2 17 5 99
p INB IN Vdd 2 17 13 99
p INB Vdd IN 2 17 21 99
p INB IN Vdd 2 16 29 100
p pad Vdd INB 2 16 37 100
p pad INB Vdd 2 18 45 98
p ENABLE 6_114_288# Vdd 2 17 71 100
p ENABLE Vdd 6_170_282# 2 18 85 100
p OUT 6_170_282# Vdd 2 18 93 98
p OUT Vdd 6_170_282# 2 18 101 98
p 6_114_288# 6_170_282# 6_156_290# 2 18 109 98
p 6_114_288# 6_156_290# 6_170_282# 2 18 117 98
p 6_170_282# pad Vdd 2 22 147 120
p 6_170_282# Vdd pad 2 22 155 120
p 6_170_282# pad Vdd 2 22 163 120
p 6_170_282# Vdd pad 2 22 171 120
p 6_170_282# pad Vdd 2 22 179 120
p 6_170_282# Vdd pad 2 15 139 101
p 6_170_282# pad Vdd 2 15 147 101
p 6_170_282# Vdd pad 2 15 155 101
p 6_170_282# pad Vdd 2 15 163 101
p 6_170_282# Vdd pad 2 15 171 101
p 6_170_282# pad Vdd 2 15 179 101
C GND 6_156_290# 14
C GND pad 70
C pad Vdd 20
C 6_170_282# Vdd 16
C IN Vdd 11
C GND Vdd 17
C Vdd GND 609
C 6_114_288# GND 60
C 6_170_282# GND 150
C OUT GND 24
C ENABLE GND 18
C IN GND 114
C INB GND 75
C 6_156_290# GND 139
C pad GND 1849
C GND GND 2079
```

3.2 Irsim simulation of V4io Pad

The following set of test vectors first runs the V4io pad as an input pad by setting ENABLE to logic 0. Then the V4io pad is configured as an output pad by setting ENABLE to logic 1. In your chips, you will hardwire configure some of the V4io pads as inputs by connecting ENABLE to GND, and configure some of the V4io pads as outputs by connecting ENABLE to Vdd. It is important to also connect the ENABLE signals of the unused pads to either Vdd or GND.

```
| Irsim Test Vector for V4io I/O pad

| Watch nodes
ana pad ENABLE IN INB OUT

| Since irsim needs a clock while the inverter is a combinational circuit,
| we will use a dummy clock signal just to keep irsim happy.
clock Vdd 1

| Configure V4io as an INPUT pad.

V ENABLE 0 0 0 0 0 0 0
V pad    0 1 0 0 1 1 0

| Simulate the circuit for this sequence of inputs
R


| Configure V4io as an OUTPUT pad.

V ENABLE 1 1 1 1 1 1 1
V OUT    0 1 0 0 1 1 0

| Simulate the circuit for this sequence of inputs
R
```

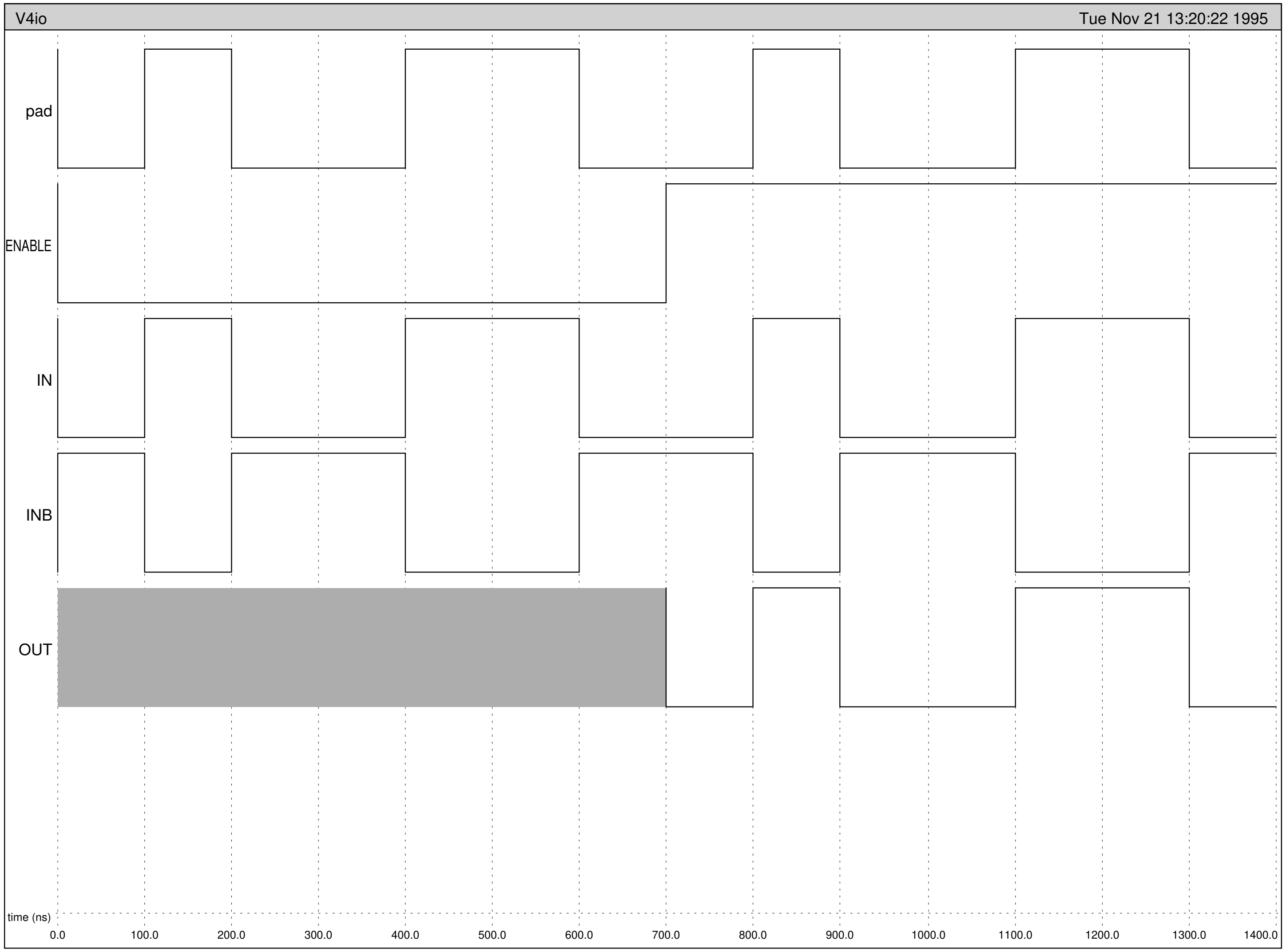

Figure 5: IRSIM simulation of V4io Pad.

3.3 Spice Simulation of V4io as an Input Pad

```
*
* Elec422 SPICE EXPERIMENT TEMPLATE;
* Set BASIC VOLTAGE levels
vdd <Vdd>  <GND>  dc 5
* set substrate voltages : P-sub = Vdd;  N-sub = GND
vs1 <CMOSP> <Vdd>  dc 0
vs2 <CMOSN> <GND>  dc 0

* ------------------------------------

* Set other constant circuit inputs, for example b, cin:
venable <ENABLE> <GND> dc 0
vout <OUT> <GND> dc 0

* ------------------------------------

* Set Circuit Input which will change, for example a:
* input pulse between node and GND (initially 0 ) of:
* pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
vin <pad> <GND> 0 pulse(0 5 0ns 0.1ns 0.1ns 4.8ns 10ns)

* ------------------------------------

* Do analysis: give increments and total time for analysis.
.tran .1ns 10ns
*
*
* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages, for example a, sum, cout
.plot tran v(<ENABLE>) v(<pad>) v(<IN>) v(<INB>)

.end
```

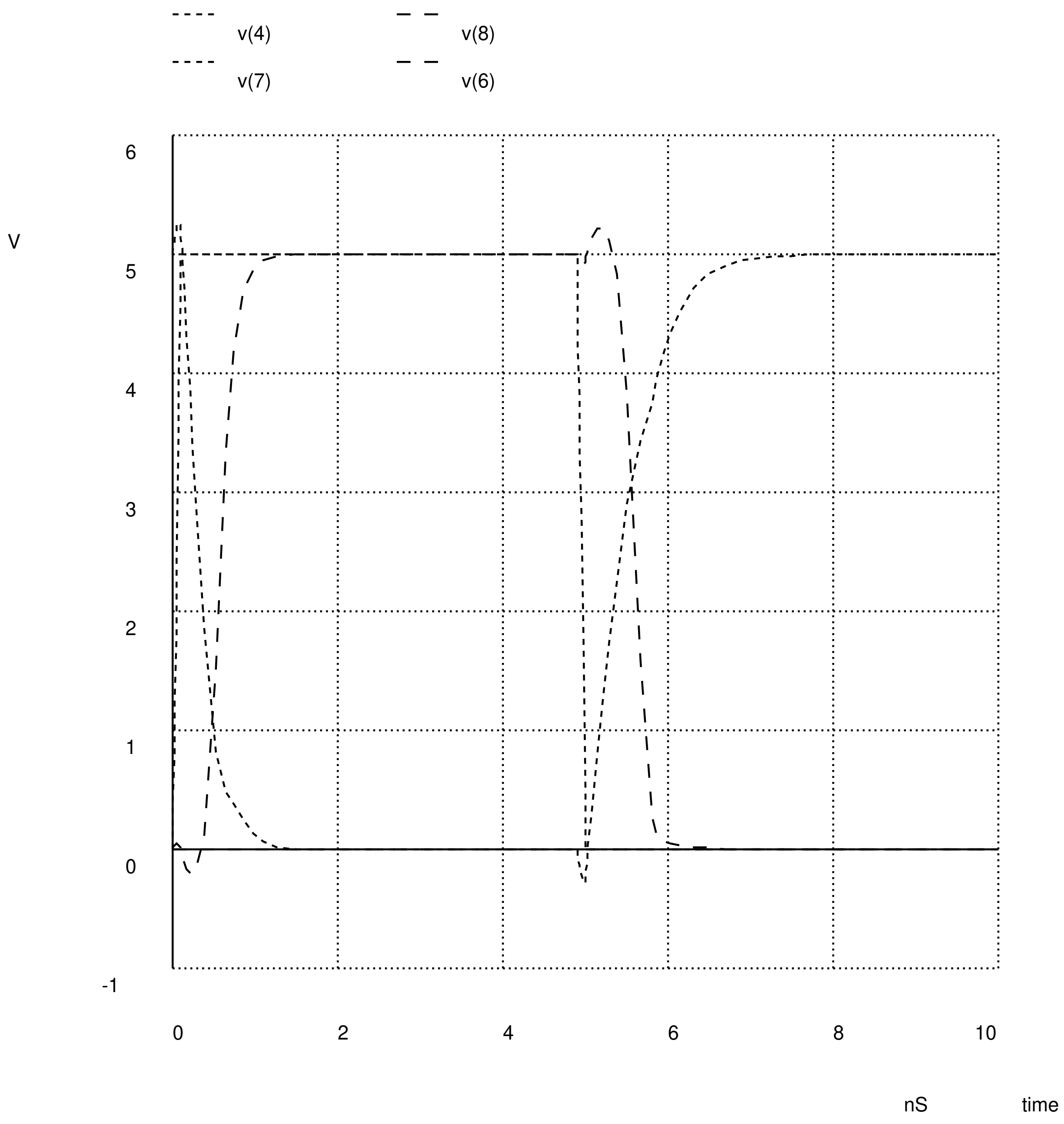

Figure 6: Spice simulation of V4io as an Input Pad where v(8) = ENABLE, v(4) = pad, v(6) = IN, and v(7) = INB.

3.4 Spice Simulation of V4io as an Output Pad

```
*
* Elec560 SPICE EXPERIMENT TEMPLATE;
* J. Cavallaro 11/88, updated 11/89,
* updated N.D.Hemkumar & Kota Kishore 11/90, 11/91
* ------------------------------------

* Set BASIC VOLTAGE levels
vdd <Vdd>  <GND>  dc 5
* set substrate voltages : P-sub = Vdd;  N-sub = GND
vs1 <CMOSP> <Vdd>  dc 0
vs2 <CMOSN> <GND>  dc 0

* ------------------------------------

* Set other constant circuit inputs, for example b, cin:
venable <ENABLE> <GND> dc 5

* ------------------------------------

* Set Circuit Input which will change, for example a:
* input pulse between node and GND (initially 0 ) of:
* pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
vout <OUT> <GND> 0 pulse(0 5 0ns 0.1ns 0.1ns 4.8ns 10ns)

* ------------------------------------

* Do analysis: give increments and total time for analysis.
.tran .1ns 10ns
*
*
* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages, for example a, sum, cout
.plot tran v(<ENABLE>) v(<pad>) v(<OUT>)

.end
```

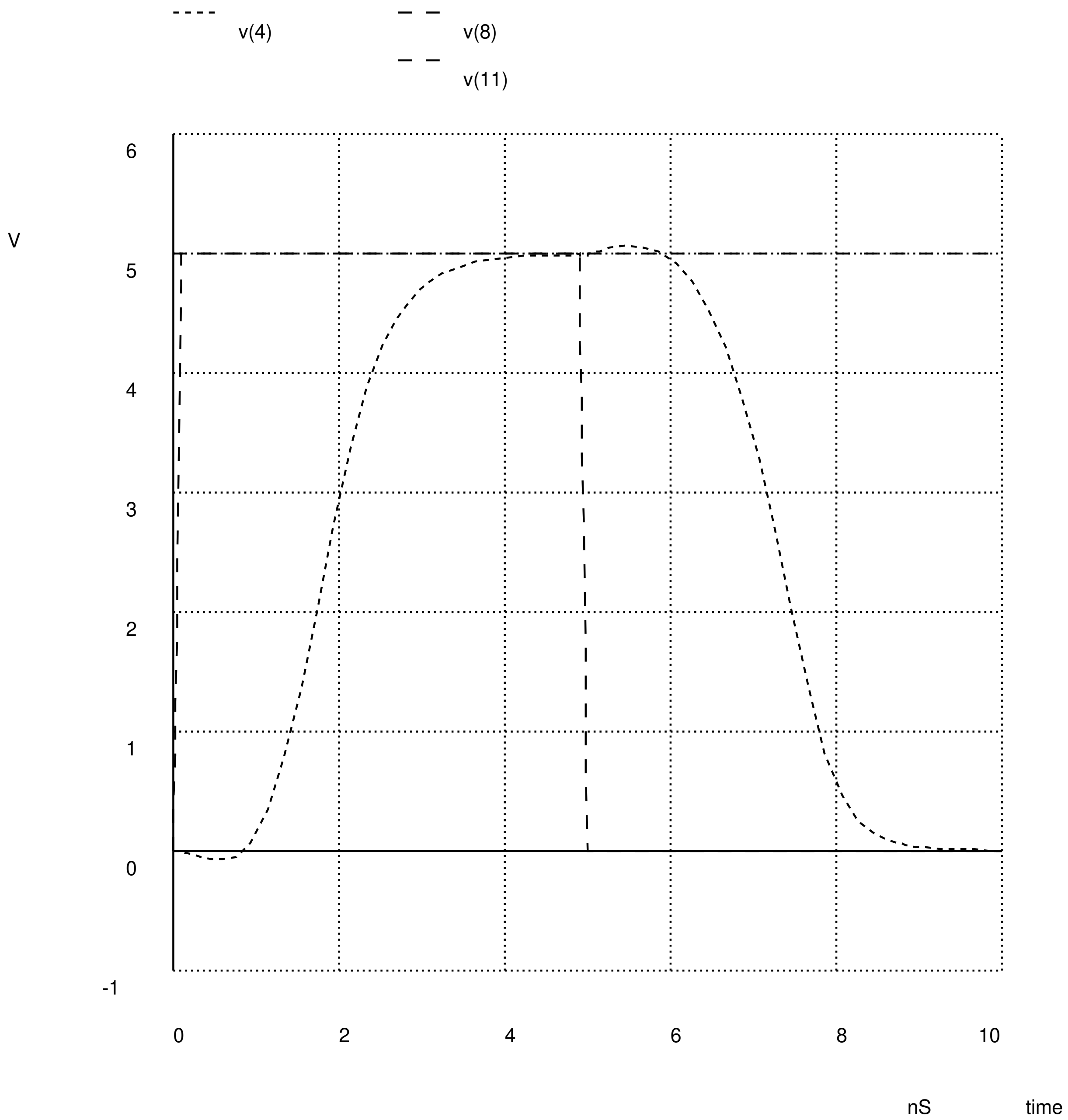

Figure 7: Spice simulation of V4io as an Output Pad where v(8) = ENABLE, v(4) = pad, v(11) = OUT.