Elec 422: VLSI Design I
Fall 1998

November 3, 1998

Notes on Basic on Ring Oscillators

Spice Simulation

Attached is a Spice simulation of three inverters connected to make a ring oscillator in a 2μ CMOS technology. After some initial transients, the period of oscillation is about $4ns$. The frequency is then about $250MHz$. The spice input file $ringosc.spcin$ can be found on Owlnet in /home/cavallar/demo/1998/ringosc. Magic layout is is also in that directory.

Note that this is an example and not a production grade circuit. The first inverter to the left has a pullup of $L = 2, W = 6$ and a pulldown of $L = 2, W = 3$. The middle inverter has the same ratio. The final inverter at the right has a pullup of $L = 2, W = 12$ and a pulldown of $L = 2, W = 6$. The output feedback node *loop* is run in polysilicon.

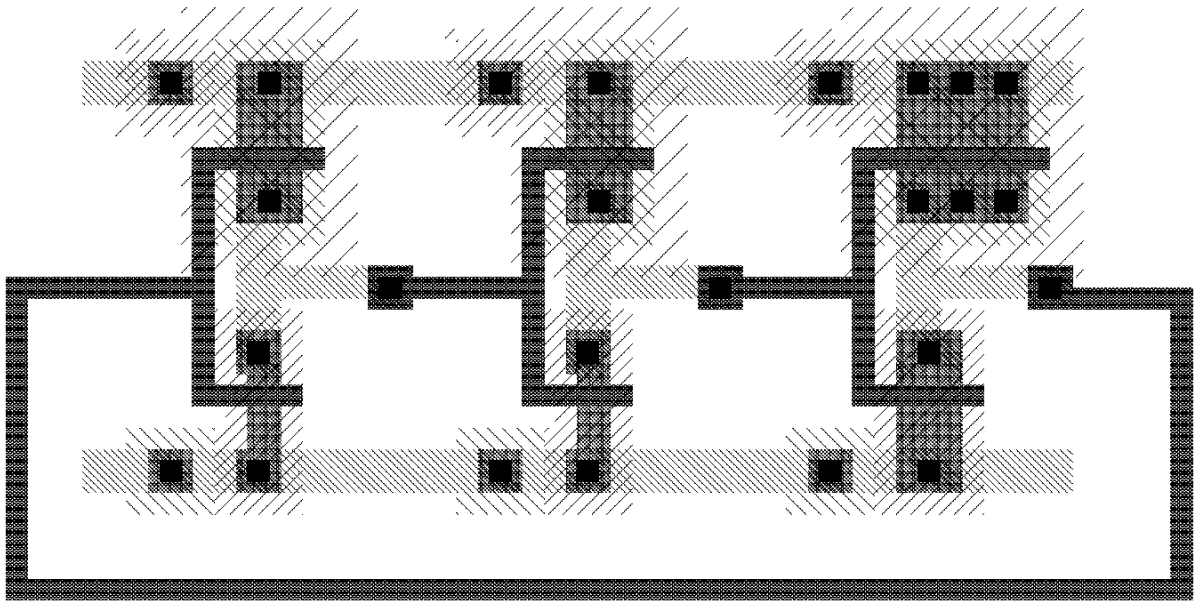

Figure 1: Plot of three stage Ring Oscillator.

```
*** SPICE DECK created from ringosc.sim, tech=scmos
M1  1  4  5  3 CMOSP L=2.0U W=12.0U
M2  5  4  0  2 CMOSN L=2.0U W=6.0U
M3  1  6  4  3 CMOSP L=2.0U W=6.0U
M4  4  6  0  2 CMOSN L=2.0U W=3.0U
M5  1  5  6  3 CMOSP L=2.0U W=6.0U
M6  6  5  0  2 CMOSN L=2.0U W=3.0U
C7  6  0  42.0F
C8  5  0  97.0F
C9  4  0  41.0F
C10  1  0  87.0F
*  GND 0
*  Vdd 1
*  NMOS 2
*  PMOS 3
*  CMOSN 2
*  CMOSP 3
*  out2 4
*  loop 5
*  out1 6
.MODEL CMOSN NMOS LEVEL=2 LD=0.240703U TOX=407.000000E-10
+ NSUB=3.133604E+15 VTO=0.711043 KP=4.879000E-05 GAMMA=0.3801
+ PHI=0.6 UO=575.027 UEXP=0.129885 UCRIT=24726.9
+ DELTA=0.82016 VMAX=63588.7 XJ=0.250000U LAMBDA=2.474695E-02
+ NFS=6.455307E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=29.040000 CGDO=3.063325E-10 CGSO=3.063325E-10 CGBO=5.135289E-10
+ CJ=1.130300E-04 MJ=0.699680 CJSW=5.235300E-10 MJSW=0.263078 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.60 um
.MODEL CMOSP PMOS LEVEL=2 LD=0.250000U TOX=407.000000E-10
+ NSUB=6.222000E+15 VTO=-0.80612 KP=2.113000E-05 GAMMA=0.5357
+ PHI=0.6 UO=249.519 UEXP=0.226251 UCRIT=18368.3
+ DELTA=1.75689 VMAX=40684.7 XJ=0.250000U LAMBDA=5.307119E-02
+ NFS=3.574015E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.160000 CGDO=3.181644E-10 CGSO=3.181644E-10 CGBO=6.682147E-10
+ CJ=2.493100E-04 MJ=0.551790 CJSW=2.815500E-10 MJSW=0.311229 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.04 um
*
* From N13L  SPICE LEVEL 2 PARAMETERS   1991 nwell
*
*
*  Elec422 SPICE EXPERIMENT TEMPLATE;
*  J. Cavallaro 11/88, updated 11/89,
*  updated N.D.Hemkumar & Kota Kishore 11/90, 11/91
*  ------------------------------------
```

```
*  Set BASIC VOLTAGE levels
*vdd <Vdd>  <GND>  dc 5
vdd 1      0      dc 5
*  set substrate voltages : P-sub = Vdd;  N-sub = GND
*vs1 <CMOSP> <Vdd>  dc 0
vs1 3       1      dc 0
*vs2 <CMOSN> <GND>  dc 0
vs2 2       0      dc 0

*  ------------------------------------

*  Set other constant circuit inputs, for example b, cin:
*  None here.

*  ------------------------------------

*  Set Circuit Input which will change, for example a:
*  input pulse between node and GND (initially 0 ) of:
*  pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
** NOTE: Commented out - no input specified.
** vin <loop> <GND> 0 pulse(0 5 0ns 0.1ns 0.1ns 4.8ns 10ns)
*  vin 5      0     0 pulse(0 5 0ns 0.1ns 0.1ns 4.8ns 10ns)

*  ------------------------------------



*  Do analysis: give increments and total time for analysis.
.tran .1ns 50ns

*  If running in batch mode spice -b, then ascii plots are made
*  Plot Voltages
*.plot tran v(<loop>)
.plot tran v(5)

*  set hcopydevtype=postscript

.end
```

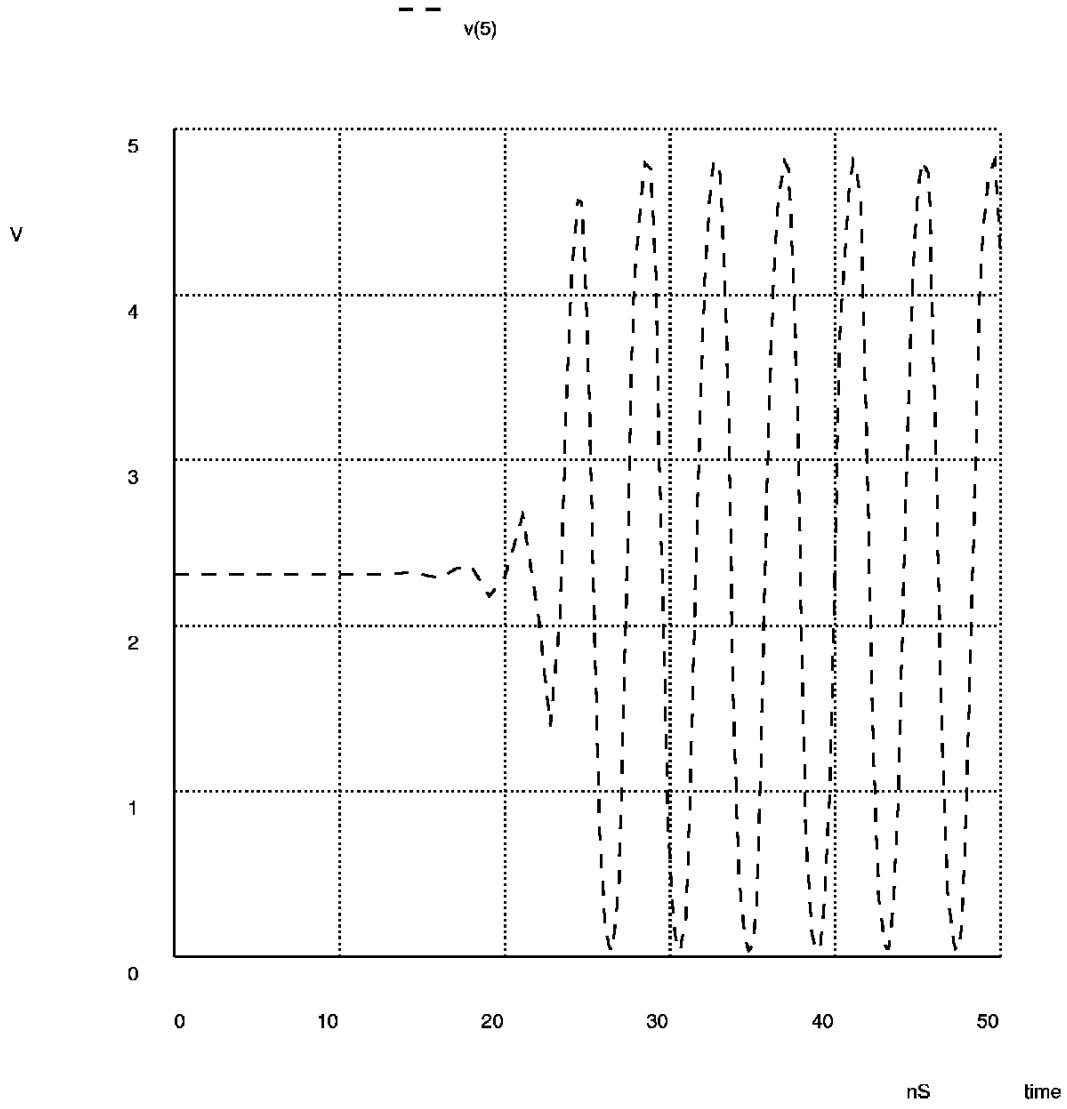

Figure 2: Spice output of node *loop*.

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Additional Information on 2 micron MOSIS Process

MOSIS PARAMETRIC TEST RESULTS

MOSIS-Reply-Posted-for-Delivery: 13 November 1991 17:25:37

RUN: N13L / LUCKY VENDOR: VTI
TECHNOLOGY: SCN FEATURE SIZE: 2.0um

I. INTRODUCTION. This report contains the lot average results obtained by MOSIS from measurements of the MOSIS test structures on the selected wafers of this fabrication lot. The SPICE LEVEL 2 and BSIM parameters obtained from similiar measurements on these wafers are also attached.

COMMENTS: This looks like a typical VLSI Technology 2.0um run.

II. TRANSISTOR

PARAMETERS:	W/L	N-CHANNEL	P-CHANNEL	UNITS
Vth (Vds=.05V)	3/2	.722	-.824	V
Vth (Vds=.05V)	18/2	.570	-.795	V
Idss (Vgds=5V)	18/2	2801.0	-1248.0	uA
Vpt (Id=1.0uA)	18/2	N/A	-16.12	V
Vth (Vds=.05V)	50/50	.763	-.794	V
Vbkd (Ij=1.0uA)	50/50	18.8	-15.8	V
Kp (Uo*Cox/2)	50/50	23.0	11.10	uA/V^2
Gamma (2.5v,5.0v)	50/50	.404	.505	V^0.5
Delta Length		.221	.421	um
Delta Width (Effective=Drawn-Delta)		.524	.124	um

COMMENTS: These parameters seem normal.

III. FIELD OXIDE

TRANSISTOR PARAMETERS:	GATE	SOURCE/DRAIN N + ACTIVE	SOURCE/DRAIN P + ACTIVE	UNITS
Vth (Vbs=0,I=1uA)	Poly	22.2	-15.6	V
Vth (Vbs=0,I=1uA)	Metal1	22.2	-20.3	V
Vth (Vbs=0,I=1uA)	Metal2	22.3	-25.5	V

COMMENTS: These parameters seem normal.

IV. PROCESS PARAMETERS:	N POLY	P POLY	N DIFF	P DIFF	N WELL	METAL 1	METAL 2	UNITS
Sheet Resistance	22.4	23.1	29.2	86.9	2281.0	.090	.038	Ohm/sq
Width Variation (Measured - Drawn)	.399	.377	.653	.198	----	.390	.820	um
Contact Resist. (Metal1 to Layer)	6.47	6.72	10.89	28.05	----	----	.111	Ohms
Gate Oxide Thickness:	----	----	----	397.	----	----	----	Angst.

COMMENTS: These parameters seem normal.

V. CAPACITANCE PARAMETERS:	POLY	N DIFF	P DIFF	METAL 1	METAL 2	UNITS
Area Cap (Layer to subs)	.036	.128	.254	.027	.020	fF/um^2
Area Cap (Layer to Poly)	----	----	----	.049	.025	fF/um^2
Area Cap (Layer to Metal1)	----	----	----	----	.046	fF/um^2
Fringe Cap (Layer to subs)	----	.510	.313	----	----	fF/um

COMMENTS: These parameters seem normal.

VI. CIRCUIT PARAMETERS:			
Vinv, K = 1	1.95	V	
Vinv, K = 1.5	2.18	V	
Vlow, K = 2.0	0.00	V	
Vhigh, K = 2.0	4.99	V	
Vinv, K = 2.0	2.41	V	
Gain, K = 2.0	-10.80		
* * * Ring Oscillator Frequency	34.73	MHz	(31 stages @ 5.0V)

COMMENTS: The ring oscillator frequency is typical.

```
N13L  SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 LD=0.240703U TOX=407.000000E-10
+ NSUB=3.133604E+15 VTO=0.711043 KP=4.879000E-05 GAMMA=0.3801
+ PHI=0.6 UO=575.027 UEXP=0.129885 UCRIT=24726.9
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+ RSH=29.040000 CGDO=3.063325E-10 CGSO=3.063325E-10 CGBO=5.135289E-10
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+ RSH=87.160000 CGDO=3.181644E-10 CGSO=3.181644E-10 CGBO=6.682147E-10
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* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.04 um
```
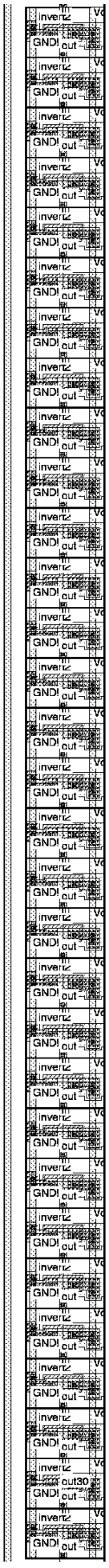



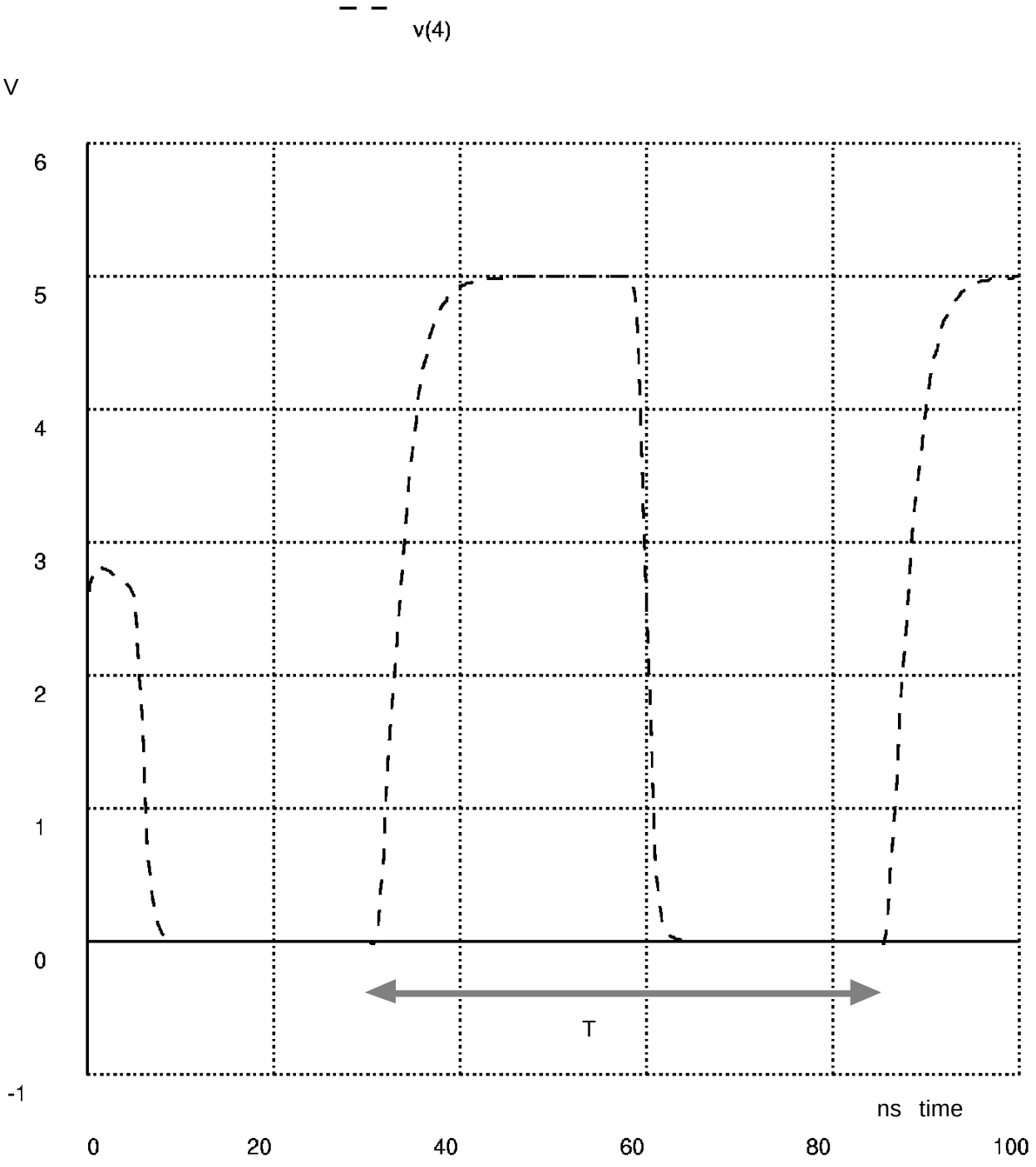
2 Micron Process

958 by 60 microns

N13L 2 micron process

18 MHz Simulated

34.73 MHz MOSIS Expected



Elec 422: VLSI Design I

Additional Information on 1.2 micron MOSIS Process

MOSIS PARAMETRIC TEST RESULTS - Feb. 1998

RUN: N81X VENDOR: AMI
TECHNOLOGY: SCN12 FEATURE SIZE: 1.2 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.56	-0.95	Volts
SHORT	10.8/1.2			
Vth		0.38	-0.71	Volts
Vpt		10.0	-6.7	Volts
Vbkd		15.0	-15.0	Volts
Idss		224	-105	uA/um
WIDE	30/1.2			
Ids0		1.6	-140.9	pA/um
LARGE	10.8/10.8			
Vth		0.55	-0.75	Volts
Vjbkd		17.1	-15.6	Volts
Ijlk		-5.8	7.5	pA
Gamma		0.62	0.54	V^0.5
Delta length		0.21	0.10	microns
(L_eff = L_drawn-DL)				
Delta width		1.25	1.31	microns
(W_eff = W_drawn-DW)				
K' (Uo*Cox/2)		35.0	-11.8	uA/V^2

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.6/2.4			
Vth		0.91	-0.95	Volts
SHORT	7.2/2.4			
Vth		0.89	-0.89	Volts
LARGE	21.6/21.			

Vth	0.88	-0.88	Volts
Delta length (L_eff = L_drawn-DL)	-0.03	-0.33	microns
Delta width (W_eff = W_drawn-DW)	1.43	1.96	microns
K' (Uo*Cox/2)	23.7	-8.1	uA/V^2

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta		106	
V_early		50.4	Volts
Vce,sat		0.2	Volts
2X2	2X2		
Beta		107	
V_early		50.6	Volts
Vce,sat		0.1	Volts
2X4	2X4		
Beta		108	
V_early		50.9	Volts
Vce,sat		0.1	Volts
2X8	2X8		
Beta		109	
V_early		51.0	Volts
Vce,sat		0.1	Volts
BVceo		11.6	Volts
BVcbo		29.3	Volts
BVebo		8.0	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Sheet Resistance	56.9	79.2	40.2	24.8	0.05	0.03	1530	ohms/sq
Width Variation (measured - drawn)	-0.50	-0.67	-0.18	0.19	0.33	0.24		microns
Contact Resistance	53.2	36.2	27.6	15.2		0.05		ohms
Gate Oxide Thickness	297							angstrom

PROCESS PARAMETERS	N\PLY	UNITS
Sheet Resistance	1565	ohms/sq
Width Variation (measured - drawn)		microns
Contact Resistance		ohms

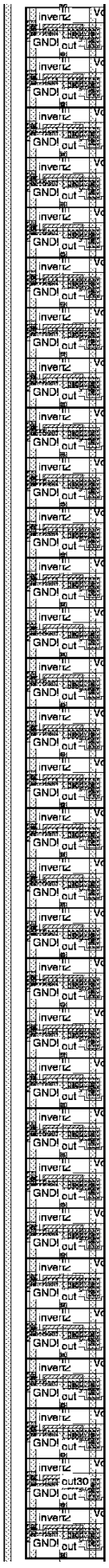
COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	METAL1	METAL2	UNITS
Area (substrate)	282	294	36		20	13	aF/um^2
Area (N+active)			1161	770	48	27	aF/um^2
Area (P+active)			1139	762			aF/um^2
Area (poly)				648	45	24	aF/um^2
Area (poly2)					45		aF/um^2
Area (metal1)						44	aF/um^2

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	1.92	Volts
Vinv	1.5	2.25	Volts
Vol (100 uA)	2.0	0.55	Volts
Voh (100 uA)	2.0	4.36	Volts
Vinv	2.0	2.46	Volts
Gain	2.0	-9.28	
Ring Oscillator Freq.			
MOSIS (31-stage,5V)		70.78	MHz

N81X SPICE LEVEL3 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=2.9700E-08 XJ=0.200000U TPG=1
+ VTO=0.5597 DELTA=9.3220E-01 LD=6.5780E-08 KP=7.8748E-05
+ UO=677.3 THETA=1.0950E-01 RSH=2.9330E+01 GAMMA=0.5743
+ NSUB=1.3430E+16 NFS=7.1500E+11 VMAX=1.8650E+05 ETA=8.3910E-02
+ KAPPA=1.5110E-01 CGDO=1.1472E-10 CGSO=1.1472E-10
+ CGBO=3.3855E-10 CJ=2.7107E-04 MJ=5.2656E-01 CJSW=1.5072E-10
+ MJSW=1.0000E-01 PB=9.1954E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 8.7580E-07
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=2.9700E-08 XJ=0.200000U TPG=-1
+ VTO=-0.7595 DELTA=2.2970E+00 LD=1.1000E-09 KP=2.3440E-05
+ UO=201.6 THETA=1.2730E-01 RSH=8.4110E-01 GAMMA=0.3238
+ NSUB=4.2700E+15 NFS=6.4990E+11 VMAX=1.9020E+05 ETA=1.3470E-01
+ KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.3325E-10 CJ=2.9032E-04 MJ=4.5540E-01 CJSW=1.8518E-10
+ MJSW=1.0904E-01 PB=8.0729E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 8.5120E-07
```



1.2 micron process

574 by 36 microns

```
| units: 60 tech: scmos
p out31 invert2_0[1]/in Vdd 2 3 14 30
n out31 GND invert2_0[1]/in 2 3 15 8
p invert2_0[1]/in invert2_0[2]/in Vdd 2 3 44 30
n invert2_0[1]/in GND invert2_0[2]/in 2 3 45 8
p invert2_0[2]/in invert2_0[3]/in Vdd 2 3 74 30
n invert2_0[2]/in GND invert2_0[3]/in 2 3 75 8
p invert2_0[3]/in invert2_0[4]/in Vdd 2 3 104 30
n invert2_0[3]/in GND invert2_0[4]/in 2 3 105 8
p invert2_0[4]/in invert2_0[5]/in Vdd 2 3 134 30
n invert2_0[4]/in GND invert2_0[5]/in 2 3 135 8
p invert2_0[5]/in invert2_0[6]/in Vdd 2 3 164 30
n invert2_0[5]/in GND invert2_0[6]/in 2 3 165 8
p invert2_0[6]/in invert2_0[7]/in Vdd 2 3 194 30
n invert2_0[6]/in GND invert2_0[7]/in 2 3 195 8
p invert2_0[7]/in invert2_0[8]/in Vdd 2 3 224 30
n invert2_0[7]/in GND invert2_0[8]/in 2 3 225 8
p invert2_0[8]/in invert2_0[9]/in Vdd 2 3 254 30
n invert2_0[8]/in GND invert2_0[9]/in 2 3 255 8
p invert2_0[9]/in invert2_0[9]/out Vdd 2 3 284 30
n invert2_0[9]/in GND invert2_0[9]/out 2 3 285 8
p invert2_0[9]/out invert2_0[11]/in Vdd 2 3 314 30
n invert2_0[9]/out GND invert2_0[11]/in 2 3 315 8
p invert2_0[11]/in invert2_0[12]/in Vdd 2 3 344 30
n invert2_0[11]/in GND invert2_0[12]/in 2 3 345 8
p invert2_0[12]/in invert2_0[13]/in Vdd 2 3 374 30
n invert2_0[12]/in GND invert2_0[13]/in 2 3 375 8
p invert2_0[13]/in invert2_0[14]/in Vdd 2 3 404 30
n invert2_0[13]/in GND invert2_0[14]/in 2 3 405 8
p invert2_0[14]/in invert2_0[15]/in Vdd 2 3 434 30
n invert2_0[14]/in GND invert2_0[15]/in 2 3 435 8
p invert2_0[15]/in invert2_0[16]/in Vdd 2 3 464 30
n invert2_0[15]/in GND invert2_0[16]/in 2 3 465 8
p invert2_0[16]/in invert2_0[17]/in Vdd 2 3 494 30
n invert2_0[16]/in GND invert2_0[17]/in 2 3 495 8
p invert2_0[17]/in invert2_0[18]/in Vdd 2 3 524 30
n invert2_0[17]/in GND invert2_0[18]/in 2 3 525 8
p invert2_0[18]/in invert2_0[19]/in Vdd 2 3 554 30
n invert2_0[18]/in GND invert2_0[19]/in 2 3 555 8
p invert2_0[19]/in invert2_0[20]/in Vdd 2 3 584 30
n invert2_0[19]/in GND invert2_0[20]/in 2 3 585 8
p invert2_0[20]/in invert2_0[21]/in Vdd 2 3 614 30
n invert2_0[20]/in GND invert2_0[21]/in 2 3 615 8
p invert2_0[21]/in invert2_0[22]/in Vdd 2 3 644 30
n invert2_0[21]/in GND invert2_0[22]/in 2 3 645 8
p invert2_0[22]/in invert2_0[23]/in Vdd 2 3 674 30
n invert2_0[22]/in GND invert2_0[23]/in 2 3 675 8
p invert2_0[23]/in invert2_0[24]/in Vdd 2 3 704 30
n invert2_0[23]/in GND invert2_0[24]/in 2 3 705 8
p invert2_0[24]/in invert2_0[25]/in Vdd 2 3 734 30
n invert2_0[24]/in GND invert2_0[25]/in 2 3 735 8
p invert2_0[25]/in invert2_0[26]/in Vdd 2 3 764 30
n invert2_0[25]/in GND invert2_0[26]/in 2 3 765 8
p invert2_0[26]/in invert2_0[27]/in Vdd 2 3 794 30
n invert2_0[26]/in GND invert2_0[27]/in 2 3 795 8
p invert2_0[27]/in invert2_0[28]/in Vdd 2 3 824 30
n invert2_0[27]/in GND invert2_0[28]/in 2 3 825 8
p invert2_0[28]/in invert2_0[29]/in Vdd 2 3 854 30
```

irsim format sim file for 31 stage ring oscillator for 1.2 micron process

```
n invert2_0[28]/in GND invert2_0[29]/in 2 3 855 8
p invert2_0[29]/in out30 Vdd 2 3 884 30
n invert2_0[29]/in GND out30 2 3 885 8
p out30 out31 Vdd 2 3 914 30
n out30 GND out31 2 3 915 8
C out31 GND 146
C out30 GND 19
C Vdd GND 310
C invert2_0[29]/in GND 18
C invert2_0[28]/in GND 18
C invert2_0[27]/in GND 18
C invert2_0[26]/in GND 18
C invert2_0[25]/in GND 18
C invert2_0[24]/in GND 18
C invert2_0[23]/in GND 18
C invert2_0[22]/in GND 18
C invert2_0[21]/in GND 18
C invert2_0[20]/in GND 18
C invert2_0[19]/in GND 18
C invert2_0[18]/in GND 18
C invert2_0[17]/in GND 18
C invert2_0[16]/in GND 18
C invert2_0[15]/in GND 18
C invert2_0[14]/in GND 18
C invert2_0[13]/in GND 18
C invert2_0[12]/in GND 18
C invert2_0[11]/in GND 18
C invert2_0[9]/out GND 18
C invert2_0[9]/in GND 18
C invert2_0[8]/in GND 18
C invert2_0[7]/in GND 18
C invert2_0[6]/in GND 18
C invert2_0[5]/in GND 18
C invert2_0[4]/in GND 18
C invert2_0[3]/in GND 18
C invert2_0[2]/in GND 18
C invert2_0[1]/in GND 18
```

```
*
* Elec422 SPICE EXPERIMENT TEMPLATE;
* ----------------------------------

* Set BASIC VOLTAGE levels
vdd <Vdd>  <GND>  dc 5
* set substrate voltages : P-sub = Vdd;  N-sub = GND
vs1 <CMOSP> <Vdd>  dc 0
vs2 <CMOSN> <GND>  dc 0

* ----------------------------------

* ----------------------------------


.ic v(<out31>) = 2.5

* Do analysis: give increments and total time for analysis.
.tran .25ns 100ns UIC
*
*
* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages, for example a, sum, cout
.plot tran v(<out31>)
* reminders-hints... enter in interactive spice window
* set hcopydevtype=postscript
* hardcopy filename.spiceps v(above_node_numbers)
*

.end
```

Spice Experiment File

1.2 micron process
N81X AMI process parameters

70.78 MHz MOSIS Expected

66 MHz Simulated