MOSIS Scalable CMOS (SCMOS) Design Rules

(Revision 7.2)

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1 Introduction

1.1 SCMOS Design Rules

This document defines the official MOSIS scalable CMOS (SCMOS) layout rules. It supersedes all previous revisions.

In the SCMOS rules, circuit geometries are specified in the Mead and Conway's lambda based methodology [1]. The unit of measurement, lambda, can easily be scaled to different fabrication processes as semiconductor technology advances.

Each design has a **technology-code** associated with the layout file. At the moment, three technology-codes are used to specify the basic CMOS process. Each technology-code may have one or more associated **options** added for the purpose of specifying either (a) special features for the target process or (b) the presence of novel devices in the design. At the time of this revision, MOSIS is offering six CMOS processes from three different foundries with feature sizes from 2.0 micron to 0.5 micron.

2 Standard SCMOS

The standard CMOS technology accessed by MOSIS is a single polysilicon, double metal, bulk CMOS process with enhancement-mode n-MOSFET and p-MOSFET devices [3].

2.1 Well Type

Three technology-codes are used to indicate the well type (substrate) used for fabrication (as shown in Table 1).

Technology-Code	Description
SCN	Scalable CMOS N-well
SCP	Scalable CMOS P-well
SCE	Scalable CMOS Either-well

Table 1: SCMOS well types

The SCN and SCP technology-codes are used when submitting a design for fabrication in a process of the specified well. For convenience, in either case, the layout file may contain the 'other' well, but it will always be ignored.

Designs specifying the SCE technology-code may be fabricated in any CMOS process, N-well or P-well (either) and must include both wells (and correspondingly, well/substrate contacts for proper bias). For any given fabrication process the 'other' well be ignored during mask generation. If twin-tub processes are offered in the future, both wells will be used. **Note:** Currently MOSIS only offers n-well processes.

2.2 SCMOS Options

SCMOS options are used to designate projects that use additional layers beyond the standard single-poly, double metal CMOS. Each option is called out with a designator that is appended to the basic technology-code. Please note that not all possible combinations are available. The current list is shown in Table 2.

Designation	Long Form	Description
E	Electrode	Adds a second polysilicon layer (electrode) that can serve either as the upper electrode of a poly capacitor or as a gate for transistors.
A	Analog	Adds electrode (as in E option), plus layers for vertical NPN transistor pbase and buried CCDs.
3M	Triple Metal	Adds second via (via2) and third metal (metal3) layers.
4M	Quad Metal	Adds 3M plus third via (via3) and fourth metal (metal4) layers.
LC	Linear Capacitor	Adds a cap_well layer for linear capacitors.
_MEMS	Micro Machining	Adds mems_open and mems_etch_stop for CMOS-compatible MEMS devices.
_SUBM	Sub Micron	Uses revised layout rules for better fit to submicron processes (see section 2.4).

Table 2: SCMOS technology options

In addition to the options in Table 2, two undeclared options exist. The first is for high voltage

MOSFET. The second is for a tight metal rule for metal interconnect. For options available to specific processes, see Tables 3a and 3b.

Foundry	Process	Lambda	Options
Orbit	2.0um N-well	1.0um	SCNA, SCNE, SCN, SCNA_MEMS
AMI	ABN (1.2um N-well)	0.6um	SCNA(1), SCNE, SCN, High Voltage
HP	CMOS34 / AMOSI (1.2um N-well)	0.6um	SCNLC, SCN, Tight Metal
HP	CMOS26G (0.8um N-well)	0.5um	SCN3M, SCN, Tight Metal
AMI	CWL (0.8um N-well)	0.5um	SCNPC, Tight Metal
HP	GMOS14TB/AMOS14TB (0.5um N-well)	0.35um	SCN3M, SCN, SCN3MLC, SCNLC, Tight Metal
HP	GMOS10QA (0.35um N-well)	0.25um	SCN4N, Tight Metal

Table 3a: MOSIS SCMOS-compatible mappings

Foundry	Process	Lambda	Options
HP	CMOS26G (0.8um N-well)	0.4um	SCN3M_SUBM, SCN_SUBM
HP	GMOS14TB/AMOS14TB (0.5um N-well)	0.3um	SCN3M_SUBM, SCN_SUBM, SCN3MLC_SUBM, SCNLC_SUBM
HP	GMOS10QA (0.35um N-well)	0.2um	SCN4M_SUBM

Table 3b: MOSIS SCMOS_SUBM-compatible mappings

2.3 SCMOS-compatible processes

MOSIS currently offers the fabrication processes shown above in Tables 3a and 3b. For each process the list of appropriate SCMOS technology-codes is shown. Note that whenever SCNxx appears, SCExx is also appropriate.

2.4 SCMOS_SUBM - Sub Micron Rules

The SCMOS layout rules were historically developed for 1.0 to 3.0 micron processes. To take full advantage of advanced submicron processes, the SCMOS rules were revised to create SCMOS_SUBM. By increasing the lambda size for some rules (those that didn’t shrink as fast in practice as did the overall scheme of things), the submicron rules allow for use of a smaller value of lambda, and better fit to these small feature size processes. Table 4 lists the differences between SCMOS, SCMOS tight metal and SCMOS sub-micron.

Description	Rule	SCMOS	SCMOS tight metal	SCMOS sub-micron
Well width	1.1	10	10	12
Well space (different potential)	1.2	9	9	18
Well overlap (space) to transistor	2.3	5	5	6
Poly space	3.2	2	2	3
Contact space	5.3, 6.3	2	2	3
Metal1 space	7.2	3	2	3
Via on flat	8.5	2	2	unrestricted
Metal2 space	9.2	4	3	3
Metal3 width	15.1	6	6	5
Metal3 space	15.2	4	4	3

Table 4: SCMOS, SCMOS tight metal, SCMOS Sub-micron differences

3 CIF and GDS layer specification

A user design submitted to MOSIS using the SCMOS rules can be in either Calma GDSII format [2] or Caltech Intermediate Form (CIF version 2.0) [1]. The two are completely interchangable. Note that all submitted cif and gds files have already been scaled before submission, and are always in absolute metric units -- never in lambda units.

GDSII is a binary format, while CIF is a plain ASCII text. For detailed syntax and semantic specifications of GDS and CIF, refer to [2] and [1] respectively.

In GDS format, a design layer is specified as a number between 0 and 255 (formerly 63). MOSIS SCMOS now reserves layer numbers 21 through 62, inclusive, for drawn layout. Layers 0 through 20 plus layers 63 and above can be used by designers for their own purposes and will be ignored by MOSIS.

In this revision, nine new layers were added as shown below:

P-high-voltage is used to indicate high-voltage p-type areas.

N-high-voltage is used to indicate high-voltage n-type areas.

MEMS-open is used to indicate substrate pit opening area for MEMS devices.

MEMS-etch-stop is used to indicate substrate p+ etch-stop area for MEMS devices.

Contact replaces the previously separate poly-contact, active-contact and electrode-contact layers.

Pads is used to indicate bonding pad locations.

Explicit field implant denotes the field implant reversal layer.

Poly-cap supports the AMI-style linear capacitor called SCNPC. It has the regular (two-metal) SCN layers, plus the new layer POLY_CAP1.

Silicide block is used for blocking the siliciding of poly and/or active.

Users should be aware that there is only one contact mask layer, although several separate layers were defined and are retained for backward compatibility. A complete list of SCMOS layers is shown in Table 5.

SCMOS layer	CIF name	GDS2 number	SCMOS layer	CIF name	GDS2 number
P-high-voltage	CVP	21	Poly	CPG	46
N-high-voltage	CVN	22	Contact	CCG	25
MEMS-open	COP	23	Metal1	CMF	49
MEMS-etch-stop	CPS	24	Via	CVA	50
Pad	XP	26	Metal2	CMS	51
Explicit field implant	CFI	27	Glass	COG	52
Poly-cap	CPC	28	Electrode	CEL	56
Silicide block	CSB	29	Buried-CCD	CCD	57
P-well	CWP	41	P-base	CBA	58
N-well	CWN	42	Cap-well	CWC	59
Active	CAA	43	Via2	CVS	61
P-plus-select	CSP	44	Metal3	CMT	62
N-plus-select	CSN	45	Via3	CVT	30
-	-	-	Metal4	CMQ	31

Table 5: SCMOS layer map

References

[1] C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley, 1980

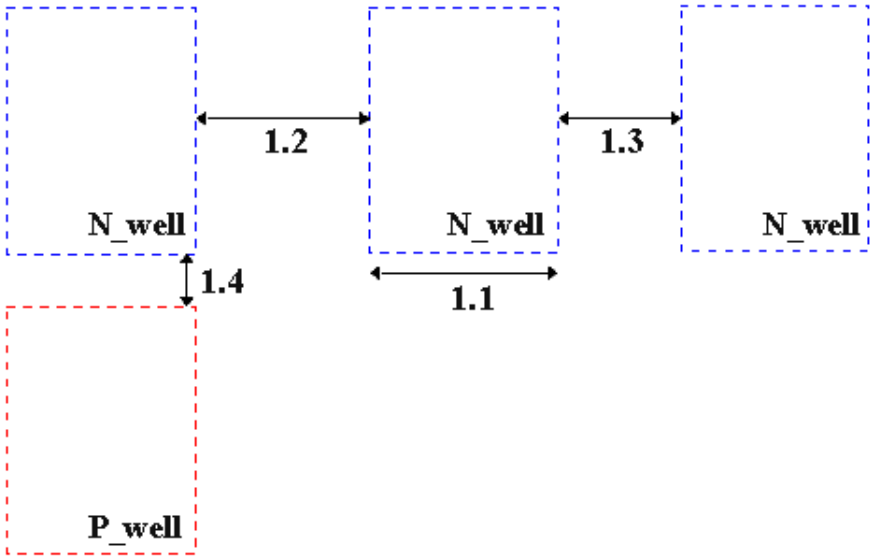
[2] Cadence Design Systems, Inc./Calma. *GDSII Stream Format Manual*, Feb. 1987, Release 6.0, Documentation No. B97E060

[3] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A System Perspective*, Addison-Wesley, 2nd edition, 1993

SCMOS Layout Rules - Well

Rule	Description	Lambda
1.1	Minimum width	10 [SUBM 12]
1.2	Minimum spacing between wells at different potential	9 [SUBM 18]
1.3	Minimum spacing between wells at same potential	0 or 6
1.4	Minimum spacing between wells of different type (if both are drawn)	0

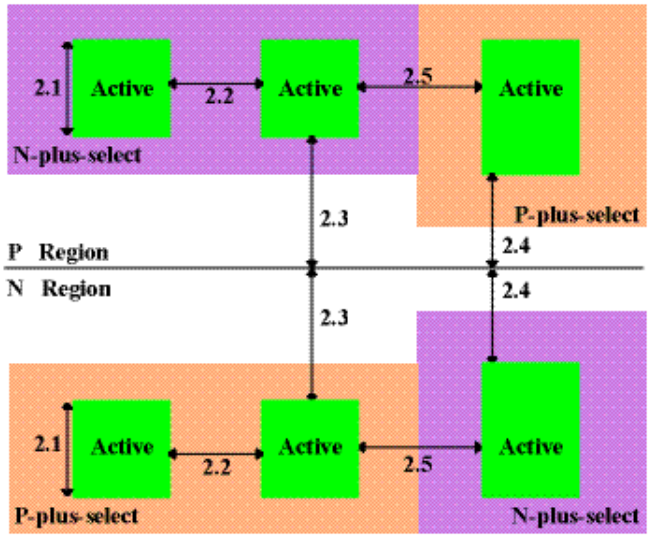
Table 6: SCMOS Layout Rules - Well



SCMOS Layout Rules - Active

Rule	Description	Lambda
2.1	Minimum width	3
2.2	Minimum spacing	3
2.3	Source/drain active to well edge	5 [SUBM 6]
2.4	Substrate/well contact active to well edge	3
2.5	Minimum spacing between active of different implant	0 or 4

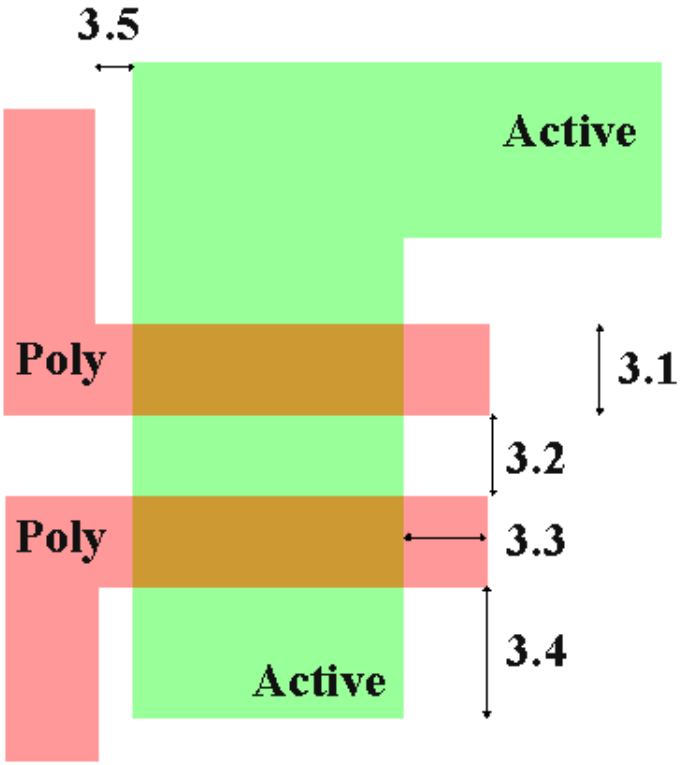
Table 7: SCMOS Layout Rules - Active



SCMOS Layout Rules - Poly

Rule	Description	Lambda
3.1	Minimum width	2
3.2	Minimum spacing	2 [SUBM 3]
3.3	Minimum gate extension of active	2
3.4	Minimum active extension of poly	3
3.5	Minimum field poly to active	1

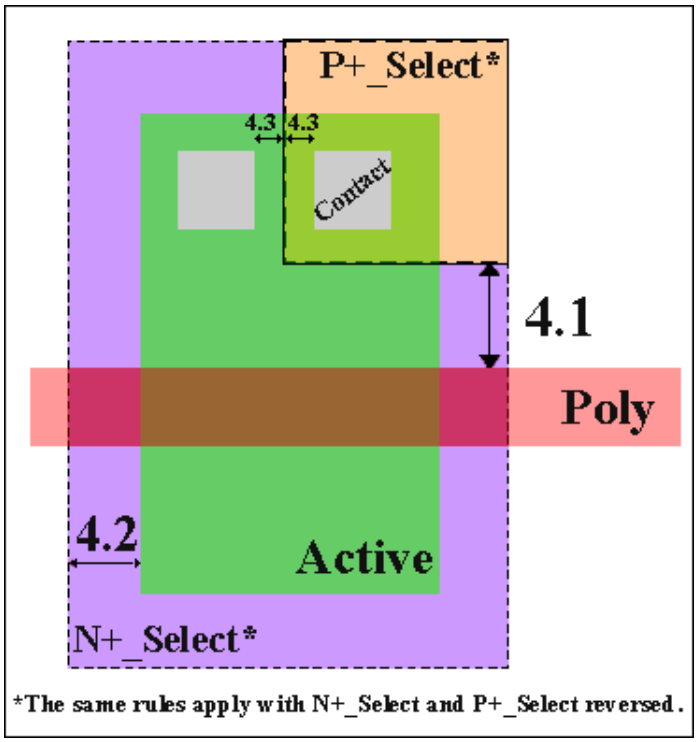
Table 8: SCMOS Layout Rules - Poly



SCMOS Layout Rules - Select

Rule	Description	Lambda
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3
4.2	Minimum select overlap of active	2
4.3	Minimum select overlap of contact	1
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2

Table 9: SCMOS Layout Rules - Select

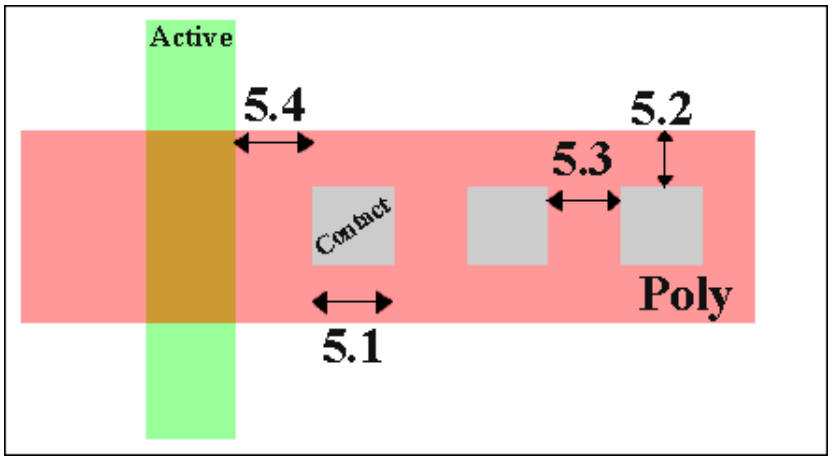


SCMOS Layout Rules - Simple Contact to Poly

On HP's CMOS14 process (and probably on all subsequent processes as they evolve), HP requires that ALL features on the insulator layers (CONTACT, VIA, VIA2) MUST BE of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings.

Rule	Description	Lambda
5.1	Exact contact size	2 x 2
5.2	Minimum poly overlap	1.5
5.3	Minimum contact spacing	2 [SUBM 3]
5.4	Minimum spacing to gate of transistor	2

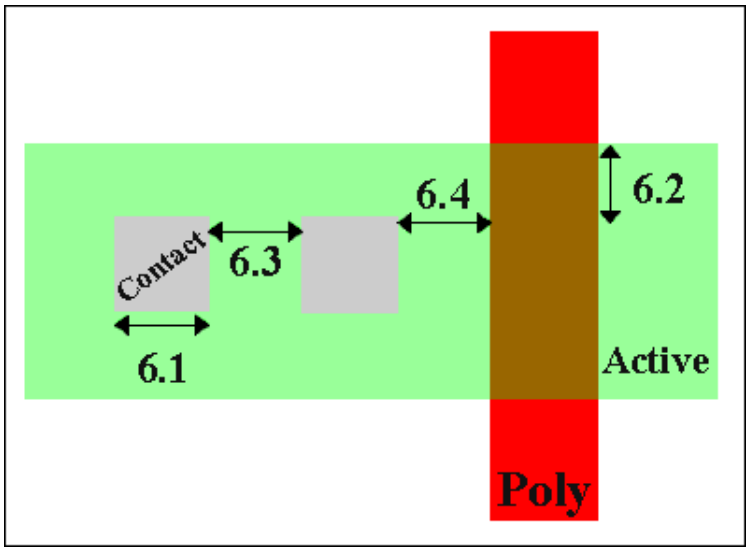
Table 10: SCMOS Layout Rules - Simple Contact to Poly



SCMOS Layout Rules - Simple Contact to Active

Rule	Description	Lambda
6.1	Exact contact size	2 x 2
6.2	Minimum active overlap	1.5
6.3	Minimum contact spacing	2 [SUBM 3]
6.4	Minimum spacing to gate of transistor	2

Table 11: SCMOS Layout Rules - Simple Contact to Active

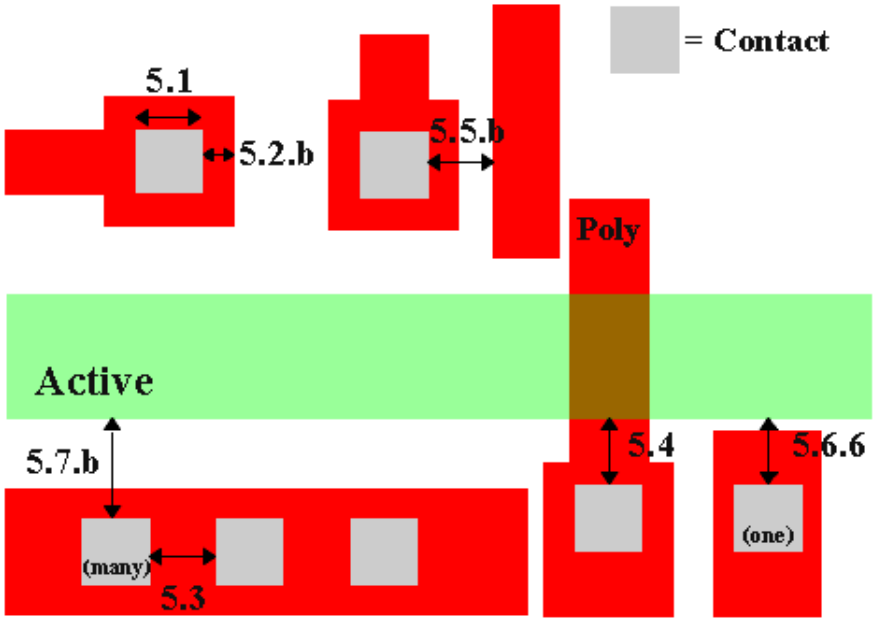


SCMOS Layout Rules - Alternative Contact to Poly

The rules above are preferred. If, however, one cannot handle the 1.5 lambda contact overlap in 5.2, then that rule, 5.2, may be replaced by these rules, which reduce the overlap, but increase the spacing to surrounding features. The remaining rules above, 5.1, 5.3, and 5.4, still apply as originally stated.

Rule	Description	Lambda
5.2.b	Minimum poly overlap	1
5.5.b	Minimum spacing to other poly	4 [SUBM 5]
5.6.b	Minimum spacing to active (one contact)	2
5.7.b	Minimum spacing to active (many contacts)	3

Table 12: SCMOS Layout Rules - Alternative Contact to Poly

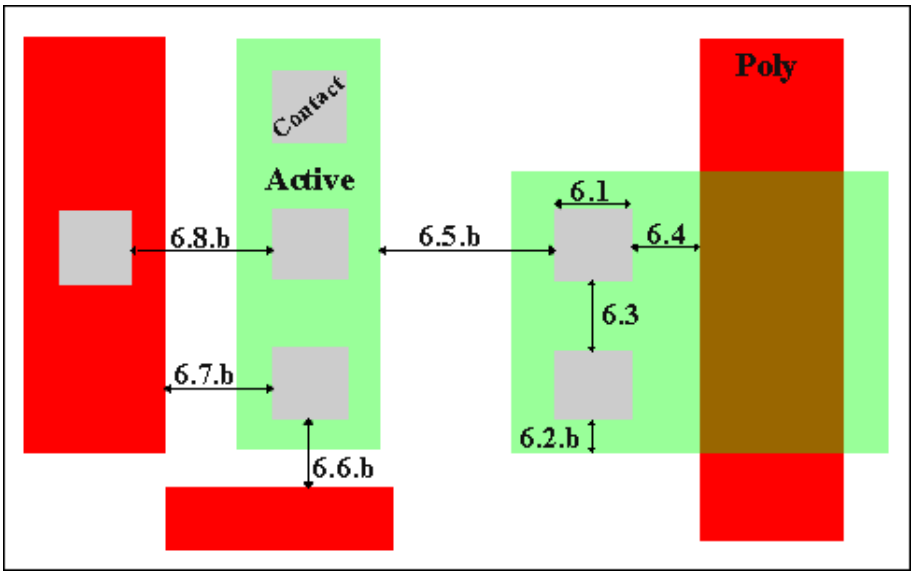


SCMOS Layout Rules - Alternative Contact to Active

The rules above are preferred. If, however, one cannot handle the 1.5 lambda contact overlap in 6.2, then that rule, 6.2, may be replaced by these rules, which reduce the overlap, but increase the spacing to surrounding features. The remaining rules above, 6.1, 6.3, and 6.4, still apply as originally stated.

Rule	Description	Lambda
6.2.b	Minimum active overlap	1
6.5.b	Minimum spacing to diffusion active	5
6.6.b	Minimum spacing to field poly (one contact)	2
6.7.b	Minimum spacing to field poly (many contacts)	3
6.8.b	Minimum spacing to poly contact	4

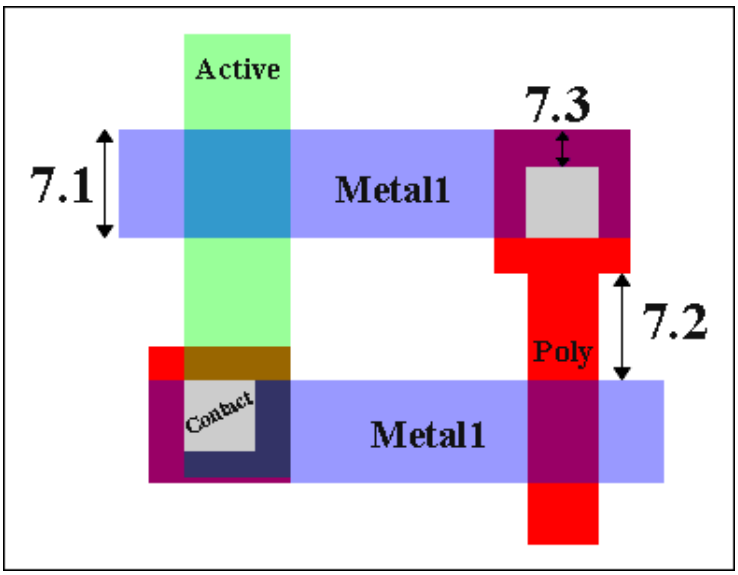
Table 13: SCMOS Layout Rules - Alternative Contact to Active



SCMOS Layout Rules - Metal1

Rule	Description	Lambda
7.1	Minimum width	3
7.2.a	Minimum spacing	3
7.2.b	Minimum tight metal spacing *(only allowed between minimum width wires - otherwise, use regular spacing rule)*	2
7.3	Minimum overlap of any contact	1

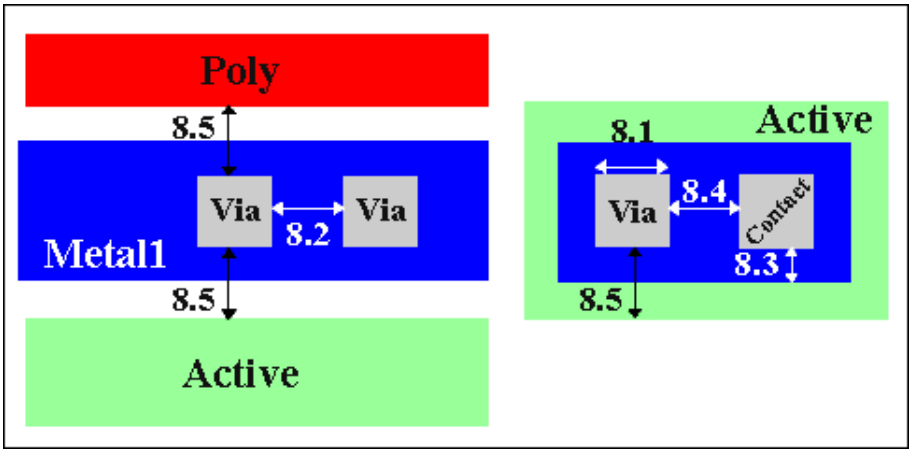
Table 14: SCMOS Layout Rules - Metal1



SCMOS Layout Rules - Via1

Rule	Description	Lambda
8.1	Exact size	2 x 2
8.2	Minimum via1 spacing	3
8.3	Minimum overlap by metal1	1
8.4	Minimum spacing to contact	2
8.5	Minimum spacing to poly or active edge	2

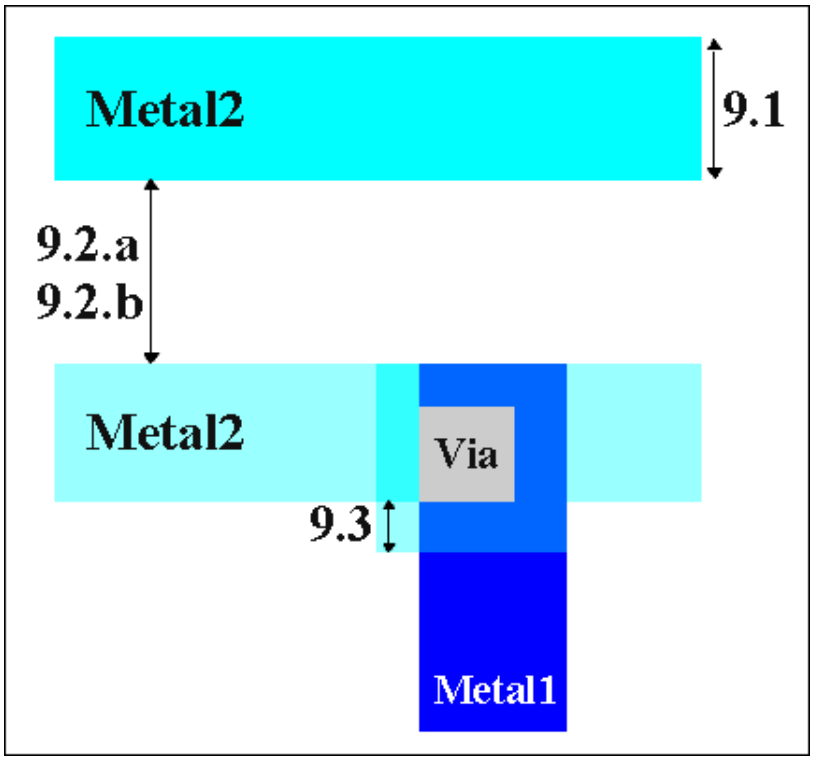
Table 15: SCMOS Layout Rules - Via1



SCMOS Layout Rules - Metal2

Rule	Description	Lambda
9.1	Minimum width	3
9.2.a	Minimum spacing	4
9.2.b	Minimum tight metal or SUBM spacing *(only allowed between minimum width wires - otherwise, use regular spacing rule)*	3
9.3	Minimum overlap of via1	1

Table 16: SCMOS Layout Rules - Metal2

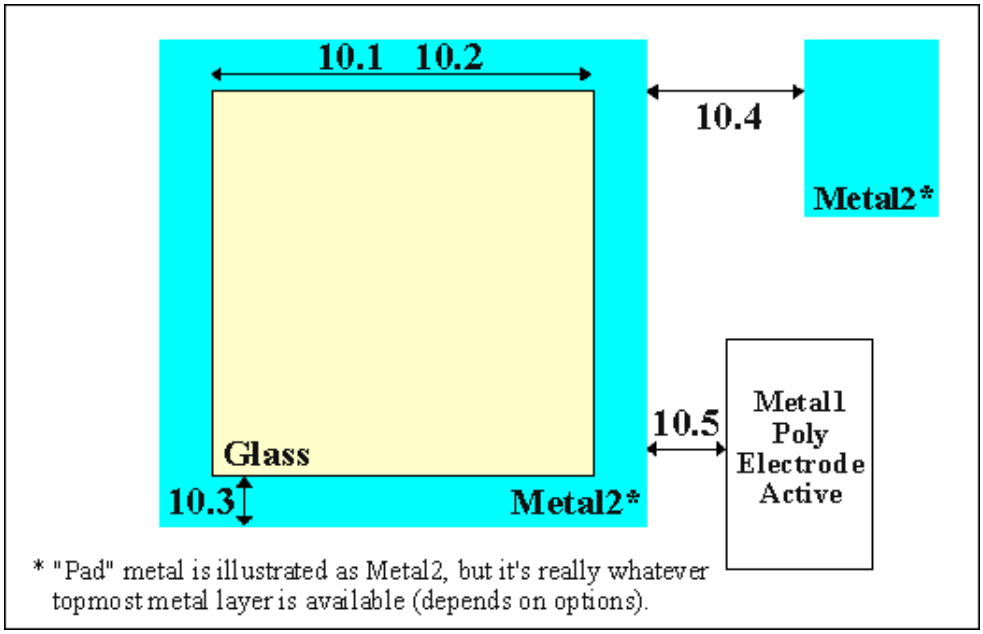


SCMOS Layout Rules - Overglass

Note that rules in this section are in units of microns. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.

Rule	Description	Microns
10.1	Minimum bonding pad width	100 x 100
10.2	Minimum probe pad width	75 x 75
10.3	Pad metal overlap of glass opening	6
10.4	Minimum pad spacing to unrelated metal2 *(and metal3 if triple metal is used)*	30
10.5	Minimum pad spacing to unrelated metal1, poly, electrode or active	15

Table 17: SCMOS Layout Rules - Overglass

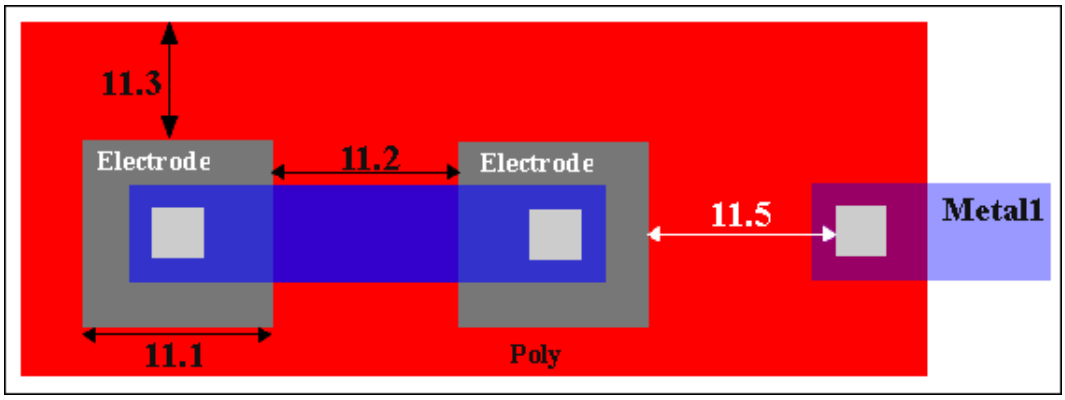


SCMOS Layout Rules - Electrode for Capacitor (Analog Option)

The new layer in this option is the electrode layer, which is a second polysilicon layer (physically above the standard, or first, poly layer). The oxide between the two polys is the capacitor dielectric. The capacitor area is the area of coincident poly and electrode.

Rule	Description	Lambda
11.1	Minimum width	3
11.2	Minimum spacing	3
11.3	Minimum poly overlap	2
11.4	Minimum spacing to active or well edge (not illustrated)	2
11.5	Minimum spacing to poly contact	3

Table 18: SCMOS Layout Rules - Electrode for Capacitor (Analog Option)

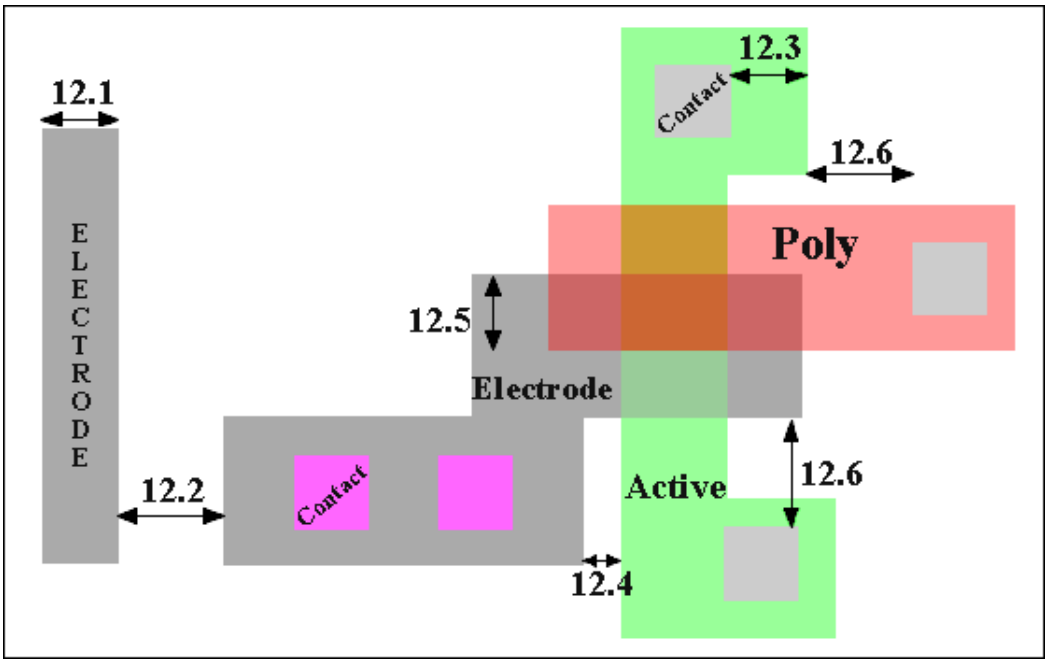


SCMOS Layout Rules - Electrode for Transistor (Analog Option)

Same electrode (second poly) layer as above.

Rule	Description	Lambda
12.1	Minimum width	2
12.2	Minimum spacing	3
12.3	Minimum electrode gate overlap of active	2
12.4	Minimum spacing to active	1
12.5	Minimum spacing or overlap of poly	2
12.6	Minimum spacing to poly or active contact	3

Table 19: SCMOS Layout Rules - Electrode for Transistor (Analog Option)

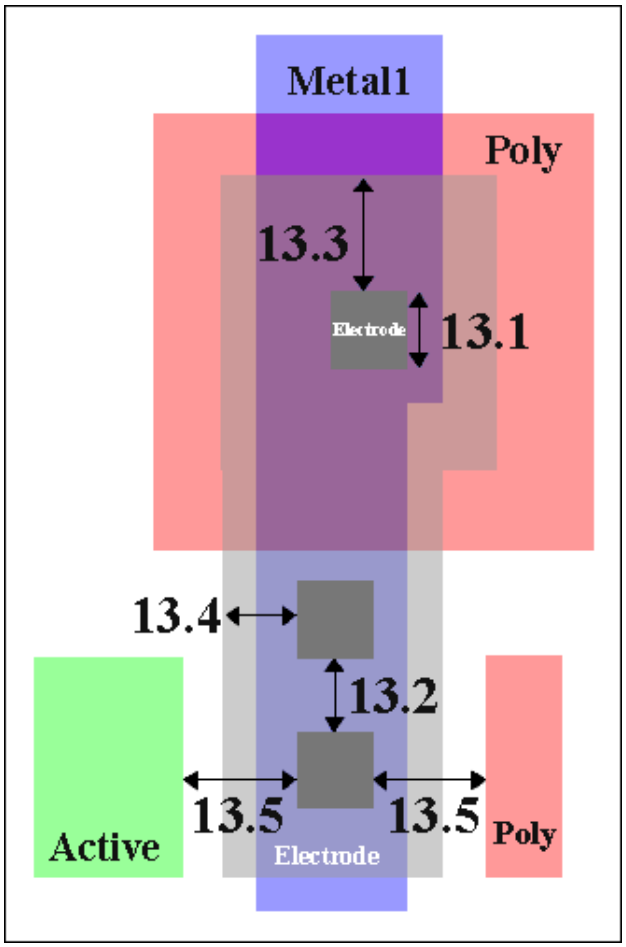


SCMOS Layout Rules - Electrode Contact (Analog Option)

The electrode is contacted through the standard contact layer, similar to the first poly. The overlap numbers are larger, however.

Rule	Description	Lambda
13.1	Exact contact size	2 x 2
13.2	Minimum contact spacing	2
13.3	Minimum electrode overlap (on capacitor)	3
13.4	Minimum electrode overlap (not on capacitor)	2
13.5	Minimum spacing to poly or active	3

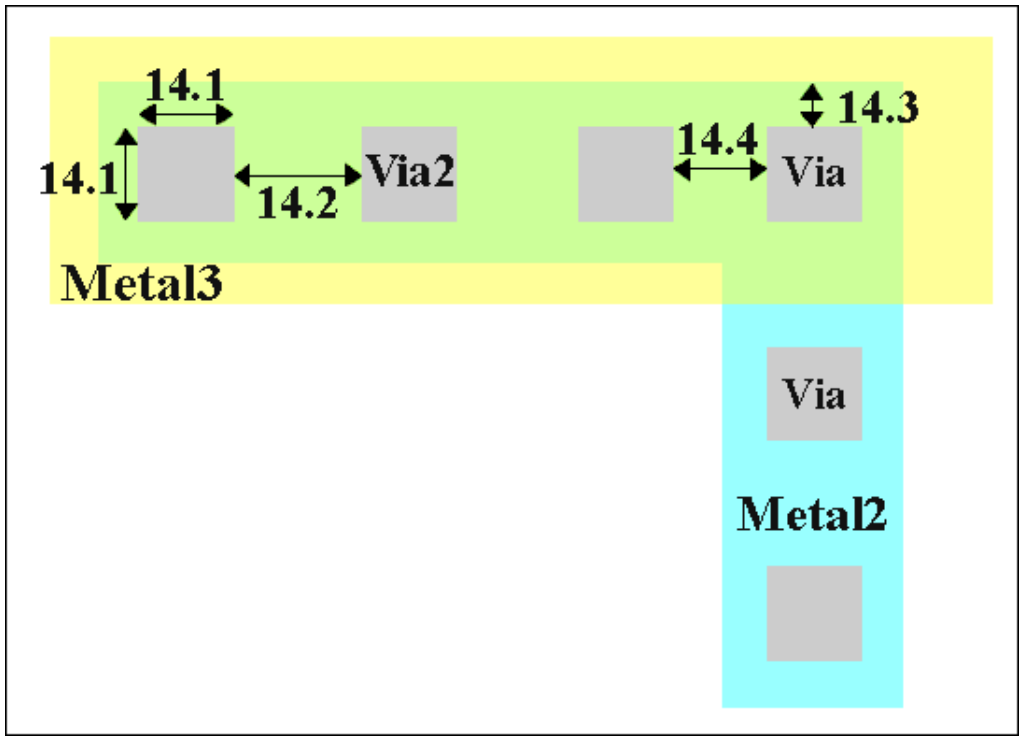
Table 20: SCMOS Layout Rules - Electrode Contact (Analog Option)



SCMOS Layout Rules - Via2 (Triple Metal Option)

Rule	Description	Lambda
14.1	Exact size	2 x 2
14.2	Minimum spacing	3
14.3	Minimum overlap by metal2	1
14.4	Minimum spacing to via1	2
14.5	Via2 may be placed over contact	

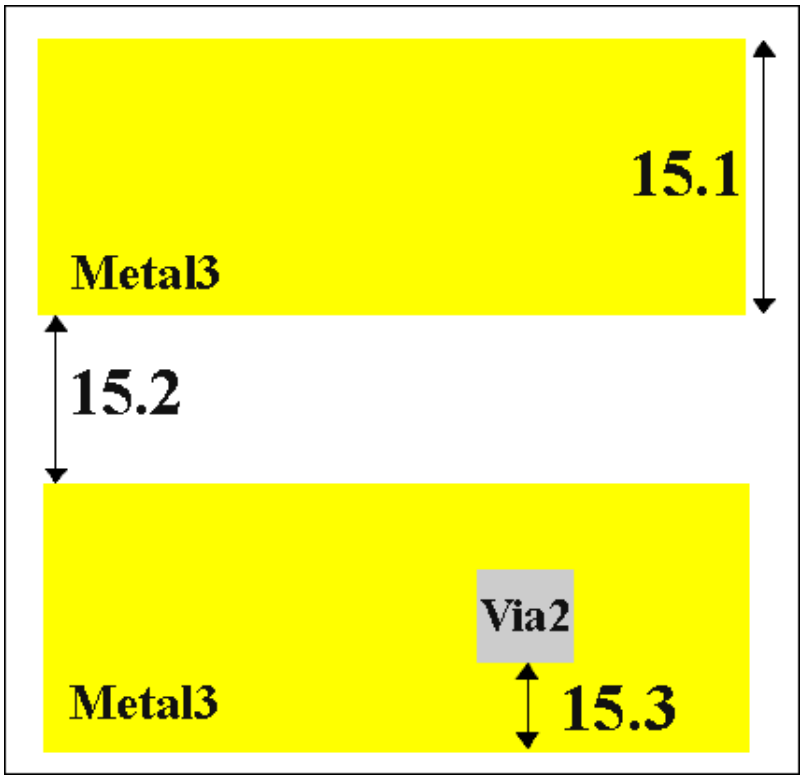
Table 21: SCMOS Layout Rules - Via2 (Triple Metal Option)



SCMOS Layout Rules - Metal3 (Triple Metal Option)

Rule	Description	Lambda
15.1	Minimum width	6 [SUBM 5]
15.2	Minimum spacing to metal3	4 [SUBM 3]
15.3	Minimum overlap of via2	2

Table 22: SCMOS Layout Rules - Metal3 (Triple Metal Option)

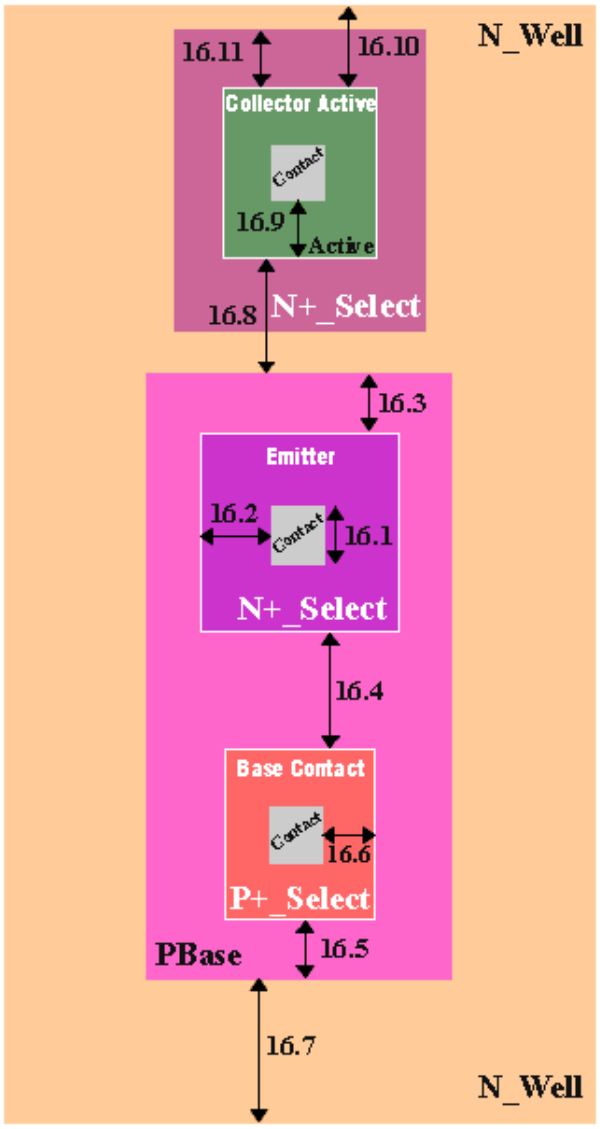


SCMOS Layout Rules - NPN Bipolar Transistor (Analog Option)

The new layer in this option is the pbase layer, which is an active area that is implanted with the pbase implant to form the base. The base contact is enclosed in p-select. The emitter is an n-select region within (and on top of) the base. The entire pbase sits in an n-well that is the collector. The collector contact is a well contact, but the overlaps are larger.

Rule	Description	Lambda
16.1	All active contact	2 x 2
16.2	Minimum emitter select overlap of contact	3
16.3	Minimum pbase overlap of emitter select	2
16.4	Minimum spacing between emitter select and base select	4
16.5	Minimum pbase overlap of base select	2
16.6	Minimum base select overlap of contact	2
16.7	Minimum nwell overlap of pbase	6
16.8	Minimum spacing between pbase and collector active	4
16.9	Minimum collector active overlap of contact	2
16.10	Minimum nwell overlap of collector active	3
16.11	Minimum select overlap of collector active	2

Table 23: SCMOS Layout Rules - NPN Bipolar Transistor (Analog Option)

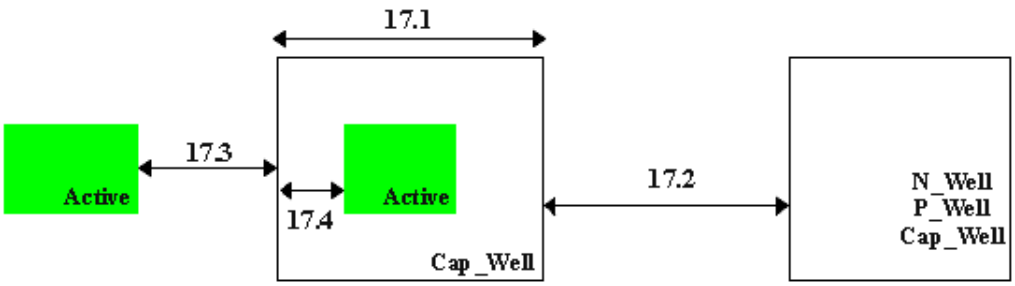


SCMOS Layout Rules - Capacitor Well (Linear Capacitor Option)

This illustration applies only to CMOS34. Note that the smaller values apply only to CMOS34; the larger values apply to CMOS14.

Rule	Description	Lambda
17.1	Minimum width	10 [SUBM 12]
17.2	Minimum spacing	9 [SUBM 18]
17.3	Minimum spacing to external active	5 [SUBM 6]
17.4	Minimum overlap of active (This rule was 3 lambda for CMOS34 process use, and that smaller value is still acceptable for layout intended for that process only.)	5 [SUBM 6]

Table 24: SCMOS Layout Rules - Capacitor Well (Linear Capacitor Option)

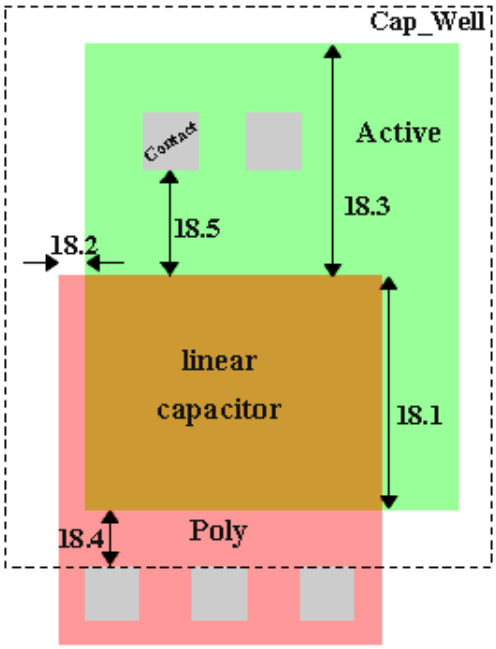


SCMOS Layout Rules - Linear Capacitor (Linear Capacitor Option)

This illustration applies only to CMOS34. Note that the smaller values apply only to CMOS34; the larger values apply to CMOS14.

Rule	Description	Lambda
18.1	Minimum width	3
18.2	Minimum poly extension of active	1/2
18.3	Minimum active overlap of poly	3
18.4	Minimum poly contact to active	2
18.5	Minimum active contact to poly	4/6

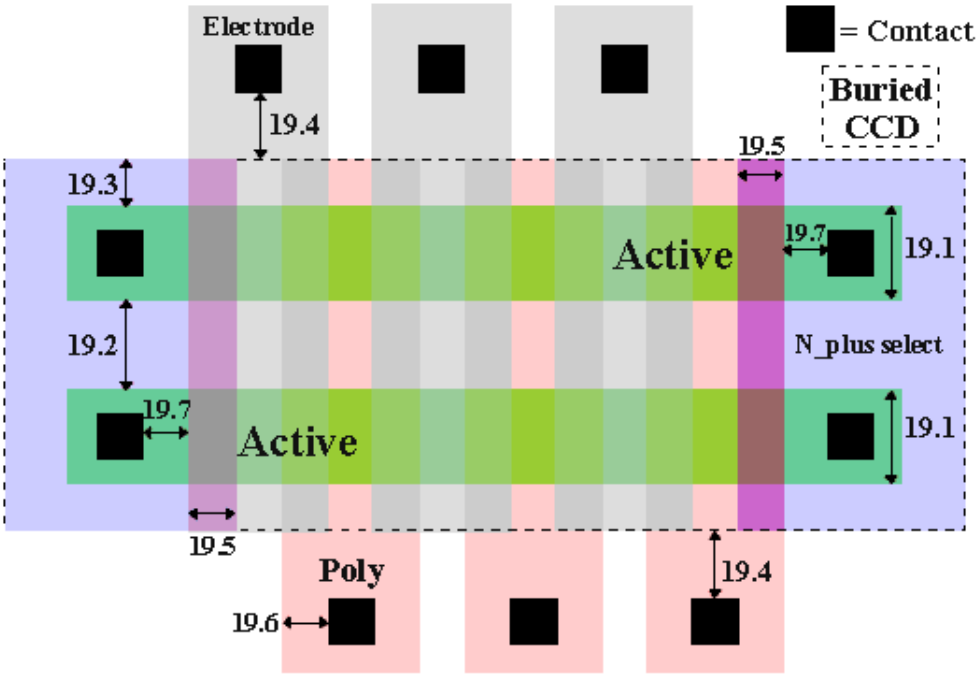
Table 25: SCMOS Layout Rules - Linear Capacitor (Linear Capacitor Option)



SCMOS Layout Rules - Buried Channel CCD (2um Analog Option)

Rule	Description	Lambda
19.1	Minimum CCD channel active width	4
19.2	Minimum CCD channel active spacing	4
19.3	Minimum CCD implant overlap of channel active	2
19.4	Minimum outside contact to CCD implant	3
19.5	Minimum select overlap of electrode (or poly)	2
19.6	Minimum poly/electrode overlap within channel active	2
19.7	Minimum contact to channel electrode (or poly)	2

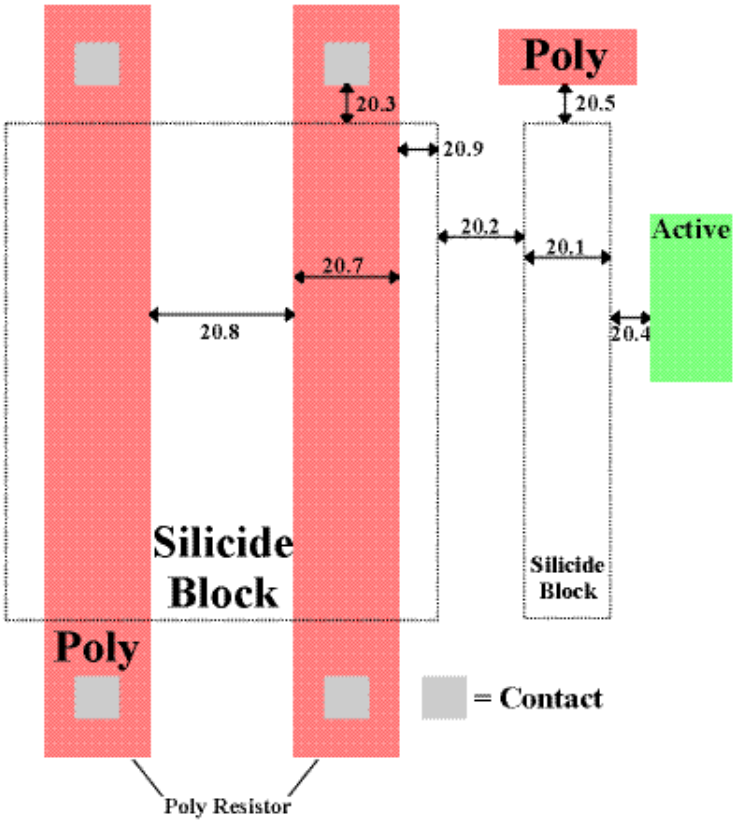
Table 26: SCMOS Layout Rules - Buried Channel CCD (2um Analog Option)



SCMOS Layout Rules - Silicide Block

Rule	Description	Lambda
20.1	Minimum SB width	4
20.2	Minimum SB spacing	4
20.3	Minimum spacing, SB to contact (no contacts allowed inside SB)	2
20.4	Minimum spacing, SB to external active	2
20.5	Minimum spacing, SB to external poly	2
20.6	Resistor is poly inside SB; poly ends stick out for contacts must be outside well and over field	
20.7	Minimum poly width in resistor	5
20.8	Minimum spacing of poly resistors (in a single SB region)	7
20.9	Minimum SB overlap of poly	2

Table 27: SCMOS Layout Rules - Silicide Block



SCMOS Layout Rules - Via3 (Quad Metal option)

A fourth metal layer will be available around the time of the 0.5 um feature size regime. In processes with four metal layers, the third metal is made thinner and therefore has the same layout rules as the second metal. Rules 15.1 and 15.3 are therefore revised in this option. These rules are designed for the SUBM variant directly.

Rule	Description	Lambda
15.1	Minimum Metal3 width	3 (not illustrated)
15.3	Minimum Metal3 overlap of VIA2	1 (not illustrated)
21.1	Exact size	2 x 2
21.2	Minimum spacing	4
21.3	Minimum overlap by Metal3	1

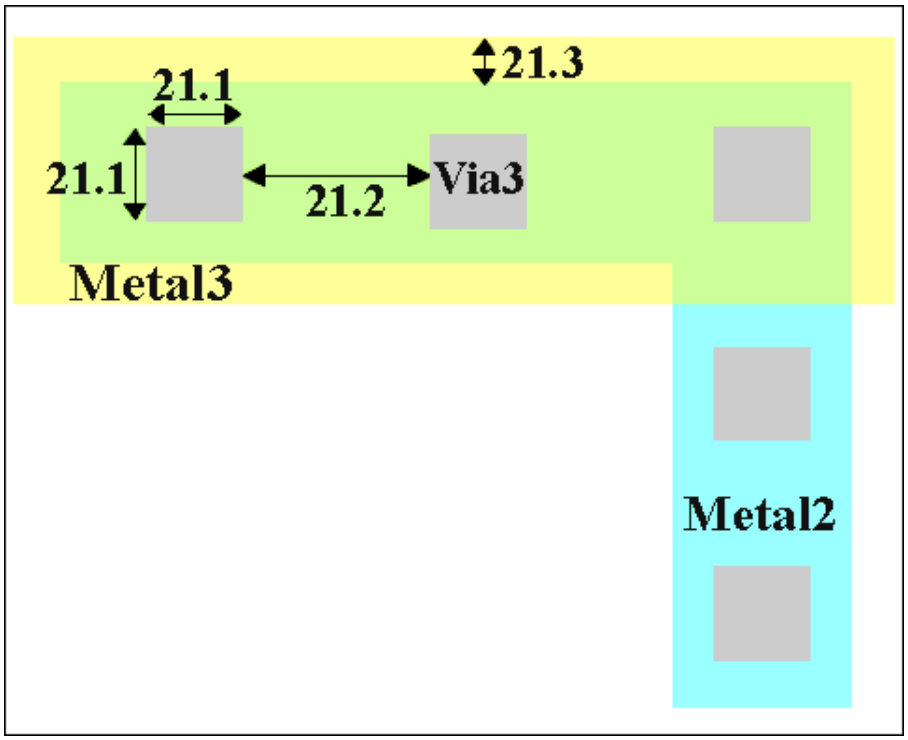


Table 28: SCMOS Layout Rules - Via3 (Quad Metal Option)

SCMOS Layout Rules - Metal4 (Quad Metal Option; SUBM only)

Rule	Description	Lambda
22.1	Minimum width	6
22.2	Minimum spacing to Metal4	6
22.3	Minimum overlap of Via3	2

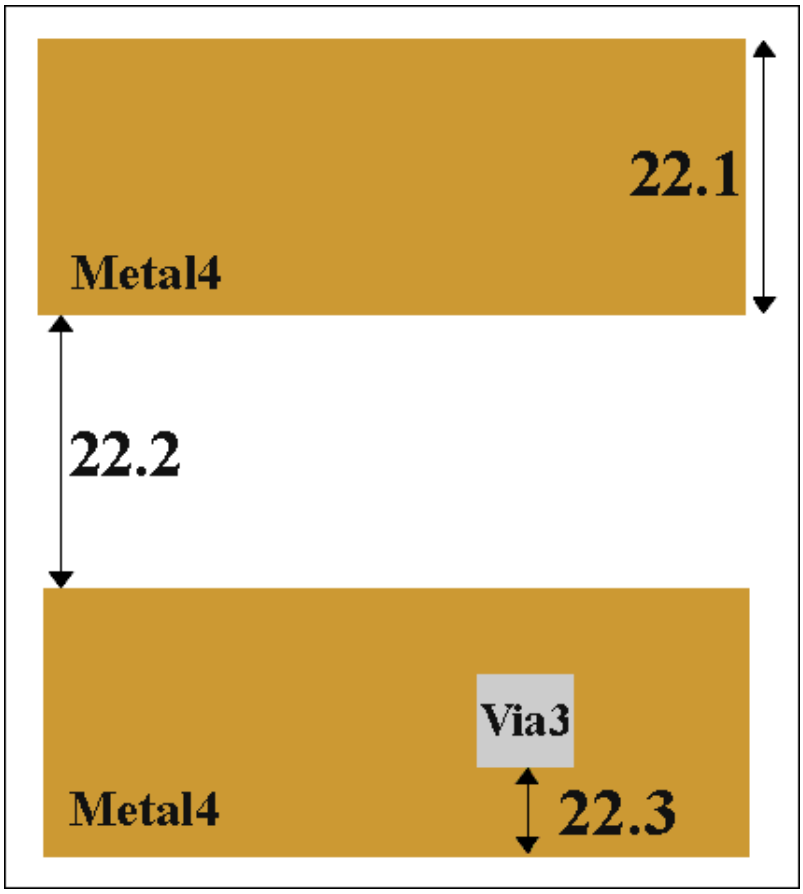


Table 29: SCMOS Layout Rules - Metal4 (Quad Metal option)

SCMOS Layout Rules - SCNPC with POLY_CAP1

The two plates of an SCNPC capacitor are POLY and POLY_CAP1. The POLY_CAP1 must surround the POLY everywhere; the area of the capacitor is the area of the POLY. POLY is physically on top of POLY_CAP1, so that contact to the POLY_CAP1 must be made in the region where it extends beyond the POLY. The capacitor may be in the well or the substrate, but may not straddle a well boundary. The only metal that may cross over a capacitor is the connecting METAL1 wires.

Rule	Description	Lambda
23.1	Minimum POLY_CAP1 width This is lithographic; the minimum to build a real capacitor is greater than 12 lambda	8
23.2	Minimum spacing, POLY_CAP1 to POLY_CAP1 (neighboring capacitor)	4
23.3	Minimum spacing, POLY_CAP1 to ACTIVE (all capacitors must be over field)	8
23.4	Minimum overlap, POLY_CAP1 over POLY	3
23.5	Minimum overlap, POLY_CAP1 over CONTACT	2
23.6	Minimum overlap, POLY over CONTACT (in a capacitor only; still 1 lambda elsewhere)	2
23.7	Minimum spacing, POLY to CONTACT-to-POLY_CAP1	2
23.8	Minimum spacing, unrelated METAL1 to POLY_CAP1	4
23.9	Minimum spacing, METAL2 to POLY_CAP1	2

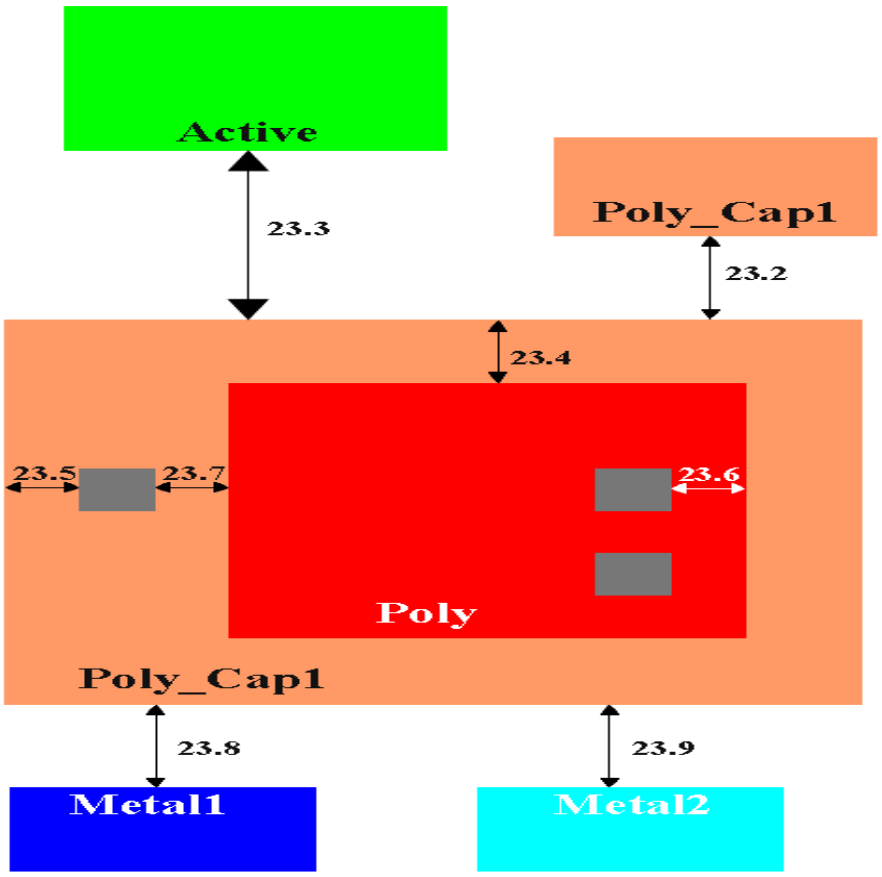


Table 30: SCMOS Layout Rules - SCNPC with POLY_CAP1