Elec 422: VLSI Design I – Project Milestones - Fall 1999

Date	Week	Milestone
Sept. 1 - 3	1	Group Formation
Sept. 7	2	Initial Project Idea
Sept. 7 - 10	2	Project Discussion during Office Hours
Sept. 14	3	One to Two Page Functional Description and Start of WWW page
Sept. 14 - 17	3	Project Discussion during Office Hours
Sept. 21	4	Initial Logic and Algorithm Flow Due
Sept. 21 - 24	4	Project Discussion during Office Hours
Sept. 28	5	PLA Finite State Machine, Control and Timing Description Due
Sept. 28 - Oct. 1	5	Project Discussion during Office Hours
Oct. 5	6	Initial Circuit Sub-Cell Layout Due
Oct. 5 - 8	6	Project Discussion during Office Hours
Oct. 12	7	Mid-Semester Project Status Report Due
Oct. 12 - 15	7	Mid-Semester Project Discussion during Office Hours
Oct. 26	9	Datapath Circuit Module Layout Due
Oct. 26 - 29	9	Project Discussion during Office Hours
Nov. 2	10	System Integration, Floorplan, I/O Pads Placement Due
Nov. 11	11	Mid-Term Exam, In-Class
Nov. 16	12	System Routing, System Simulation and Verification Plan Due
Nov. 16 - 19	12	Project Discussion during Office Hours
Nov. 30	14	Final Electrical Rules Checks and Preliminary CIF Due
Nov. 30 - Dec. 3	14	Final Design Evaluation of Layout during Office Hours
Dec. 7	15	Project Presentation to Class
Dec. 8	15	Final Layout CIF file, Project Report, and WWW Page Due
Dec. 20		Final Layout CIF file Due at MOSIS