Elec 422: VLSI Design I
Fall 2000

Notes on Final Layout and Submission to MOSIS.

Use of MOSIS AMI 1.5u Process

In order to prepare for chip fabrication, you will need to provide the following data:

1 Project Description

MOSIS requests a one paragraph description of your project. Please limit the description to approximately 50 words and e-mail it to cavallar@rice.edu. Please add this to your WWW project homepage. Also, please give your project a name which is less than 8 characters long, (for example, vending, for a vending machine project). MOSIS only tracks project names which are less than 8 characters.

2 Final CIF File

Please read Magic Tutorial 9: Format Conversion for CIF and Calma in the Elec 422 manual.

2.1 MOSIS pad frame

The 1.6 micron AMI pads are on Owlnet in /home/cavallar/demo/pads_16 and the main cell is 40p2200.mag It includes all of the pads cells. Please do not modify the I/O pads.

This set of pads should be used with a new technology file and new version of magic. It seems to support all designs done with the earlier technology file used this fall.

The new version will be called "magic_subm" and the correct technology file is SCNA.80 indicating the AMI process with a lambda of 0.8 microns. It will be installed on Owlnet in /usr/site/cad/bin. So invoke "magic_subm -T SCNA.80" when working on the final CIF file.

Make sure that you do a final *irsim* simulation of the chip after you have connected the pads to your design. Don't forget that there are special Vdd and GND pads to provide power to the internals of the chip. Once you have included the *40p2200* padframe in your design and completed the wire routing, you will need to create a final CIF file.

Note: Reading and writing CIF can take about 20 minutes at this stage. From within *magic_subm*,

```
:cif ostyle lambda=0.8(p)
:cif write project
:quit
```

Now create a new directory, copy the CIF file there, and read it back into *magic* to make sure that there are no final Design Rule Errors due to the creation of the well regions.

```
mkdir finalchip
cp project.cif finalchip
cd finalchip
magic_subm -T SCNA.80
:cif istyle lambda=0.8(p)
:cif read project
```

Check for Design Rule Errors, and correct if necessary.

```
:writeall
:quit
```

You will now have the final magic files with corrections. Start Magic_subm again and create a final CIF file if corrections were made.

```
:cif ostyle lambda=0.8(p)
:cif write submit
:quit
```

3 CIFflat file creation

The current version of *magic_subm* contains an alternative method to create a "flattened" CIF file which should lessen the problems with design rule errors due to nwell. I do not recommend the CIFflat file creation since you loose all design hierarchy. Start Magic again and create a flattened CIF file as follows:

```
:cif ostyle lambda=0.6(nwell)
:cif flat submit
:quit
```

There are, however, three limitations to this process:

1. LARGE amounts of memory are used. The Sun's may run out of memory. You may need to run on a lightly loaded machine or on one of the "compute" server machines, such as $great - gray$.
2. A very LARGE CIF file is created, usually 1 to 2 MB. This may cause problems with your disk quota.
3. All labels will be lost in the flattening process and you will be left with only one *magic* cell. You will need to relabel the pads and then run *irsim* to validate the final layout.

4 Final CIF Location

Please send e-mail indicating the location of the final CIF file, (publically readable) called "submit" in the above example. Please do not mail the file, since it will be quite large. Please make sure that the file and directory are publically readable.

5 Additional Materials

In order to facilitate the testing of the fabricated chips in Elec 423, please prepare a pin description in your report. Please label the signals on the padframe sheet which was handed out, and include this in your report. You may wish to redraw the diagram. Also indicate the purpose of each pin, (for example, "b0: First data input bit" and whether it is an input, output, or bidirectional. Indicate the controlling signal, if the pin is bidirectional.

Summarize this information in a file called "project.io" which should be formatted as follows:

```
i b0
i b1
i b2
i bipin0
i RESET
o result0
o result1
o bipin0
```

Each signal is on a new line, where the first character indicates whether the signal is an input or an output. (Note that if the pin is bi-directional, then it appears as both an input and an output.) Use the labels that are in your final .sim file.
Please e-mail this file to cavallar@rice.edu.

6 Final Irsim

A final *irsim* simulation should be performed from the pads. Paint some metal over the pad in the top level cell, and label appropriately. You make wish to call a signal "data1" internally and "pdata1" at the I/O pad.
Please create a directory for the final *isrim* simulation which contains the .sim file, the .cmd files, and Postscript files of the simulation results. Please e-mail the location of this publically readable directory to cavallar@rice.edu. Please choose a set of test vectors that will show the basic functionality of the chip.

7 Some Final Checks

When you have your final cif file and final read-back-in *magic* database, it is good to check the following details:

- Verify Vdd and GND connectivity. Use the "s" select key in magic to highlight "in white" all the connected Vdd lines. This will visually verify that your routing is complete. Make sure that the Vdd strap in the PLA is connected. Be careful about extractor warnings and warnings from ext2sim. Please track done, document, and eliminate those warnings. Do the same for GND, clka, clkb.

- Please verify that there are no Design Rule Errors.
- Please check all extractor and ext2sim warnings. Many times these do truly indicate sections of Vdd or GND or clka or clkb that are not connected. You may need to look in the *.sim* file to see if there are two separate nets for each of these signals.
- Be careful about substrate contacts of the wrong polarity. Again select the Vdd net. Then in *magic* do a :what command. This will show all layers and labels connected to Vdd. Among the layers, you should see "nsubstratecontact". If you see also "psubstratecontact" listed, then there is a major problem and a potential short. Use the same technique to verify that only "psubstratecontact" is connected to GND. The output of :what will be several screens worth of data. Make sure that your terminal window can capture it all.

8 Fabrication Status

Once the CIF file has been accepted by MOSIS and queued for fabrication, I will post the fabrication status reports outside my office. Good luck.