Elec 422: VLSI Design I

Homework 3

Fall 2000, October 19, 2000
Independent work is expected.
Due: October 26, 2000, in class.

Timing Analysis: Problems 1 and 2

The following problems 1 and 2 stress the area of timing analysis, based on the papers by Karplus. I have *coarsely sketched* the main units in the system. You may need to add Latches, and And/Nand gates in several places for the system to conform to the timing discipline. The Latches prevent problems due to feedback through the circuit, and the And/Nand gates are needed to qualify the latch control signals.

This assignment is intended to help with some of the high-level timing issues in your design project. In this assignment, you may ignore the actual functionality of the designs.

1. You should add timing labels on each of the "wires" interconnecting the circuit blocks with Valid, Stable, and Qualified clock signals.

2. Create a meg description of the PLA needed to control the adder circuit. Produce a *magic* file for the PLA and simulate the PLA with $irsim$. Simulate the following computation:

$$M_1 = A_1 + B_1 + C_1 + D_1 \tag{1}$$

   on both hardware systems. You will need to run the systems through enough states to complete the computation.

3. Show on the block timing diagram sktech which cycle the signals will operate on by using the cycle subscript notation introduced in class, (for example $V_{B_2}S_{A_3}$). You *do not* need to produce *magic* layout for the latches, adder, and transmission gates; that is, only *magic* layout for the PLA.

1 Accumulator Based System

This system uses a single adder and an accumulator register. The adder is busy on every clock cycle. It will take several cycles to complete the computation.

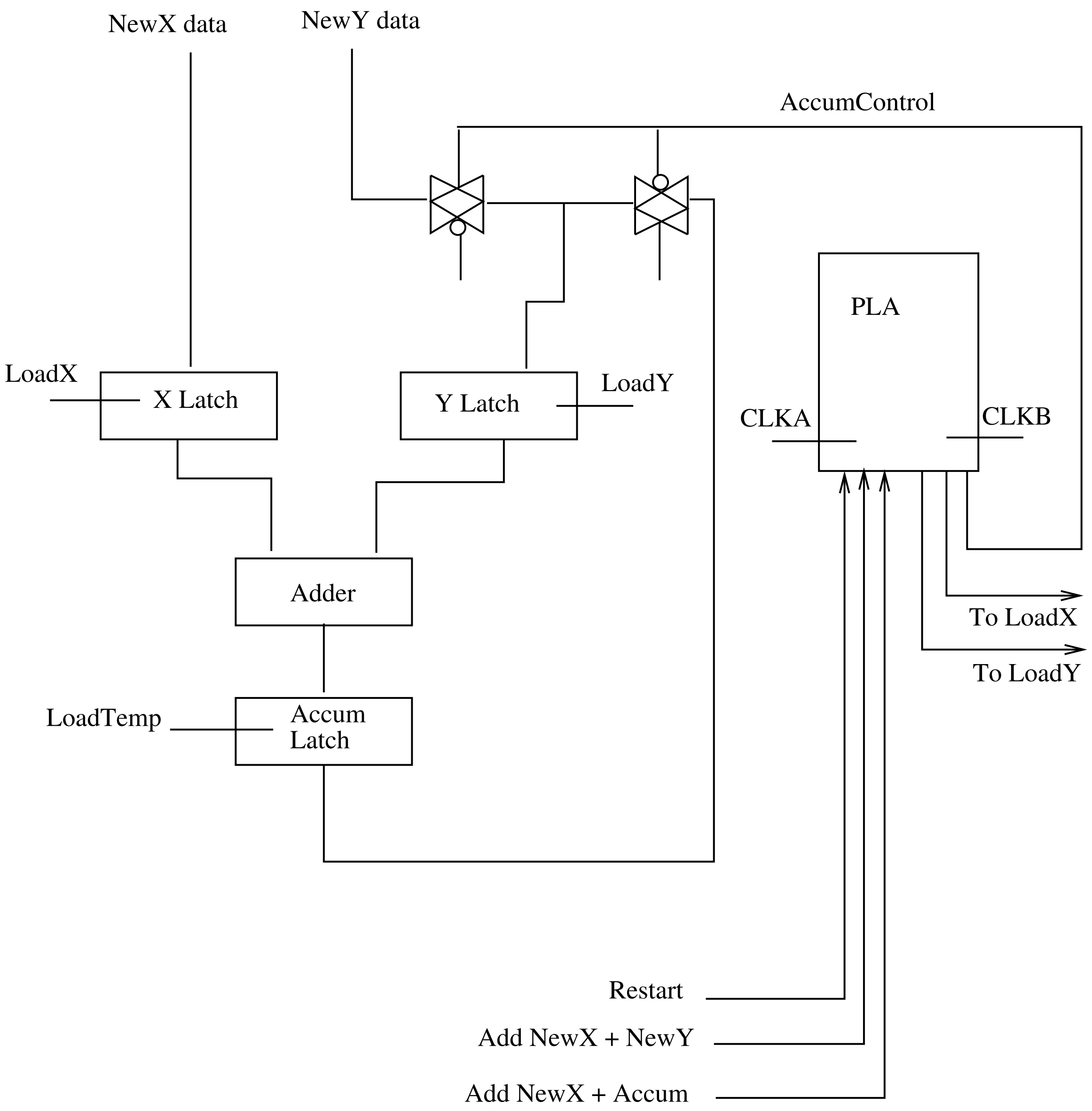

Figure 1: Accumulator Based System for Problem 1.

2 Multiple Cycle System (Pipelined)

This system uses several separate adders to complete the computation. Each adder will only be used once to compute M_1. You could begin the calculation of $M_2 = A_2 + B_2 + C_2 + D_2$ while the calculation of M_1 is still ongoing, since registers separate and isolate the computations. Please describe the timing so that the pipeline fills properly and then flushes properly when computation is done. That is, the pipeline should be active only to complete the set of computations desired. Please show this would work for three sets of results, $M_1, M_2, and M_3$.

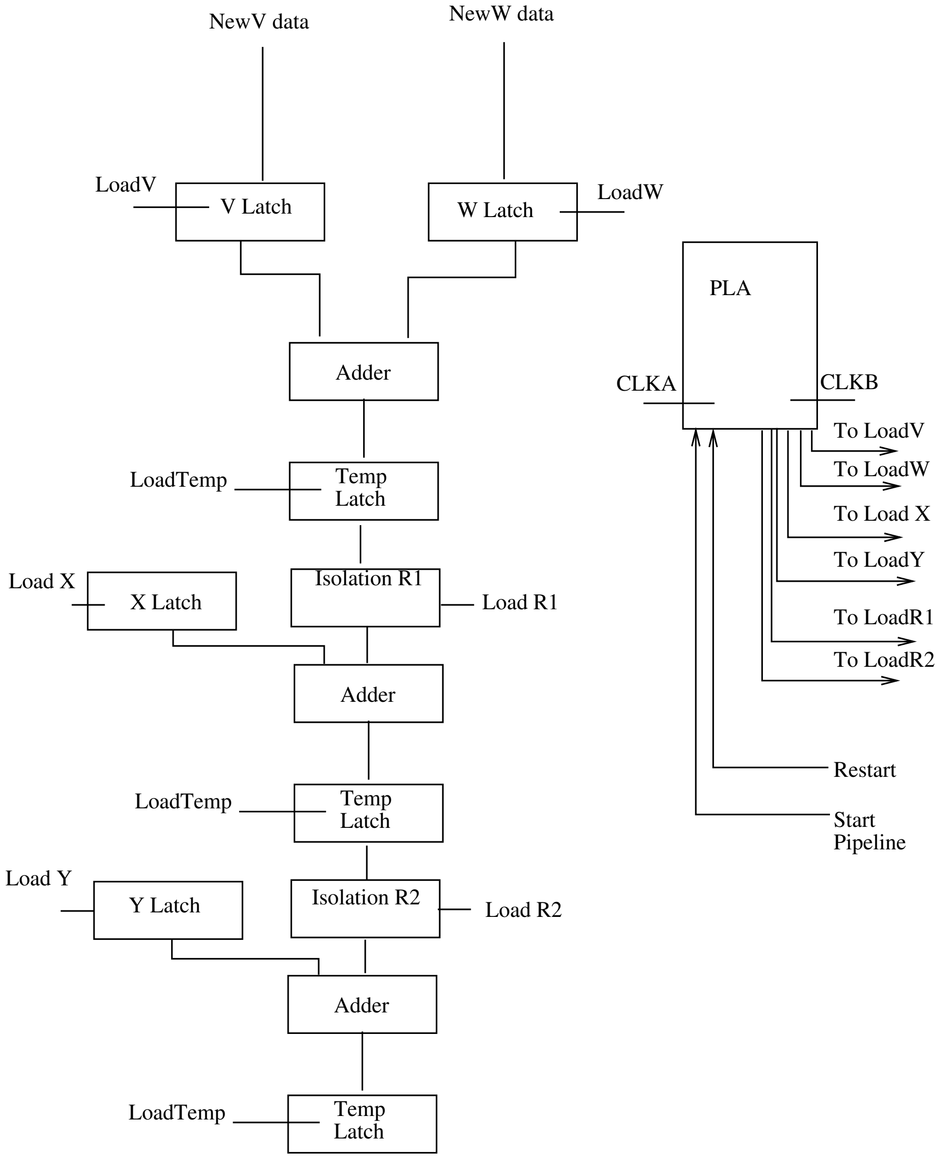

Figure 2: Pipeline Based System for Problem 2.

3 Timing with Crystal

Design the following circuit using $magic$. You may use cells which you have designed for previous homeworks. Use $crystal$ to determine the longest path for the following unclocked circuit.

Hint: Read the $crystal$ manual page and the tutorial at the end of the VLSI manual.

1. From the $crystal$ results, list the longest and second longest path through the circuit.

2. On a *cif2ps* or *pplot* plot of the complete circuit, trace (in color, if possible) the longest path through the circuit that $crystal$ discovers. Trace the second longest path on a copy of the *cif2ps* or *pplot* plot. This may or may not be related to or a subset of the first, longest path. You may need to add extra labels to your circuit to make sense of the intermediate nodes that $crystal$ traces through.

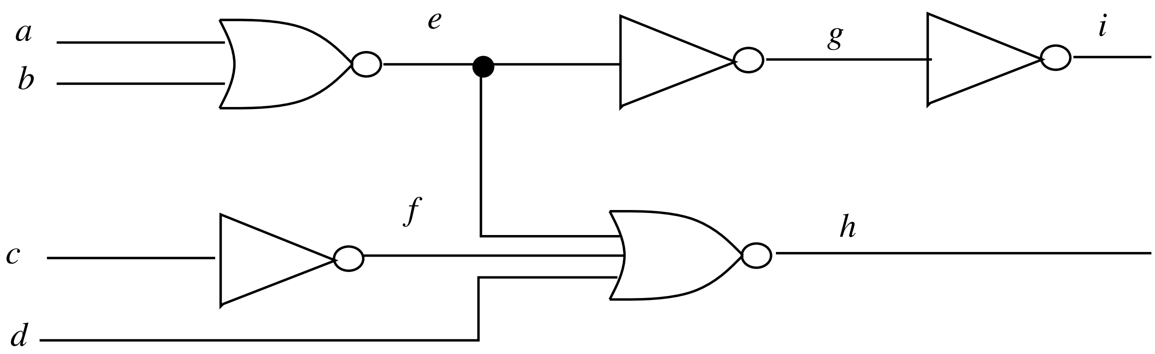

Figure 3: Circuit for $crystal$ analysis for Problem 3.