Elec 422: VLSI Design I

Homework 4

Fall 2000, October 26, 2000

Independent work is expected.

Due: Monday, November 6, 2000, at 5 pm.

Problem 1: Pseudo-NMOS Logic

Implement the following circuit in Pseudo-NMOS CMOS logic as shown. Draw a transistor level diagram of the circuit and use $magic$ and $irsim$ to layout and extensively simulate the circuit. Hint: You will need to modify the length and width ratio between the n-channel and p-channel devices in the NOR gates for proper operation. Experiment with (A) the standard static complementary CMOS ratio, and (B) a modified ratio as described in class.

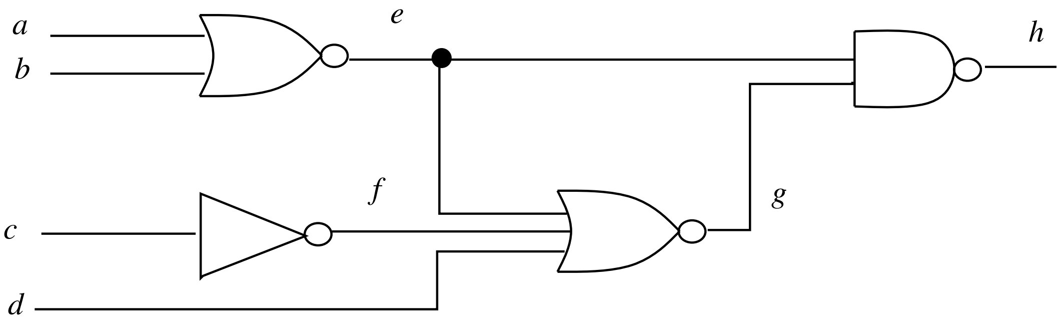

Figure 1: Circuit for Problem 1.

Problem 2: Domino CMOS Logic

Implement the following circuit in dynamic Domino CMOS logic as shown. Draw a transistor level diagram of the circuit and use $magic$ and $irsim$ to layout and extensively simulate the circuit. Hint: You will also need a precharge signal for this circuit. The gates used below are intentionally AND and OR structures due to the structural limitations of Domino CMOS in providing NAND and NOR blocks.

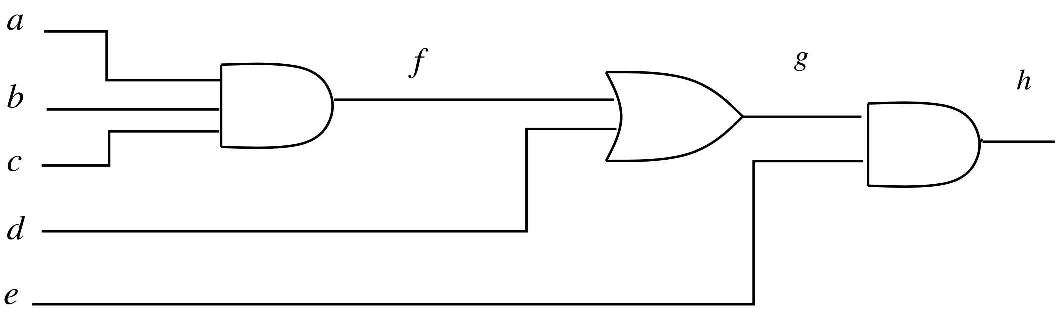

Figure 2: Circuit for Problem 2.