Elec 422: VLSI Design I
Homework 5

Fall 2000

November 7, 2000
Independent work is expected.
Problem 1 Due: November 14, 2000, in class.
Problem 2,3 Due: November 16, 2000, in class.

Problem 1: RC Timing Analysis

Perform an RC timing analysis of a 2-input NOR gate connected to an inverter. The inputs are a and b. The output of the NOR is $NORout$. The output of the inverter is $INVout$. Compute

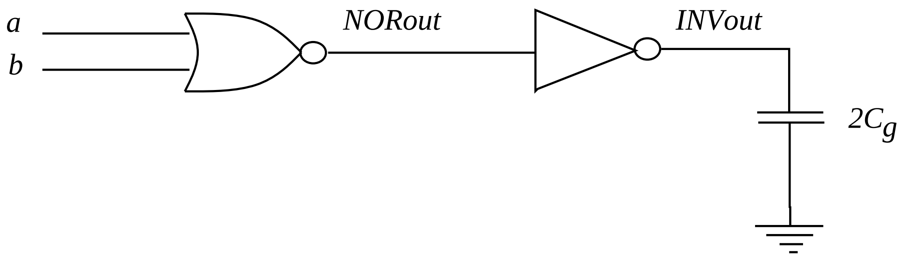

Figure 1: Circuit for Problem 1.

$R_{NORrise}$, $R_{NORfall}$, C_{NORout}, $R_{INVrise}$, $R_{INVfall}$, C_{INVout}. You may assume that the output load on the inverter is $2C_g$, and you may ignore wire lengths in this problem. Use the values below and determine the actual times in nanoseconds of $T_{NORfall}$ followed by $T_{INVrise}$, and also $T_{NORrise}$ followed by $T_{INVfall}$. For this problem, assume that the lengths and widths of the transistors are as follows:

n-channel $L = 2\lambda, W = 2\lambda$
p-channel $L = 2\lambda, W = 2\lambda$

Use the following approximate values for the parameters for approximate RC analysis:

nfet passing 0 = $14K\Omega = 1R/\Box$, nfet passing 1 = $56K\Omega = 4R/\Box$

pfet passing 0 = $112K\Omega = 8R/\Box$, pfet passing 1 = $28K\Omega = 2R/\Box$

$C_g = 12fF$

Standard size Contacts: 4×4 ndiff = $2.0C_g$, 4×4 pdiff $= 1.5C_g$, 4×4 poly = $0.25C_g$.

pdiff lumped with pchannel = $0.5C_g/\lambda$ of transistor width.

ndiff lumped with nchannel = $0.5C_g/\lambda$ of transistor width.

gate of nfet or pfet = $0.5C_g/\lambda$ of length where min width $= 2\lambda$.

Spice Analysis

For each of the following problems:

1. Use $magic$ to design the circuit, and $irsim$ to simulate the logic.
2. Please hand in a $cif2ps$ or $pplot$ plot of the circuit, and the results of the $irsim$ simulation.
3. Design an $HSPICE$ experiment file from the descriptions given below.
4. Use $ext2spice$ to build your $HSPICE$ input netlist file. Add the $HSPICE$ transisitor models to the netlist file. Finally, add your $HSPICE$ experiment to the end of the netlist files and save the file with a $.sp$ file extension. Please hand in the final $HSPICE$ $.sp$ input file.
5. Run $awaves$ and then invoke $HSPICE$ to generate output data for plotting the waveforms in the following experiments. Please hand in the $awaves$ plots.
6. There are some demo files in $/home/cavallar/demo/hspice/test2$ on Owlnet.

Problem 2: HSPICE Analysis of XOR

Run $HSPICE$ on a static complementary XOR circuit. The variable t refers to time in the de-

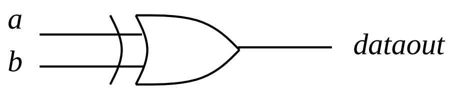

Figure 2: Circuit for Problem 2.

scription given below. Logic $0 = 0$ Volts and logic $1 = 5$ Volts. Mark nodes *a, b* as inputs and node *dataout* as output. Perform the following experiments with $spice$:

1. Node $dataout$ rises:
   At $t = 0,\ \ a = b = 0$
   At $t > 0,\ \ a = 0,\ \ b = 1,$

2. Node $dataout$ falls:
   At $t = 0,\ \ a = 1,\ \ b = 0$
   At $t > 0,\ \ a = b = 1.$

Problem 3: HSPICE Analysis of Pseudo-NMOS Logic

Run $HSPICE$ on the Pseudo-NMOS CMOS circuit shown below. The variable t refers to time

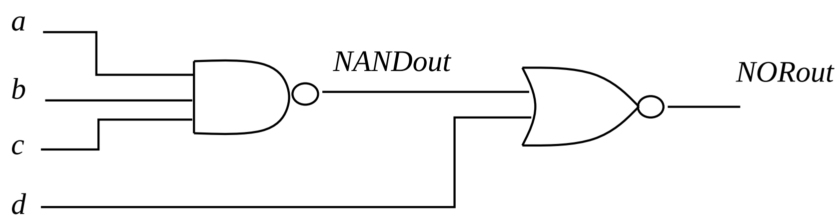

Figure 3: Circuit for Problem 3.

in the description given below. Logic $0 = 0$ Volts and logic $1 = 5$ Volts. Mark nodes *a, b, c, d* as inputs and node *out* as output. Perform the following experiments with $spice$:

1. Node $NANDout$ rises and node $NORout$ falls:
   At $t = 0, \;\; a = b = c = 1, \;\; d = 0$
   At $t > 0, \;\; a = d = 0, \;\; b = c = 1,$

2. Node $NANDout$ falls and node $NORout$ rises:
   At $t = 0, \;\; a = b = c = 0, \;\; d = 1$
   At $t > 0, \;\; a = b = c = 1, \;\; d = 0.$