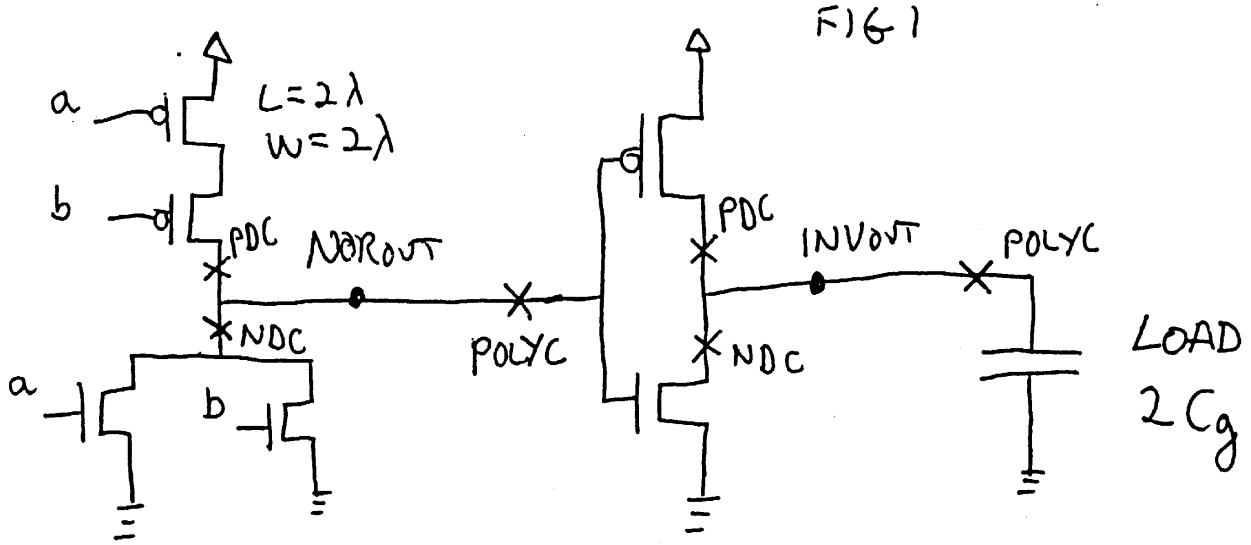
Elec 422: VLSI Design I
Homework 5 Problem 1 Solution

Problem 1: RC Timing Analysis

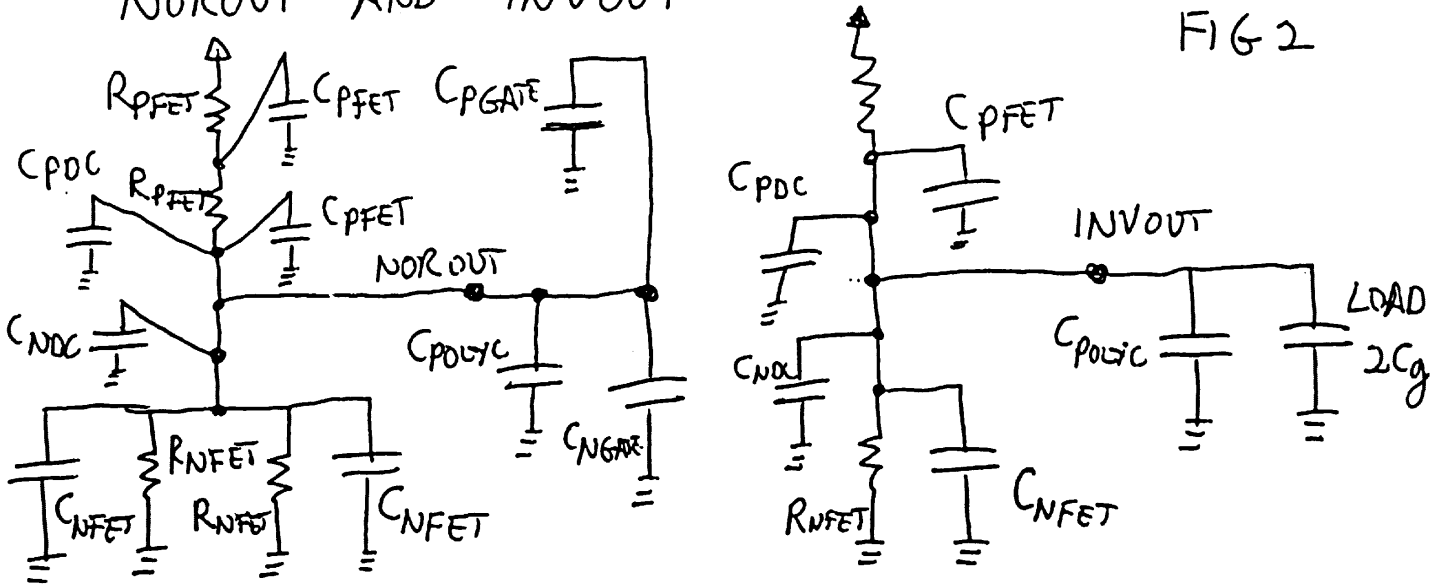
FIG 1



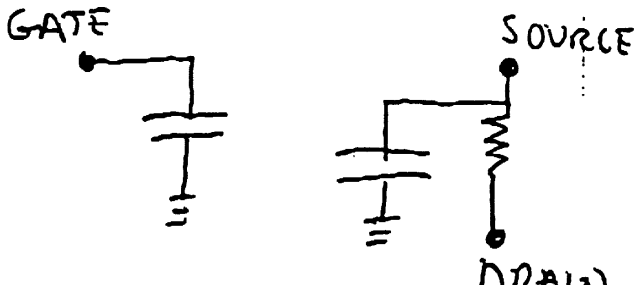
ASSUME ONE NDC, ONE PDC, ONE POLYC NEAR EACH OUTPUT NODE.

APPROXIMATE RC MODEL WITH PARALLEL CAPACITORS TO GROUND. SEPARATE MODEL FOR NOROUT AND INVOUT

FIG 2



ASSUME EACH TRANSISTOR HAS A LUMPED RESISTANCE AND CAPACITANCE TO GROUND.



SIMILAR TO "CRYSTAL" ANALYSIS OF EACH STAGE. APPROXIMATE CAPACITANCE RELATED TO "SIZE" OF TRANSISTOR.

C_{PGATE} OR C_{NGATE} OR C_{GATE} RELATED TO AREA OF GATE

WITH 1 C_g UNIT PER $4\lambda^2$ [BASED ON $2\lambda \times 2\lambda$ MIN GATE]

$$C_{GATE} = \frac{L \times W}{4\lambda^2} C_g = \frac{2\lambda \times 2\lambda}{4\lambda^2} C_g = 1\,C_g$$

$C_{GATE} \approx 12\,fF$ FOR 2 TO 3 μm CMOS "PROCESS"

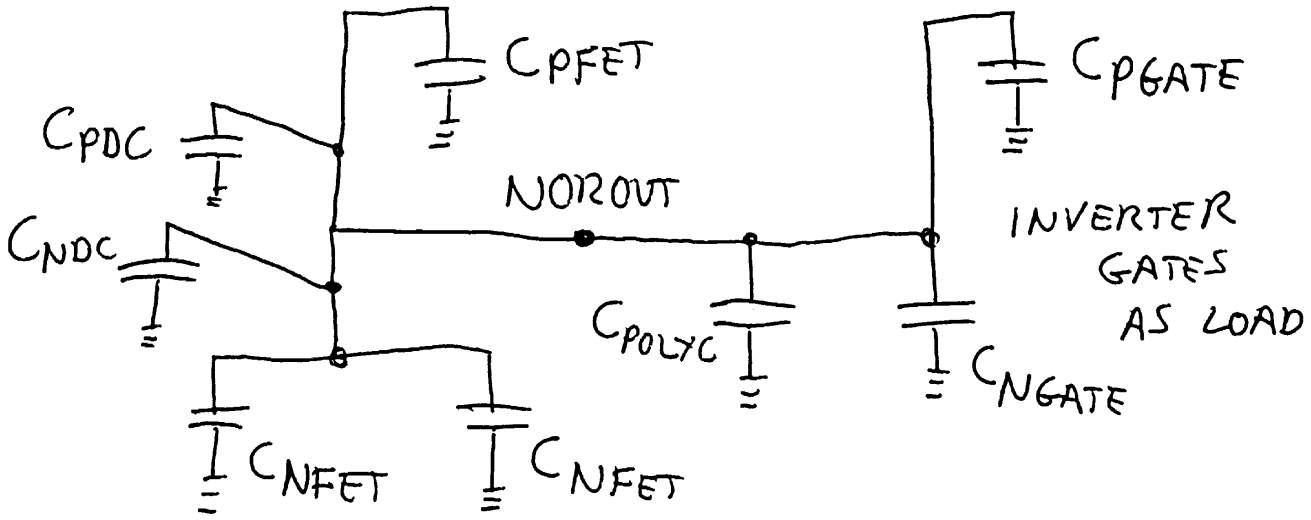
C_{SOURCE} OR C_{DRAIN} IS APPROXIMATELY RELATED TO WIDTH OF TRANSISTOR CHANNEL AND DIFFUSION

$$C_{PFET} \text{ OR } C_{NFET} \approx C_{SOURCE} = W \times \frac{0.5 C_g}{\lambda}$$

$$C_{PFET} \text{ OR } C_{NFET} = 2\lambda \times \frac{0.5 C_g}{\lambda} = 1\,C_g = 12\,fF$$

C_{NOROUT} IS RELATED TO CAPACITANCES DIRECTLY CONNECTED TO NOROUT NODE IN APPROXIMATE RC ANALYSIS IGNORE CAPACITANCE BEYOND TRANSISTORS.

FROM FIG 2.



$$C_{NOROUT} = C_{PULLUP} + C_{CONTACT} + C_{PULLDOWN} + C_{LOAD}$$

$$C_{PULLUP} = 1\,C_{PFET} = 1\,C_g$$

$$C_{CONTACT} = 1\,C_{PDC} + 1\,C_{NDC} + 1\,C_{POLYC}$$

WHERE EACH 4X4 MAGIC CONTACT HAS A 2X2 CUT REGION

$$C_{CONTACT} = 1.5 + 2.0 + 0.25 = 3.75 C_g$$

THESE NUMBERS ARE VERY CONSERVATIVE

$C_{PULLDOWN} = 2\,C_{NFET} = 2C_g$

C_{LOAD} = INVERTER GATES $= 1C_{NGATE} + 1C_{PGATE}$

$C_{LOAD.} = 2C_g$

$C_{NOROUT} = 1C_g + 3.75C_g + 2C_g + 2C_g$

$= 8.75\,C_g$

$C_{NOROUT} = 8.75\,C_g \times 12\frac{pF}{C_g} = 105\,fF$

$R_{NORRISE}$ = 2 PFET PULLUPS IN SERIES PASSING A "1" OR Vdd TO NOROUT.

$R_{NORRISE} = 2 \times \frac{L}{W} \times 2R = 2 \times \frac{2\lambda}{2\lambda} \times 2R$

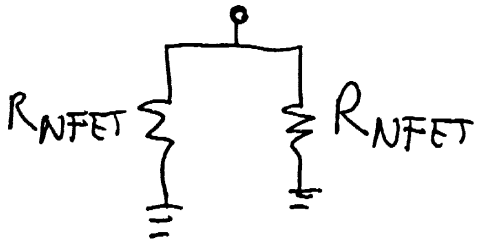
$= 4R \times 14\frac{K\Omega}{R} = 56K\Omega$

$T_{NORRISE} = R_{NORRISE} \times C_{NOROUT}$

$= 56K\Omega \times 105fF$

$T_{NORRISE} = 5.88$ ns NANOSECONDS

$R_{NORFALL}$ IS 2 NFET PULLDOWNS IN PARALLEL PASSING A "0" FROM GND TO NOROUT.



$$R_{NFET} = \frac{L}{W} \times R = \frac{2\lambda}{2\lambda} \times R = R$$

$$R_{NFET} = 14K\Omega$$

IF BOTH ARE CONDUCTING, THEN
$R_{NORFALL} = 7K\Omega$ FROM PARALLEL COMBINATION

WORST CASE WHEN ONLY ONE NFET IS ON. CONSIDER THIS WORST CASE, SO

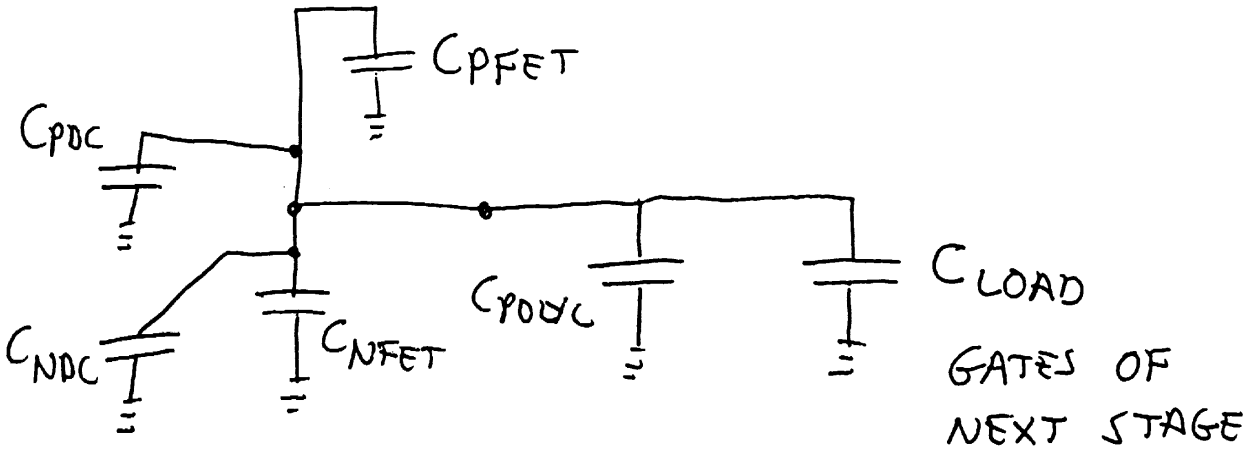
$$R_{NORFALL} = 1\,R_{NFET} = 14K\Omega$$

$$T_{NORFALL} = R_{NORFALL} \times C_{NOROUT}$$

$$= 14K\Omega \times 105fF$$

$$T_{NORFALL} = 1.470\ ns$$

INVOUT FROM FIG 2.



$$C_{INVOUT} = C_{PULLUP} + C_{CONTACT} + C_{PULLDOWN} + C_{LOAD}$$

$$C_{PULLUP} = 1\,C_{PFET} = 1\,C_g$$

$$C_{CONTACT} = 1\,C_{PDC} + 1\,C_{NDC} + 1\,C_{POLYC}$$
$$= 1.5 + 2.0 + 0.25 = 3.75\,C_g$$

$$C_{PULLDOWN} = 1\,C_{NFET} = 1\,C_g$$

$$C_{LOAD} = 2\,C_g$$

$$C_{INVOUT} = 1\,C_g + 3.75\,C_g + 1\,C_g + 2\,C_g$$
$$= 7.75\,C_g$$

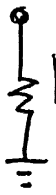
$$C_{INVOUT} = 7.75\,C_g \times 12\frac{fF}{C_g} = 93fF$$

$R_{INVRISE}$ = 1 PFET PULLUP

$R_{INVRISE} = 1 \times \frac{2\lambda}{2\lambda} \times 2R = 2R \times 14K\Omega = 28K.$

$T_{INVRISE} = R_{INVRISE} \times C_{INVOUT}$

$= 28K\Omega \times 93fF = 2.604\ ns$



$R_{INVFALL}$ = 1 NFET PULLDOWN

$R_{INVFALL} = 1 \times \frac{2\lambda}{2\lambda} \times R = 1R \times 14K\Omega = 14K\Omega$

$T_{INVFALL} = R_{INVFALL} \times C_{INVOUT}$

$= 14K\Omega \times 93fF = 1.302\ ns$

TOTAL TIMES THROUGH NOR + INV.

$T_{NORFALL} + T_{INVRISE} = 4.074\ ns$

$T_{NORRISE} + T_{INVFALL} = 7.182\ ns$