Elec 422: VLSI Design I – Project Milestones - Fall 2000

Date	Week	Milestone
Sept. 1	1	Group Formation
Sept. 5	2	Initial Project Idea
Sept. 5 - 8	2	Project Discussion during Office Hours
Sept. 12	3	One to Two Page Functional Description and Start of WWW page
Sept. 12 - 14	3	Project Discussion during Office Hours
Sept. 19	4	Initial Logic and Algorithm Flow Due
Sept. 19 - 22	4	Project Discussion during Office Hours
Sept. 26	5	PLA Finite State Machine, Control and Timing Description Due
Sept. 26 - Sept. 29	5	Project Discussion during Office Hours
Oct. 3	6	Initial Circuit Sub-Cell Layout Due
Oct. 3 - 6	6	Project Discussion during Office Hours
Oct. 10	7	Mid-Semester Project Status Report Due
Oct. 10 - 13	7	Mid-Semester Project Discussion during Office Hours
Oct. 24	9	Datapath Circuit Module Layout Due
Oct. 24 - 27	9	Project Discussion during Office Hours
Oct. 31	10	System Integration, Floorplan, I/O Pads Placement Due
Nov. 9	11	Mid-Term Exam, In-Class
Nov. 14	12	System Routing, System Simulation and Verification Plan Due
Nov. 14 - 17	12	Project Discussion during Office Hours
Nov. 28	14	Final Electrical Rules Checks and Preliminary CIF Due
Nov. 28 - Dec. 4	14	Final Design Evaluation of Layout during Office Hours
Dec. 5	15	Project Presentation to Class
Dec. 6	15	Final Layout CIF file, Project Report, and WWW Page Due
Dec. 18		Final Layout CIF file Due at MOSIS