Elec 422: VLSI Design I
Fall 2000
Final Report Format

Due: December 8, 2000

The £nal report is a group report and will represent about half of your grade. Please be thorough in your presentation. Your report should contain the following sections and will be weighted accordingly. It is very important that you indicate in the closing section, the ”division of work” by the group members. This statement must be agreed to by all members of the group so that I have an accurate assessment of each member's contribution. It is required that the ”statement of work” page be printed on paper, signed by each group member, and turned in to me. I am sorry for the need for formality.

Project Web Page

You should do your £nal report in electronic format through updates and additions to your Elec422 course project Web page. Please keep all html and graphics £les in one directory and make all Web links relative to the current page, so that the report can be easily moved to the www.ece.rice.edu server during summer 2001. The course project Web page should be reasonably complete and give a thorough overview of the design.

Report Subsections

1. Functional Description (10 points):
   Pin-map Showing Signal Name and Physical Pin Number:
   Functional Test Strategy and Output Test Signals:

2. Circuit Design (25 points):
   Logic Diagrams:
   System Timing Diagram:
   Irsim Results of Subcells:
   Irsim Results of Entire Chip:

3. PLA Description (10 points):
   Input to meg:
   Irsim Simulation:

4. Circuit Layout (30 points):
   Plots of low-level Cells (using $cif2ps$ or $pplot$):
   Cell Hierarchy:
   Floorplan:
   Full plot of Chip (using X window dump or xv or PC Xwin32 screen capture):

5. Performance Analysis; Maximum clock frequency (15 points):
   Crystal Analysis of longest path (5 points):
   Spice Analysis of critical sub-circuit (10 points):

6. Summary
   References
   Division of Work by Group Members
   Comments and Suggestions on CAD tools

7. Format and style (10 points):