Elec 422: VLSI Design I

Rice University

Spice Analysis of PseudoNmos and Static Complementary CMOS Circuits

Spice

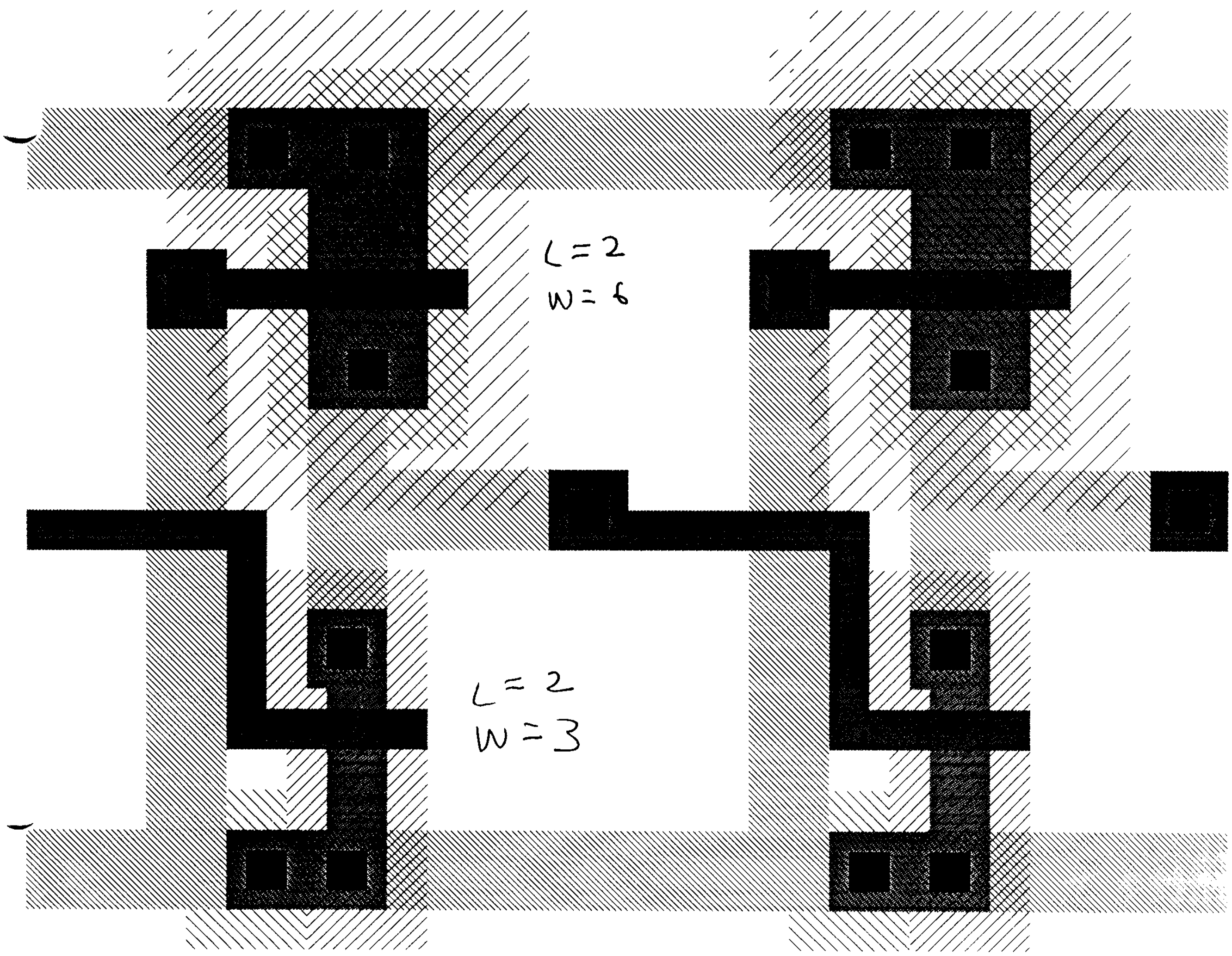
Examples of spice usage are located on Owlnet in /home/cavallar/demo, in the subdirectories cmos_buffer (for static complementary buffer) and pseudonmos_buffer (for pseudonmos buffer). Different ratios are presented for both experiments. The basic experiment file is:

```
*
* Elec422 SPICE EXPERIMENT TEMPLATE;
* ------------------------------------

* Set BASIC VOLTAGE levels
vdd <Vdd>  <GND>  dc 5
* set substrate voltages : P-sub = Vdd;  N-sub = GND
vs1 <CMOSP> <Vdd>  dc 0
vs2 <CMOSN> <GND>  dc 0

* ------------------------------------

* Set Circuit Input which will change, for example a:
* input pulse between node and GND (initially 0 ) of:
* pulse (init_value pulse_value delay rise_time fall_time pulse_width perio
vin <input> <GND> 0 pulse(0 5 0ns 0.1ns 0.1ns 9.8ns 20ns)

* ------------------------------------
* Do analysis: give increments and total time for analysis.
.tran .1ns 40ns
*
*
* If running in batch mode spice -b, then ascii plots are made
* Plot Voltages, for example a, sum, cout
.plot tran v(<input>) v(<output>) v(<outload>)

.end
```

PSEUDO-NMOS $\frac{1}{2}$ RATIO $\frac{\text{PULLUP}}{\text{PULLDOWN}}$

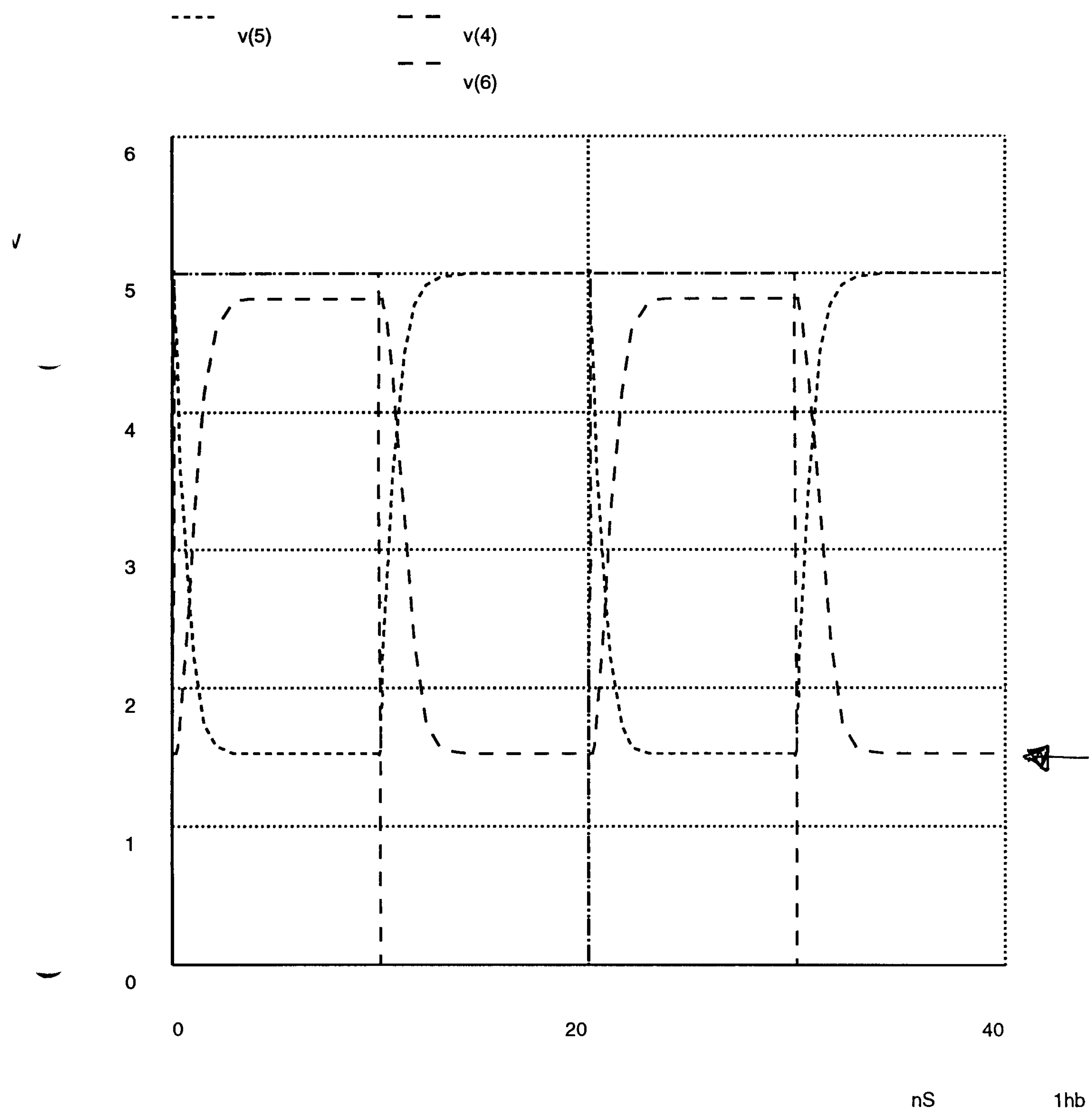
PULLUP = $\frac{2}{6}$

PULLDOWN = $\frac{2}{3}$

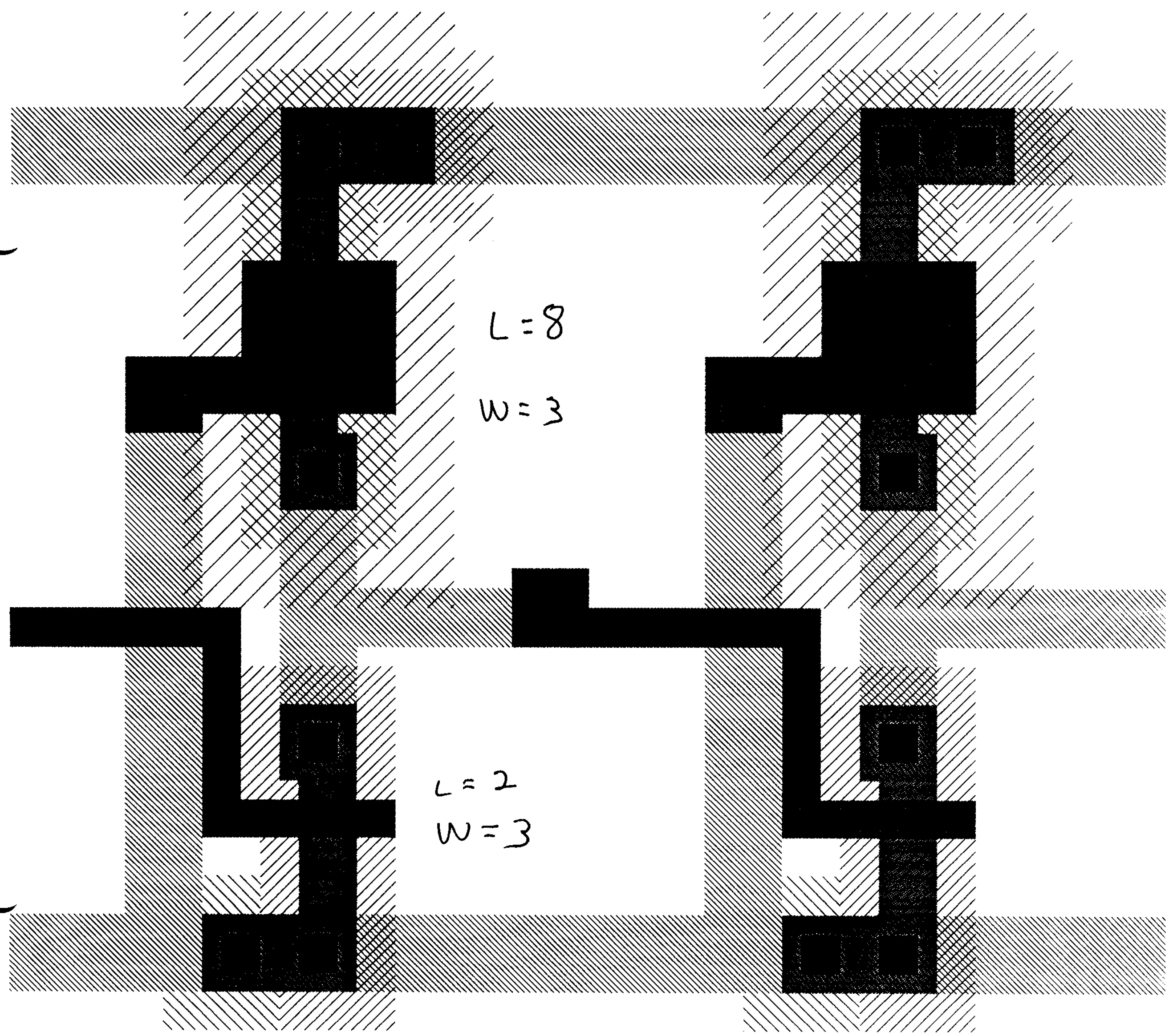


NOTE: LACK OF
FULL VOLTAGE SWING.

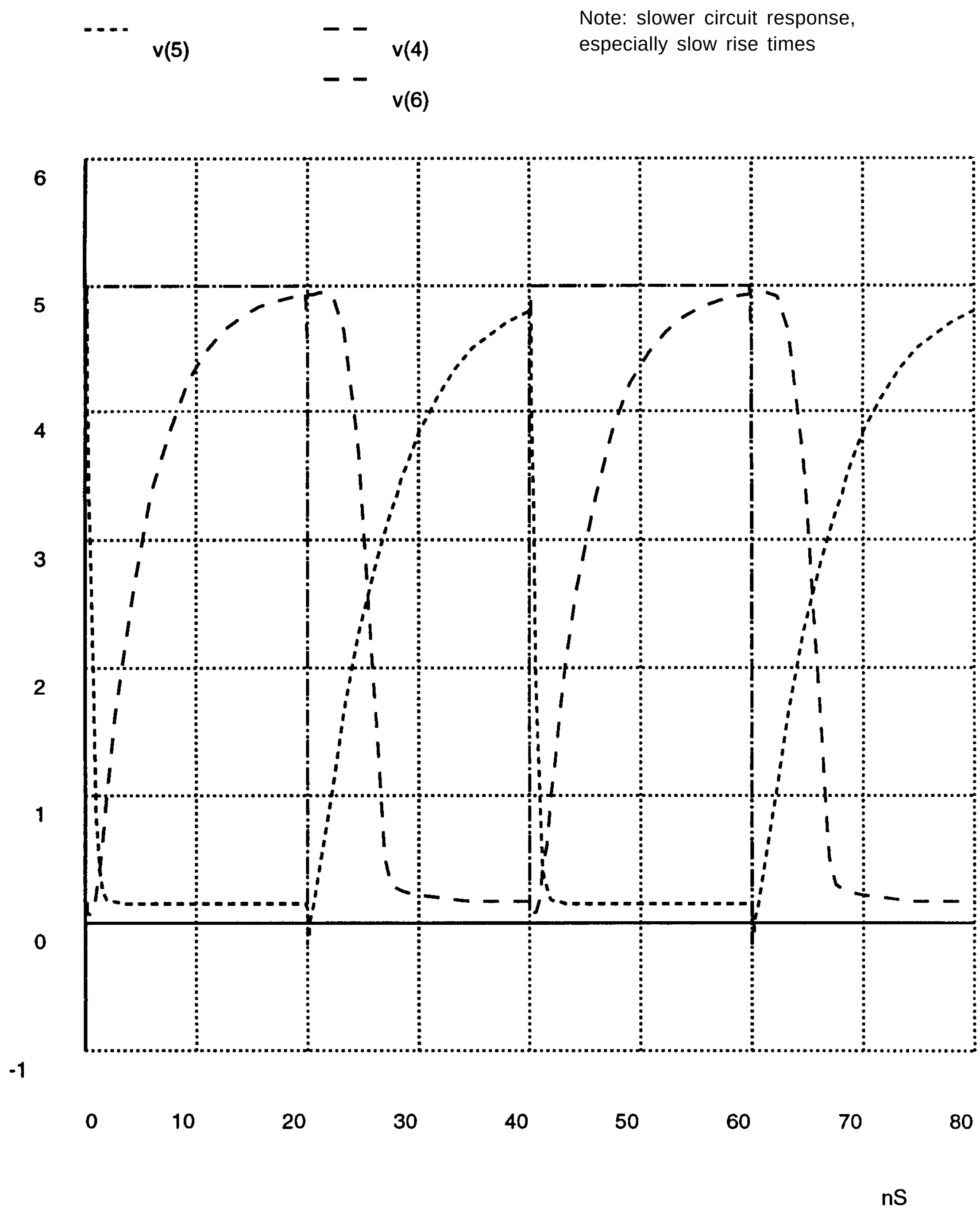
PN 1/2 RATIO



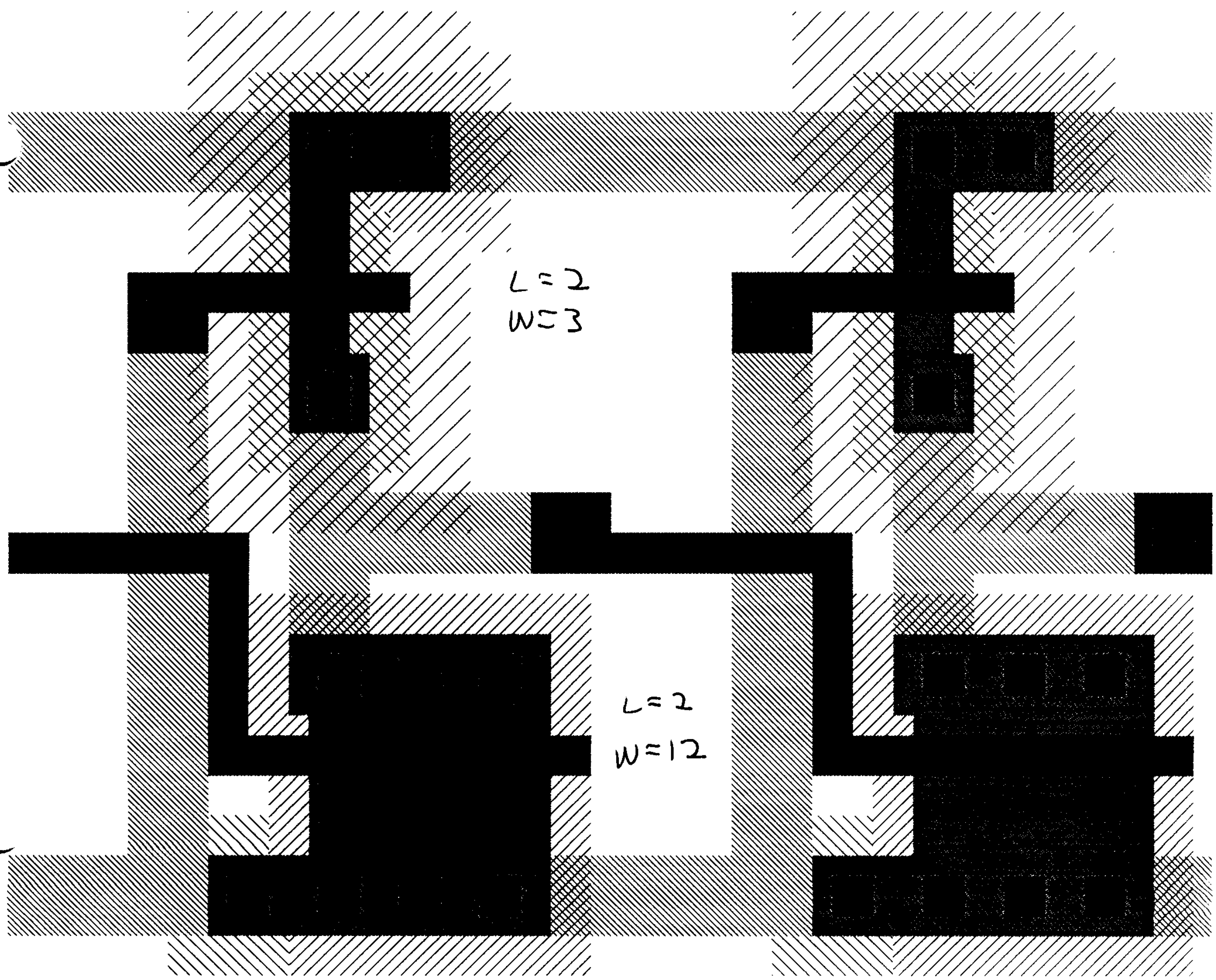
PSEUDO-NMOS $\frac{4}{1}$ RATIO

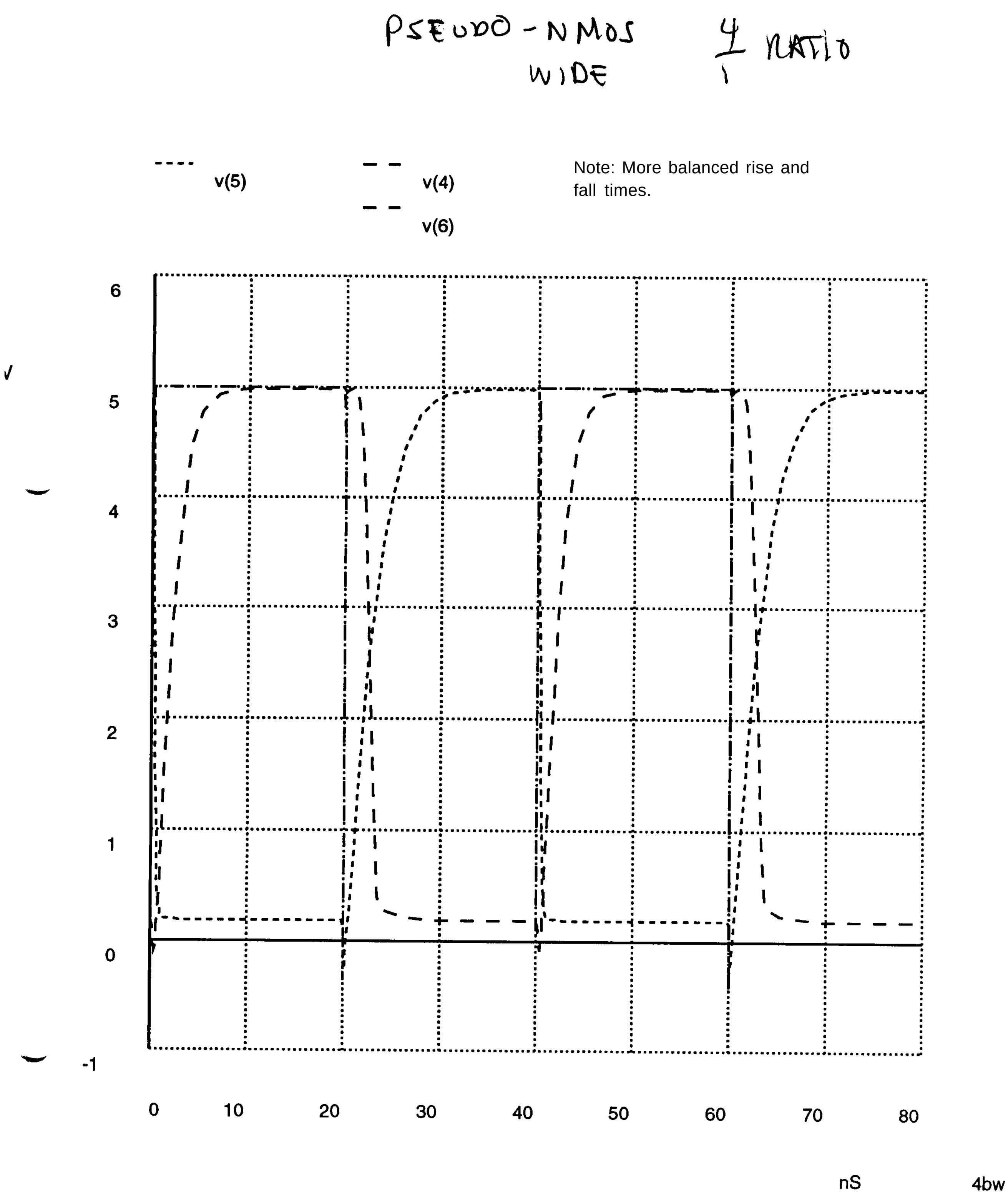


PN $\frac{4}{1}$ RATIO



PSEUDO-NMOS $\frac{1}{\frac{1}{4}} = \frac{4}{1}$ RATIO




PSEUDO-NMOS
WIDE
4/1 RATIO
v(5)
v(4)
v(6)
Note: More balanced rise and fall times.
V
6
5
4
3
2
1
0
-1
0
10
20
30
40
50
60
70
80
nS
4bw

DIGITAL CMOS CIRCUIT DESIGN

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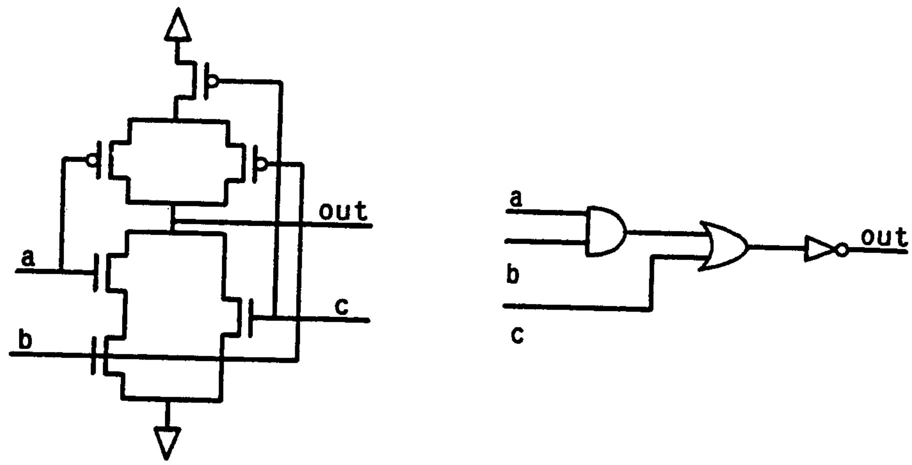


Figure 4-1: AOI implemented in complementary logic (left) and its representation in terms of basic gates.

4.1.2. nMOS-like Logic

The nMOS-like implementation of an AOI gate is shown in Fig. 4-2. Fig. 4-2(a) shows the n-channel based version, while Fig. 4-2(b) shows the p-channel based version. Each input is connected to the gate of only one device — instead of two as in complementary logic. Moreover, if the gate has n inputs, only $(n+1)$ devices are necessary. This logic occupies less area than complementary logic. Concerning circuit speed, nMOS-like logic was faster than complementary logic [12] in the early days of CMOS technology, when the gate capacitance of the MOS transistor was indeed a limiting factor. With fabrication processes of about 3μm and smaller, this is no longer true. Although the input capacitance is smaller than in complementary logic, because the input is connected to only one device, the pull-up section in Fig. 4-2(a) is a p-channel transistor used as a resistor, and the current which is delivered suffers from energy dissipation. We conclude that the two effects — decreased input capacitance but also decreased driving capability — balance each other.

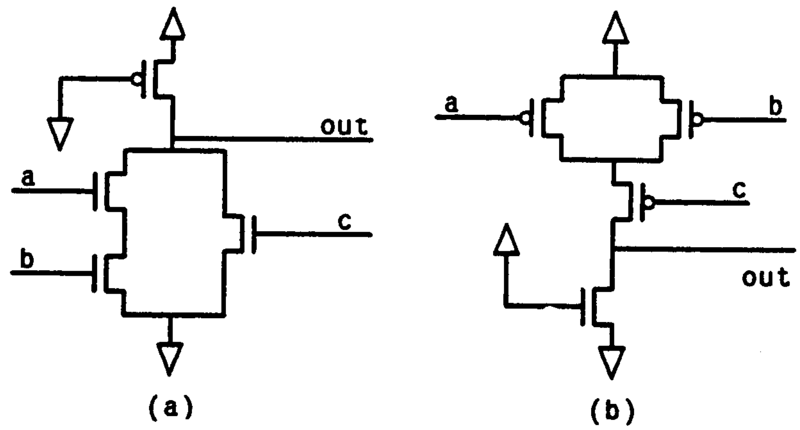


Figure 4-2: CMOS, nMOS-like AOI gates using n-channel devices (a) or p-channel devices (b).

nMOS-like logic is a *ratioed* logic. The pull-up and pull-down sections have to satisfy a certain range of ratios, otherwise the output voltage might not be able to switch the next gate(s) and/or the noise margin might be adversely affected, as shown in Figs. 4-4 and 4-5. Fig. 4-4 shows the input to an nMOS-like inverter (see Fig. 4-3 (left)) and six output curves. These curves refer to the same inverter with different pull-up|pull-down ratios. The two transistors have the same width, and the inverter drives a load of 10^{-3}pF. Curve 1 refers to the inverter with a pull-up|pull-down ratio of 1|1; curve 2 refers to the inverter with a pull-up|pull-down ratio of 2|1 (i.e., the p-channel device is twice as long as the n-channel device and both have the same width), and so on. Ratios of 1|1 and 2|1 are unacceptable. Besides providing poor noise margin, the output low level is close to 0.6V. When this output is connected to similar nMOS-like gates, it keeps the n-channel device(s) weakly off and drastically increases static power dissipation. In order to improve the noise margin and strongly turn off n-channel transistors in other gates, a ratio of either 4|1 or 5|1 is normally used. This is done at the expense of output rise-time, which increases when the ratio increases.

Figure 4-3: Inverter configurations for nMOS-like logic.

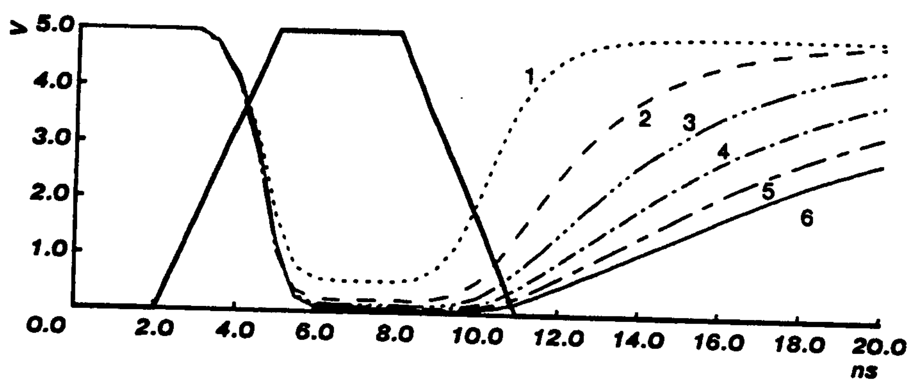


Figure 4-4: nMOS-like inverter of Fig. 4-3 (left): input signal (bold) and six output signals for different pull-up|pull-down ratios.

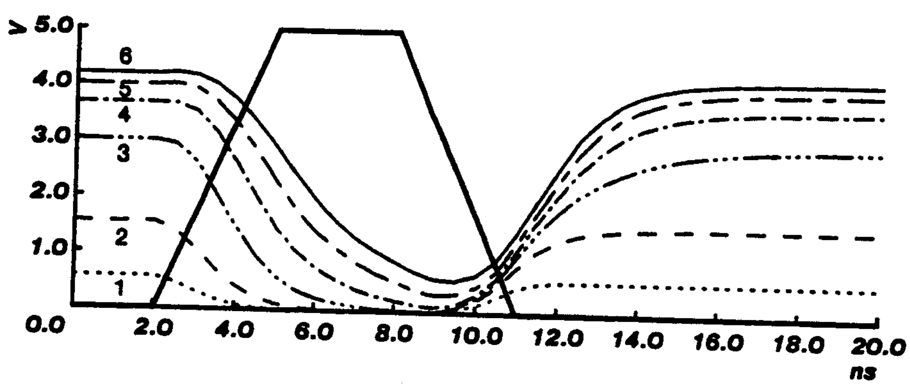


Figure 4-5: nMOS-like inverter of Fig. 4-3 (right): input signal (bold) and six output signals for different pull-up|pull-down ratios.

Fig. 4-5 shows the input signal to an inverter with a "complementary" configuration (see Fig. 4-3 (right)) and six output waveforms. The gate of the n-channel device is connected to V_{dd}, and the input signal is connected to the gate of the p-channel device. Both transistors have the same length. Curve 1 shows the output waveform for a pull-up|pull-down ratio of 1|1; curve 2 refers to a pull-up|pull-down ratio of 1|2 (i.e., the n-channel device is twice as wide as the p-channel transistor), and so on. Note that performance degradation is much more significant, and a ratio of 6 has to be considered the minimum requirement. Therefore, only a logic like the one shown in Fig. 4-2(a) is usually implemented.

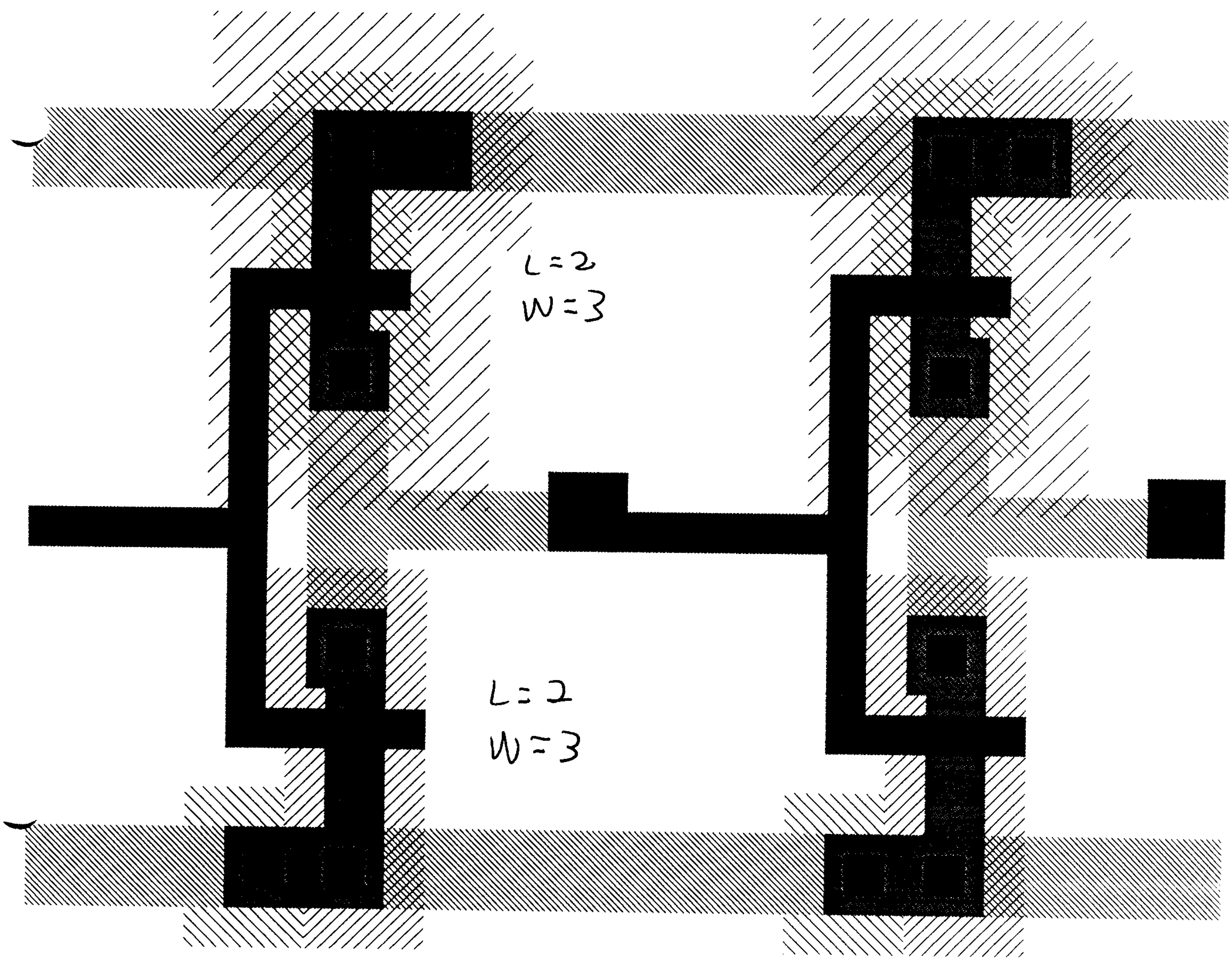
Finally, as in nMOS design, NOR-based gates are always preferred to NAND-based gates, because a NAND gate in this logic requires a long p-channel device to satisfy the necessary pull-up|pull-down ratio, making the layout more complex and slowing down the circuit. The most serious drawback of this logic is that a direct path between V_{dd} and V_{ss} exists when the input is high in the circuit in Fig. 4-3 (left). nMOS-like logic suffers from static power dissipation.

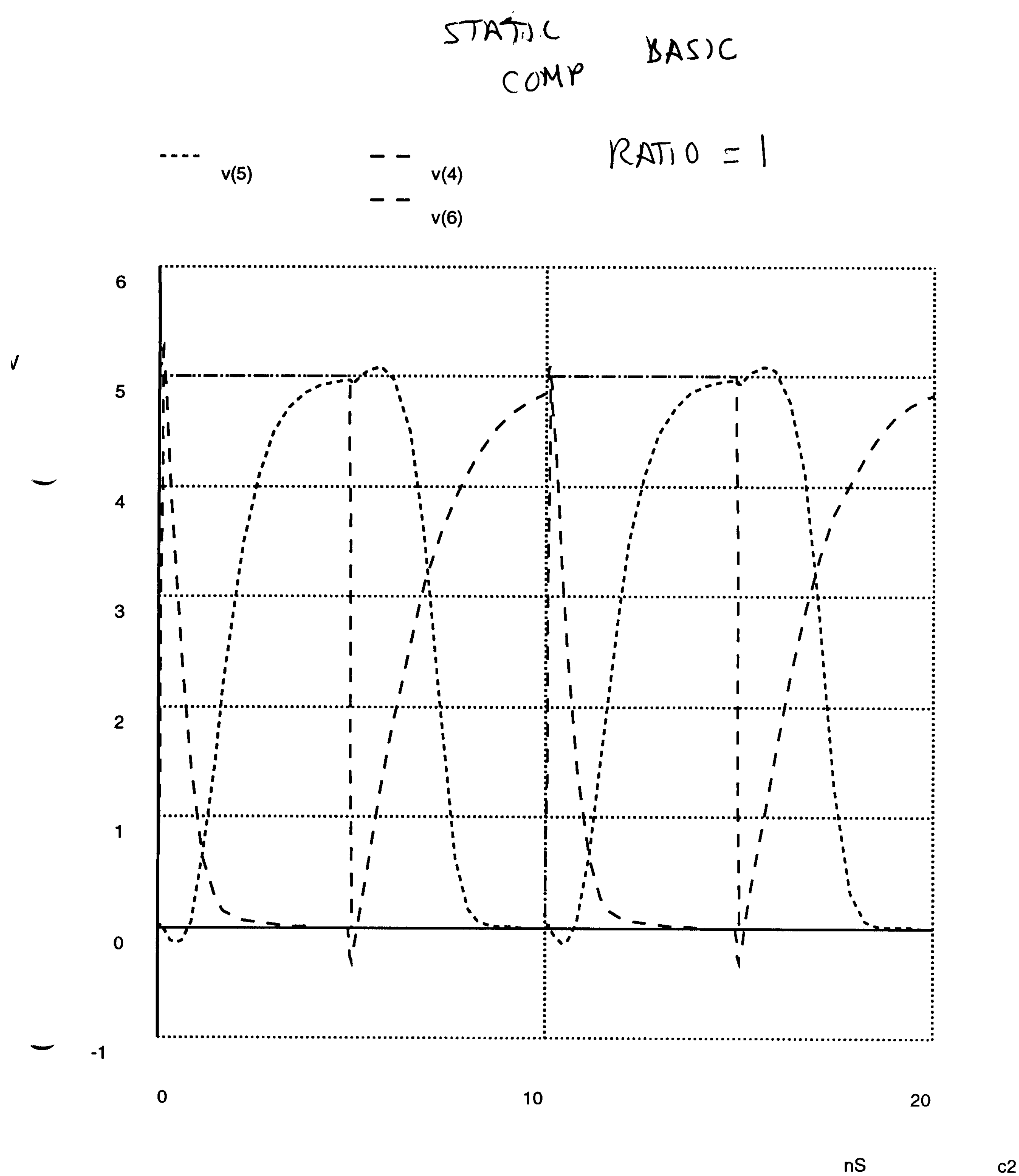
There are some applications where this logic can be useful, such as decoders with severe area limitations and no clock availability. As a general guideline, this logic can be implemented when power dissipation is not a major concern, circuit density is of fundamental importance, and no clock is available — either because there is no clock or because it cannot be used. Finally, note that the difference in power dissipation between nMOS-like and complementary logic *decreases* with higher frequency of utilization of the complementary gates, because dynamic power dissipation is proportional to the frequency of operation of the circuit, as shown in Eq. (2-23).

STATIC COMP.

BASIC

$$RATIO = \frac{\frac{2}{3}}{\frac{2}{3}} = 1$$



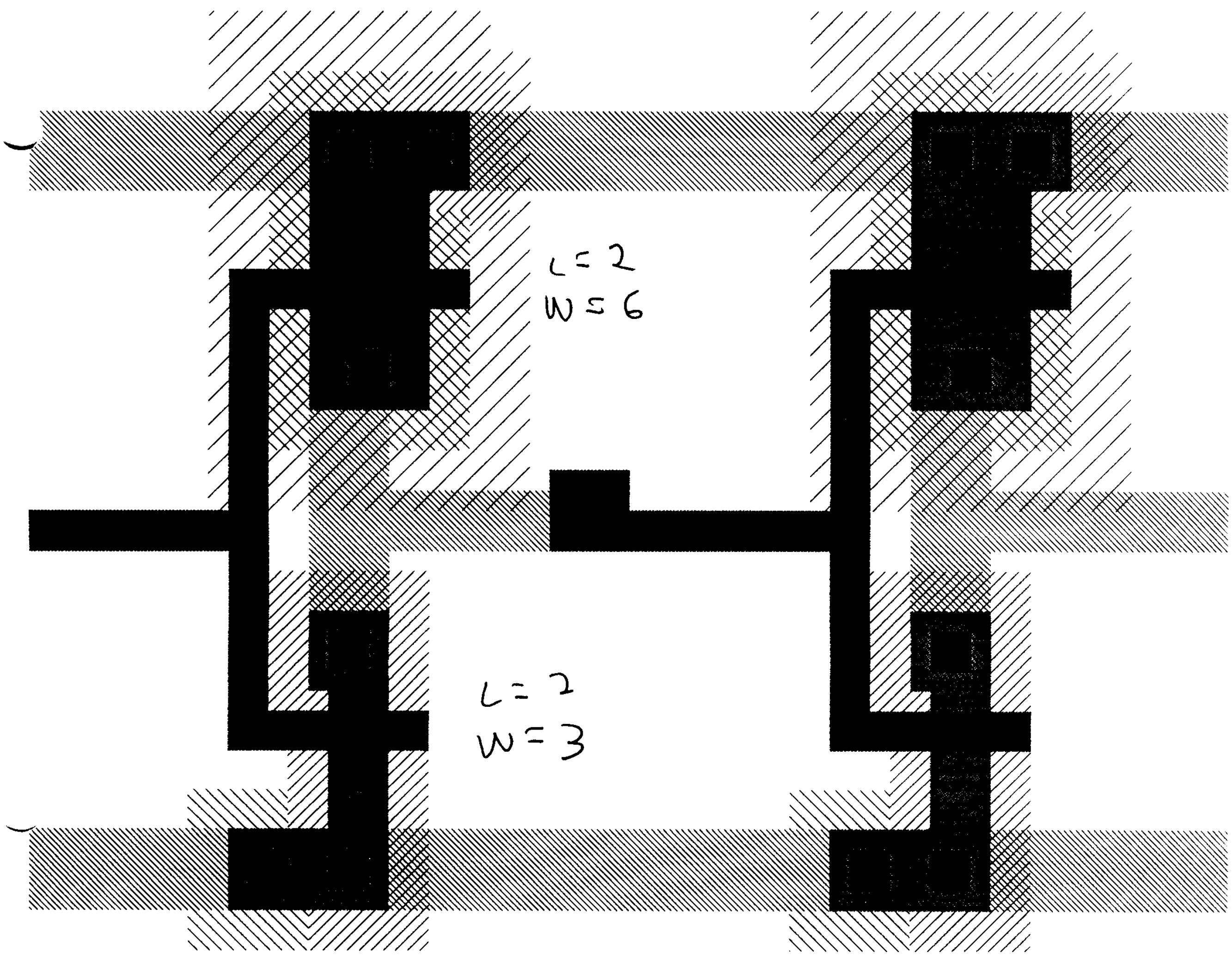

STATIC COMP
BASIC
RATIO = 1
v(5)
v(4)
v(6)
6
5
4
3
2
1
0
-1
V
0
10
20
nS
c2

STATIC COMP

WIDE PULLUP

$$\text{RATIO} = \frac{\frac{2}{6}}{\frac{2}{3}} = \frac{1}{2}$$

Note: Preferred Inverter ratio for more equal rise and fall times



Static Complementary CMOS with Wider Pullup P channel transistor to reduce pullup resistance and achieve more balanced rise and fall times.

Note: Faster Rise Time with Ratio = 1/2