# Rice University
# Elec 422, VLSI Design I
# Course Information, Fall 2000

## 1 Organization

Day & Time: TTh 2:30-3:50pm
Location: Duncan Hall 1064
Web Page: http://www.ece.rice.edu/Courses/422
Instructor: Joe Cavallaro, DH 3042, x4719, cavallar@rice.edu
Lab Assistants: Sridhar Rajagopal, sridhar@rice.edu, DH3039

## 2 Topics

Logic Design and Simulation.
CMOS Processing.
"Stick" Diagrams.
Hierarchical Layout Methodology.
State Machine Design and Programmable Logic Arrays.
Design for Testability; Fault Tolerance.
Computer-Aided Design Tools: *irsim, magic, spice...*
MOSIS Scalable CMOS Design; $1.5\mu$ nwell process.

## 3 Required Textbooks

1. Weste & Eshraghian "Principles of CMOS VLSI Design" Second Edition, Addison-Wesley, 1993.

## 4 Course Requirements

- **Students are required to enroll in Elec 423 VLSI Design II during Spring 2001. This is due to contractual obligations with the MOSIS Fabrication Service to provide a report on the success of the fabricated chip.**
- Group Project (Groups of three) to be fabricated by MOSIS.
- Five Homeworks during first half of semester. (25%) (Independent work under the Honor System is expected).
- Midterm Exam (In-class, Honor System, closed book, mid-November) (25%).
- Project Presentation & Design Review (Last week of class) (10%).
- Final Group Project Report (Due Wednesday Dec. 6) (40%).