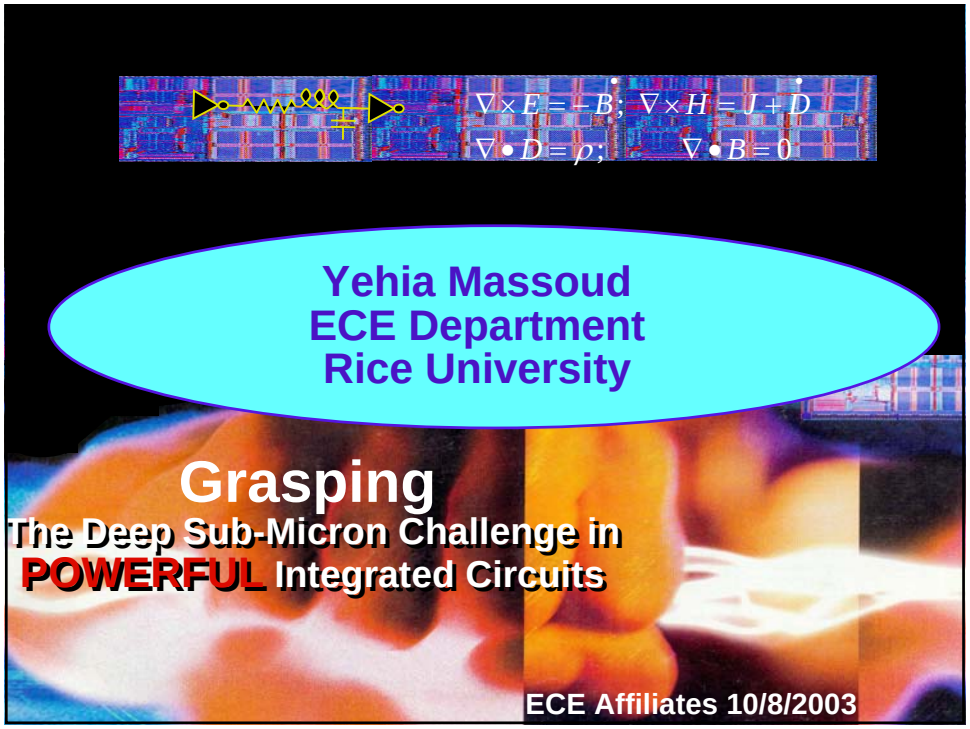
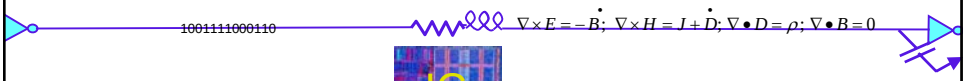
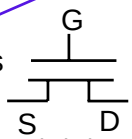


Background: Integrated Circuits





Transistors

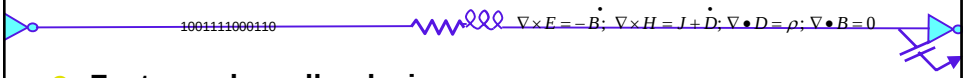
Wires (Interconnects)

- Transistor is a switch (0 or 1)
- Wires transmit logic between transistors

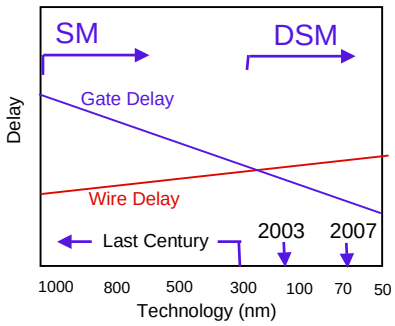
For faster chips

- Shorter gate length (t=L/v)
- Shorter gate length (0.25 Micron)
- Shorter gate length (< 100nm)
- Faster wires (less R) Use Copper

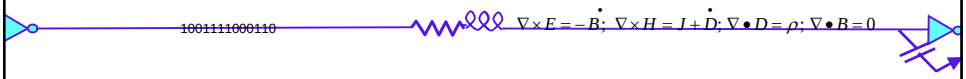
Technology scaling



- Faster and smaller devices
- Wire delay has already exceeded Gate delay

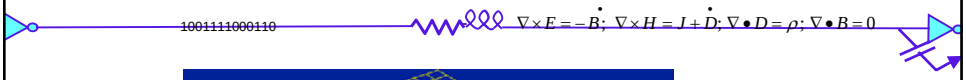


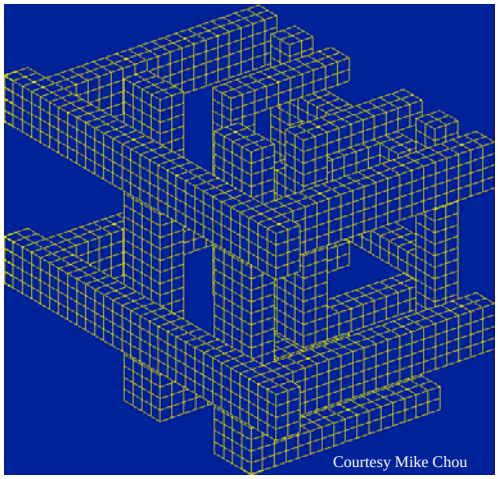
Interconnect Modeling



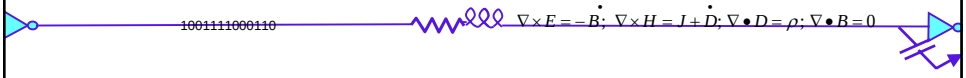
- Model interconnects as short-circuit (Gate delay was dominant)
- Interconnect resistance became comparable to gate resistance
  - Use of Copper, R is smaller
  - Faster clock speeds and faster transition times
- Inductive impedance became comparable to interconnect resistance $\omega L \geq R$
- Need Accurate and fast modeling of RC and L

3D Interconnect world

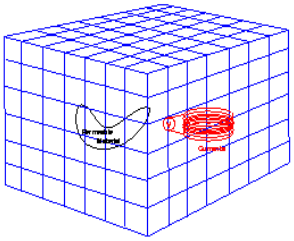




3D Interconnect Extraction (Field Solvers)

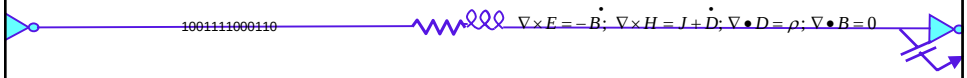


- **Finite Element Method (FEM)**
  - **Mature subject (many codes available)**
  - **Solve for the field contained in a finite volume**
  - **Volume must be big enough to assume no fields outside**
  - **Produces many unknowns**
  - **Very Slow**

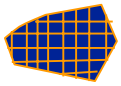


- **Cannot be run across chip**

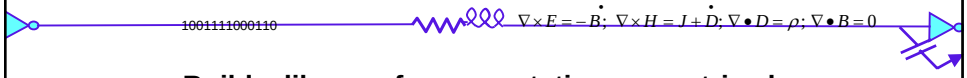
3D Interconnect Extractors (Field Solvers)



- **Boundary Element Method**
  - **Solve for the charges on the boundaries**
  - **Fewer # of unknowns than FEM but produces dense system**
  - **Need fast methods to solve dense system**
    - **Direct Gaussian Elimination, O(n^3), way too slow**
    - **Iterative methods, O(n^2), still too slow.**
    - **Multipole Accelerated iterative method O(n)**
    - **FFT O(n log(n))**
  - **Faster than FEM but still too slow to be run for the whole chip**



3D Interconnect Extraction (Pattern Matching)



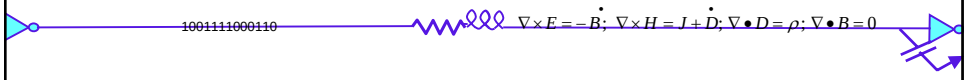
- **Build a library of representative geometric shapes**
- **Use field solvers to extract these shapes**

- **Generate library**
  Parameterized equations
  Train a Neural Net ?

- **Extraction**
  - **Decompose the layout into a set of these shapes**
  - **Evaluate interconnect values**

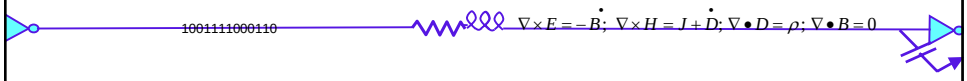
- **library generation takes long time**
- **May loose accuracy when breaking into shapes**

Optimal Interconnect Extraction



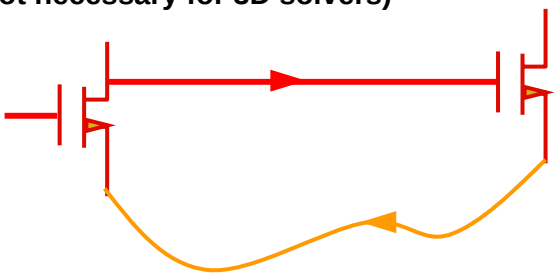
- But how would you extract thousands of interconnects?
- What you Want to do
  - Use " Super fast" 2D globally
  - Use 3D libraries/ local 3D Solvers
    - 2D model breakdown
    - Detailed analysis
    - Critical, Clock, Power nets
- Super fast extractors
  - Use 2D extraction (has been done of R and C)
  - 2D inductance extraction (Problematic ?)

What is inductance?

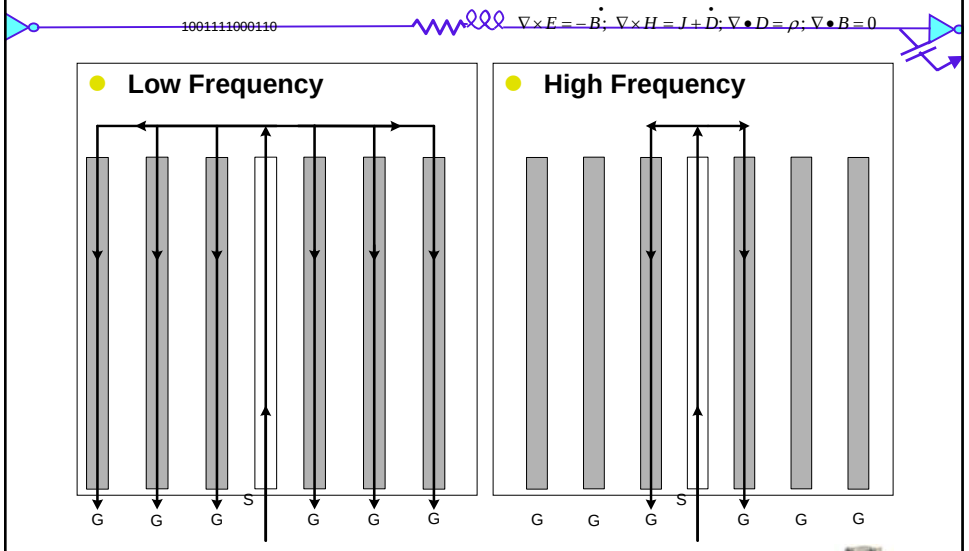


- Inductance is a loop quantity

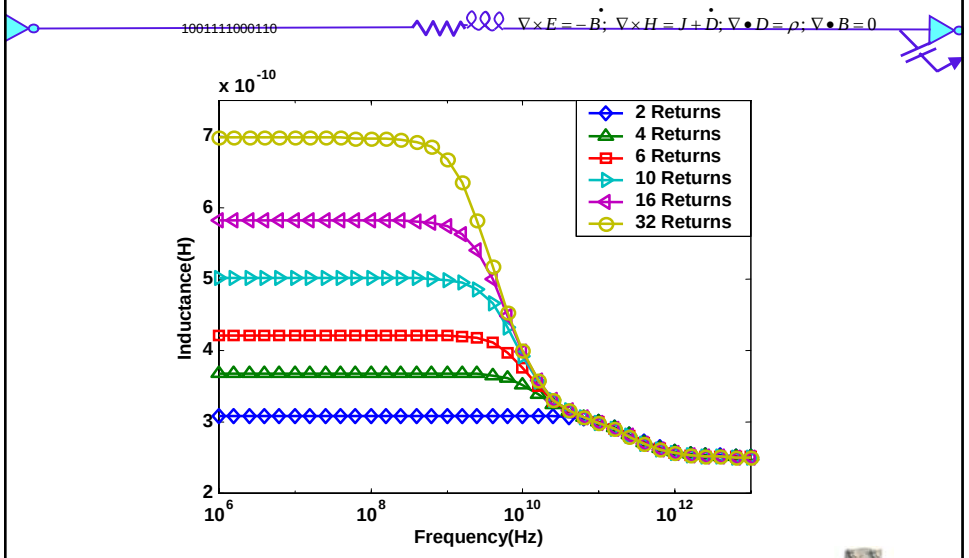
  (Flux Linkage to a loop)
- Knowledge of return path is required
  - (not necessary for 3D solvers)



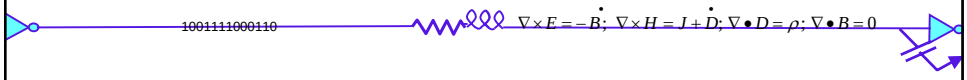
Current Return Path
Frequency Dependence

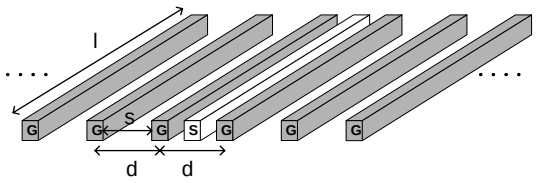


Inductance vs Frequency

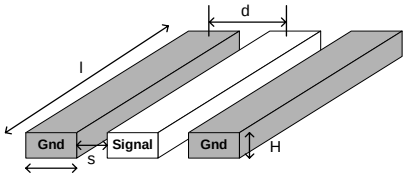


Current 2D Inductance extraction



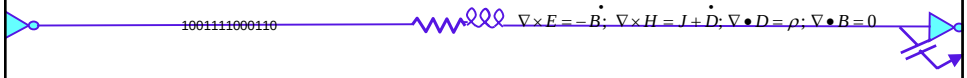


d=2(w+s)

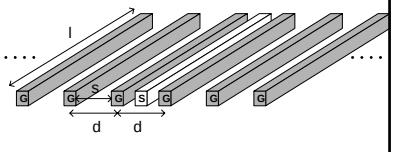


Return is the nearest line

Formula-Based Inductance Extraction



$$L_{loop} = \frac{\mu l}{2\pi}\left[a_0 \log\left(\frac{d}{w+H}\right) - a_1\frac{d}{l} + a_2\right]$$



d=2(w+s)

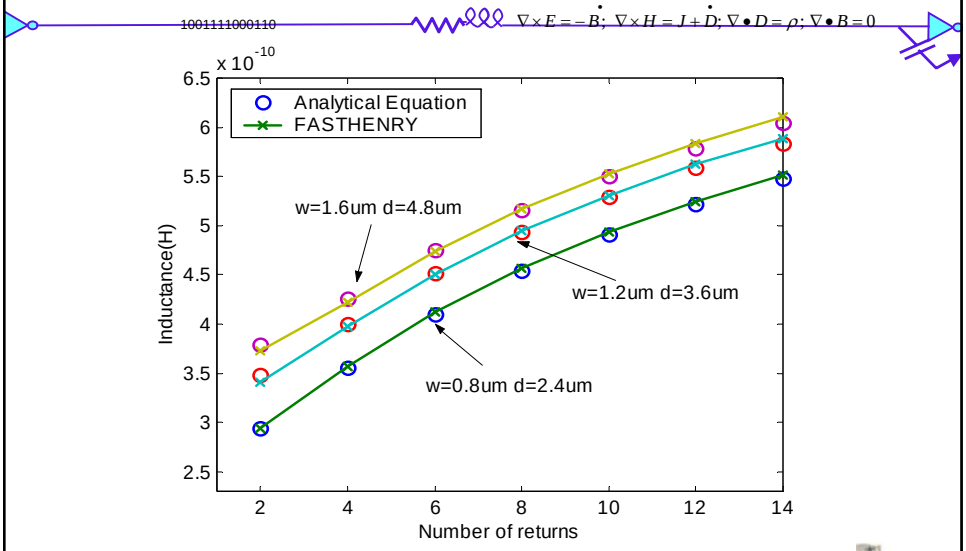
$$a_0 = 1 + \frac{1}{2N}$$

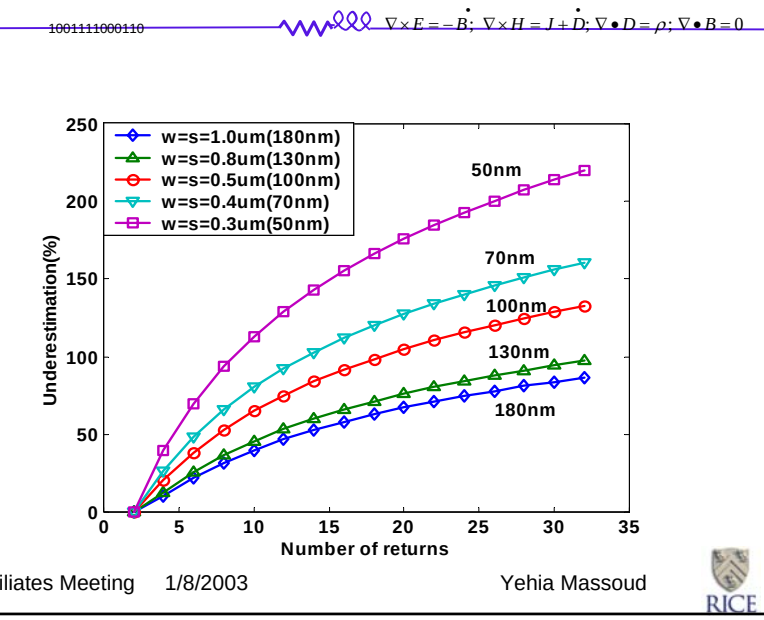
$$a_1 = \frac{5N}{6} - \frac{1}{3N} + \frac{1}{2N^2}$$

$$a_2 = \frac{3}{2} + \frac{3}{4N} - \frac{\log(N+1)}{2N} + \frac{1}{N}\left(\sum_{i=1}^{N}\log i + \log N\right)$$

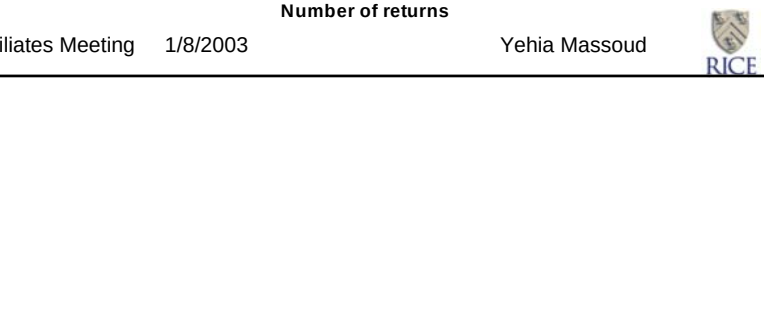
$$+ \frac{1}{2N^2}\sum_{i=1}^{N-1} i\left(2\log(i) - \log(i+1) - \log(2N+1-i)\right)$$

Formula Vs Field Solvers

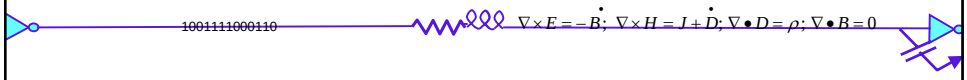




Predictions for future technology

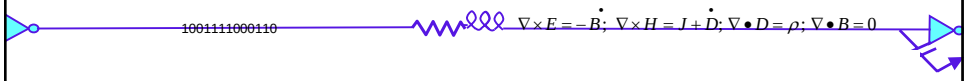


Interconnect Challenge



- Need **fast** and **accurate** extractors
- But What do you do with all these RLC elements? (Spice definitely can't handle that!)
  - Need to represent these big circuits using **reduced order models** that are fast to build
    - **Spice** can handle them
    - Can be used in **design optimization**

Deep Sub-Micron Challenges

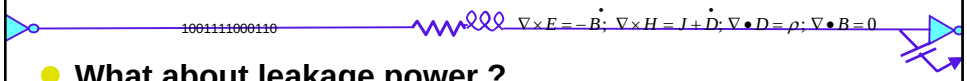


- **Interconnect Extraction and Modeling**
- **Power reduction**
- **Signal integrity (noise, IR drop, ringing)**
- **System-on-chip integration**
- **Educational**

Power Challenge

- **Why should we reduce power ?**
  - **Everything that uses battery !**
  - **It is becoming hard to cool chips down ! (heat sinks, fans, …?)**
- **POWER= P(dynamic) + P (leakage) + …**
- **P(dynamic) has been dominating**
- **P(dynamic)=** $C_L V_{dd}^2$
- **So reduce Vdd ! (went down 5 Volts to sub 1V now)**
- **Problem [Delay increases as Vdd decreases]**
- **Research**
  - **Dual Vdd**
    - **Use high Vdd on part where you need speed**
    - **Use low Vdd otherwise**
  - **Optimal regions for power and delay [power-delay product]**

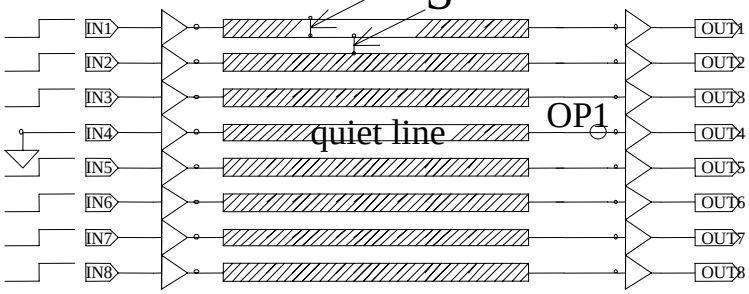
Power Challenge



- **What about leakage power ?**
  - **Important whenever you use batteries**
    - **(Telecomm; Medical; mobile electronics; ...)**
  - **Inversely proportional to threshold voltage (exp. relation)**
  - **Problem [Delay increases as Vt increases]**
- **To enable low Vdd logic, we have to use low Vt**
  - **a 100mv drop in Vt increases leakage by an ORDER of magnitude**
  - **So leakage power has been increasing with scaling**
  - **Leakage power will be soon as big as dynamic**
- **Research**
  - **Dual Vt (Multi Vt)**
    - **Use low Vt on part where you need speed**
    - **Use high Vt otherwise**
  - **Dual Vdd- Dual Vt**

Signal Integrity (Coupling Noise)

W=3um, S=1.5um, Metal 6 W S

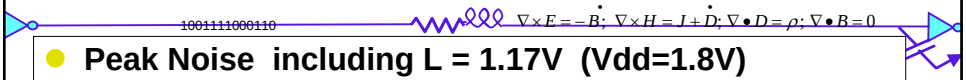


Eight-Bit Buss Cross-Talk Example

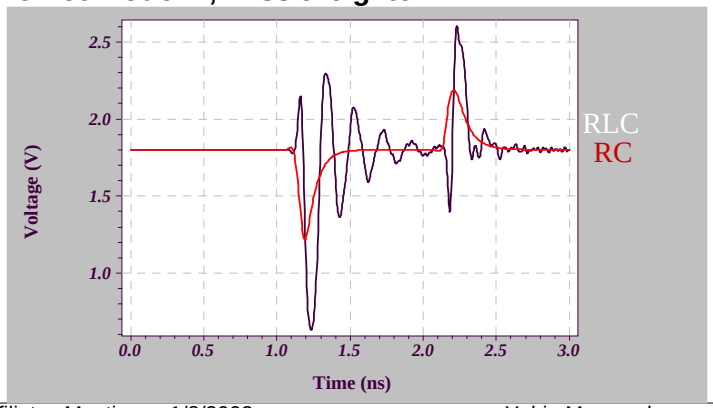
Tech=0.18um,Vdd=1.8v, Wire length=3000um,

RICE

Noise induced on the quiet line?

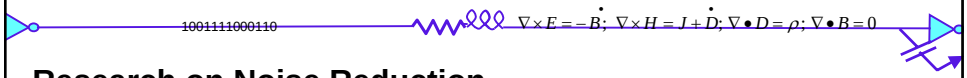


- **Peak Noise including L = 1.17V (Vdd=1.8V)**
- **Peak Noise ignoring L = 0.54V 0.18um tech**
  - **Do not model L, miss the glitch!**



RICE

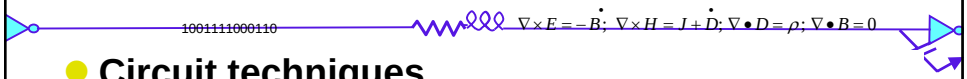
Noise Reduction remedies



Research on Noise Reduction

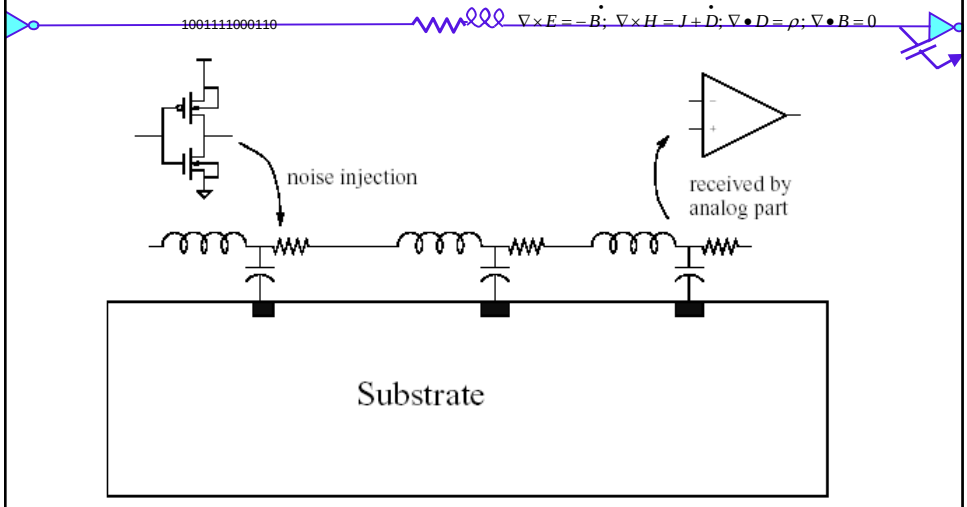
- **Architectural**
  - **Controlling bus width and spacing**
    - can be good enough if inductance is not an issue
  - **Shielding**
    - Excellent for RC problems
    - Good if L is a factor but may not be enough because of the inductance long range effects

Noise Reduction remedies

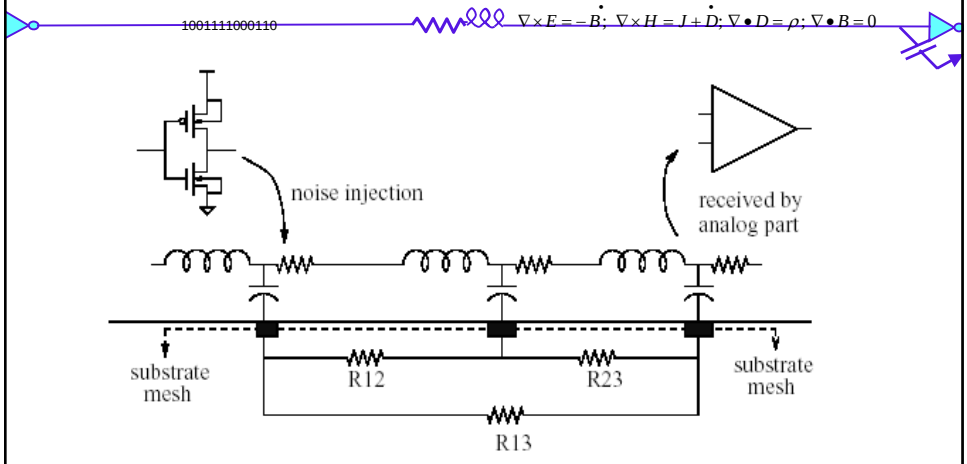


- **Circuit techniques**
  - **repeaters**
    - **Repeaters work at a cost**
      - – additional area, delay, and power
      - – Can not use aggressive repeaters (have inferior noise properties)
  - **differential signaling**
    - **Less noise production**
      - – can route over sensitive areas
    - **more noise immune**
      - – Useful for global nets
    - **Fast but consumes static power?**

System-on-Chip Integration (Model substrate coupling)

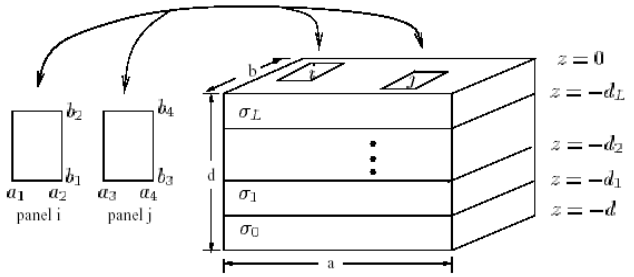


Model substrate as resistive network



Problem description

1001111000110 $\nabla\times E=-\dot{B};\ \nabla\times H=J+\dot{D};\ \nabla\bullet D=\rho;\ \nabla\bullet B=0$



Basic procedure of BEM approach

1001111000110 $\nabla\times E=-\dot{B};\ \nabla\times H=J+\dot{D};\ \nabla\bullet D=\rho;\ \nabla\bullet B=0$

- **Assume one contact has charge, it induces potential at the other contact**

Charge at Contact i → Maxwell eq. → Potential at Contact j

- **Maxwell in integral form**

$$\Phi(x,y,z)=\int_{V'}\rho(x',y',z')G(x,y,z,x',y',z')dV'$$

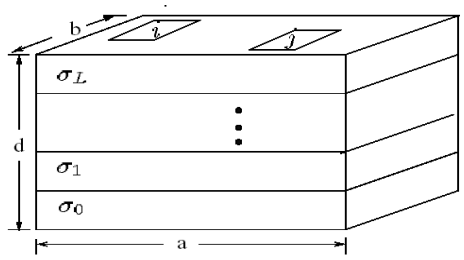
- **In matrix form** $\Phi = PQ$

$$P_p(i,j)=\frac{1}{V_iV_j}\iint G(x,y,z,x',y',z')dV_i dV_j$$

- **Formulate Green function G**
  - **Enforce boundary conditions (Floating or Grounded substrate)**
- **Construct potential coefficient matrix P**
- **solve the linear system and compute the conductance matrix**

Effects of distance between contacts

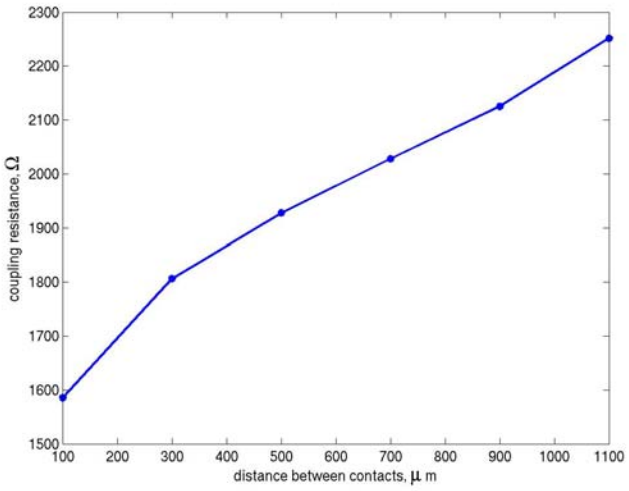
1001111000110 $\nabla \times E = -\dot{B};\ \nabla \times H = J + \dot{D};\ \nabla \bullet D = \rho;\ \nabla \bullet B = 0$



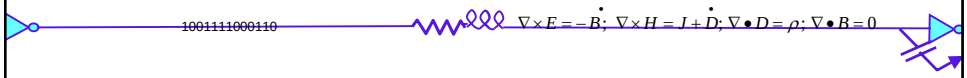
- **Size of substrate: a=b=1600um**
- **Depth of substrate: d=50um**

Effects of distance between contacts

1001111000110 $\nabla \times E = -\dot{B};\ \nabla \times H = J + \dot{D};\ \nabla \bullet D = \rho;\ \nabla \bullet B = 0$

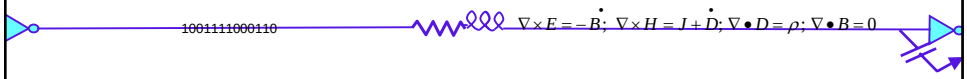


Educational Challenge



- **As feature size decreases, more EM effects need to understood and modeled**
  - **Ground ?, L, inductive coupling, electromagnetic interference, transmission line effects,**
- **Digital Vs analog ?**
  - **Digital signals are looking (behaving) like analog signals**
  - **Integration of digital and analog parts on same chip**
- **Numerical Analysis**
  - **Needed to solve these complicated integral/differential equations!**

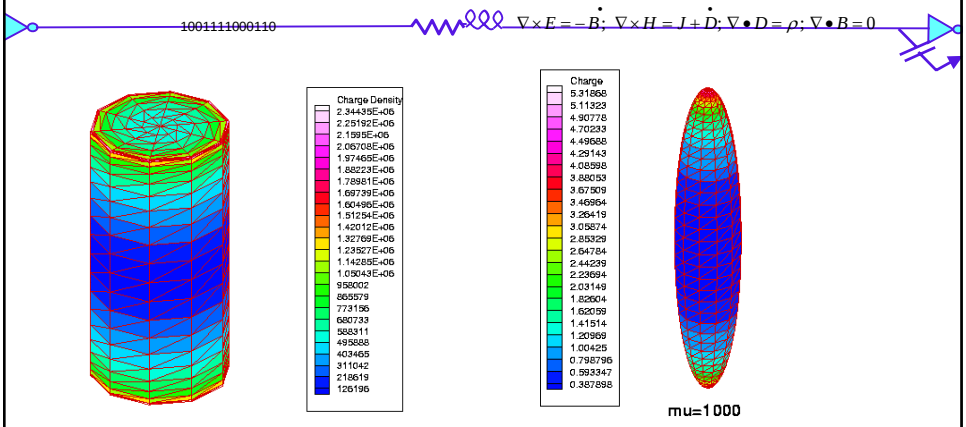
Amazing Similarities



Maxwell's Equations RULES!

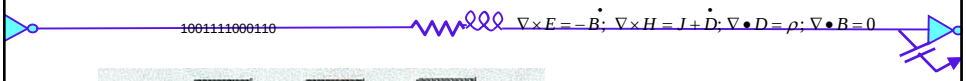
- EM simulations
- VLSI Modeling
- MEMS Modeling [sensors, Actuators, Micro-motors]
  - Applications [Automotive, Biomedical, Defense]
- RF and wireless Modeling
- Nanotechnology [Talk by N. Halas on Nanoshells!]

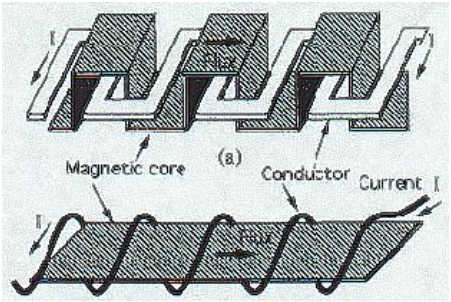
(EM) Charge Distribution



- **Charge distribution (High density at corners)**
- **Within 1% from theory**

MEMS

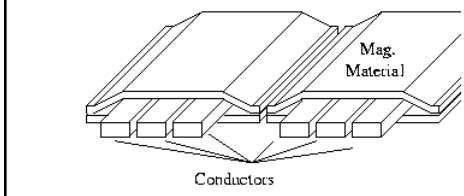




Different types of Inductors
Ref: M. Allen from GTECH

- High Permeability materials are often used in MEMS applications to increase inductance or magnetic force

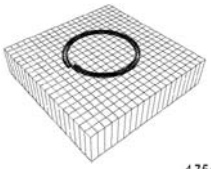
MEMS



Multi layer Micro-fabricated Inductor [L. Daniel et.al.]

Extracted inductance is within 3% from measured inductance

RF Modeling



Spiral inductor