A 40GS/s Track-and-Hold Amplifier with 62dB SFDR3 in 45nm CMOS SOI

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***Abstract*—A 40GS/s Track-and-Hold amplifier with active cancellation capability is presented to mitigate the effect of leakage in transmission gate during the holding mode. A single-ended RF input signal is converted to a differential signal that feeds the active cancellation network. A record SFDR3 of 62dB with 40GS/s and 5GHz input frequency is reported in 45nm CMOS SOI. A droop voltage of 20μv/ns is measured. An isolation of 32dB at 1GHz between the holding and tracking modes is recorded.**

***Index Terms*—Active Cancellation, Track and Hold Amplifier, ADC, SFDR, CMOS, Silicon, SOI.**

I. Introduction

Sample and hold (S/H) or track and hold (T/H) amplifier are used in the core of any ADC. These circuits sample the input signal and hold its value for a specific period of time. Traditional S/H or T/H circuits work well in low input frequencies. However, as the input frequency increases, the isolation between the input and output of the T/H (or S/H) amplifier in the hold mode decreases, which reduces the effective number of bits. This is because the isolation of a CMOS switch degrades at high frequencies. In a series switch, the gate-source (C_{GS}) and gate-drain (C_{GD}) parasitic capacitors provides an alternate path for the signal to pass. This path causes considerable amount of coupling at high frequencies and reduces the isolation. The low isolation changes the voltage of the holding capacitor in the hold mode and increases the error.

II. Proposed Architecture

In the proposed architecture, an active cancellation circuitry is designed to maximize the isolation between the input signal and the holding capacitor in the hold mode. To achieve active cancellation, a negative copy of the input signal is generated on-chip using a single-ended to differential amplifier. Shown in Fig.1 is the circuit diagram of the T/H amplifier with active cancellation. Single-ended RF signal is fed to a differential amplifier, which converts the input signal to a differential pair, one being the negative copy of the other. Ideally, this pair needs to have same amplitude and 180° phase difference in all frequencies. However due to non-idealities caused by mismatch and process variations, they have large phase and amplitude imbalance. To reduce this imbalance, the complementary pair is passed through a signal conditioning circuitry consisting of three consecutive stages of differential amplifier and voltage follower. The 3dB bandwidth of the combined system is 50GHz in simulation. At the output of the signal conditioning block, the differential signals have an amplitude imbalance of 3dB and phase imbalance of less than 10° at 100GHz.

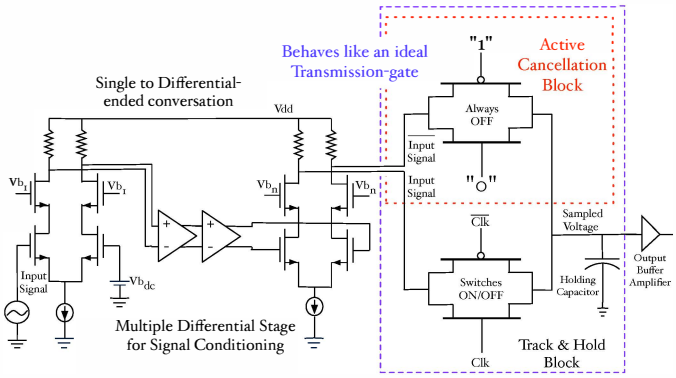

Fig. 1: The schematic of T/H circuit with active-cancellation.

After the signal conditioning block, the differential signal, which consists of the main signal and its negative copy, are passed through a T/H sampler with a differential input. A conventional T/H system consists of one transmission-gate where the input signal is sampled. When the system is in the tracking state, the transmission gate conducts and charges the capacitor. During the hold state, the transmission gate changes to isolation mode and the capacitor holds the charge. However, due to the leakage of the transmission gate in the isolation mode, the charge in the holding capacitor changes, which increases the error and reduces the effective number of bits. In the proposed architecture, apart from the standard transmission gate, a second transmission gate is added, which is fed with the negative copy of the input. This added transmission gate is always in "Off" state or isolation mode. During the hold state, both transmission-gates inject charge to the capacitor due to leakage, however, the charges injected are opposite in sign and cancel each other. This charge canceling mechanism mitigates the leakage effect. This combined process can be seen as T/H with active cancellation. Finally a high input impedance buffer amplifies the voltage of the holding capacitor and feeds a 50Ω load.

To operate the transmission switch, a clock (clk) and its complementary signal (clk′) are required. A single ended 40GHz external clock is provided which is converted into two complementary clocks with sub-10ps rise time. In this process, the clock is divided into two branches with one having an extra NOT gate to generate the complementary signal. Adding an extra NOT gate adds delay in one of the paths. This delay is

compensated by adjusting the number of transistor in one of the NOT. The fewer the number of transistors, the more time will it takes to drive the gate capacitance of the preceding NOT gate. Thus by changing the number of transistors, the delay can be appropriately compensated. In simulation, the delay was compensated with picosecond accuracy.

III. Measurement Results

The T/H circuit with active-cancellation is characterized using 67GHz RF probes and a two-channel 70GHz sampling oscilloscope (Agilent DCA-X 86100D). The RF signal generator and the sampling clock are synchronized using a 10MHz reference signal as shown in Fig.2.

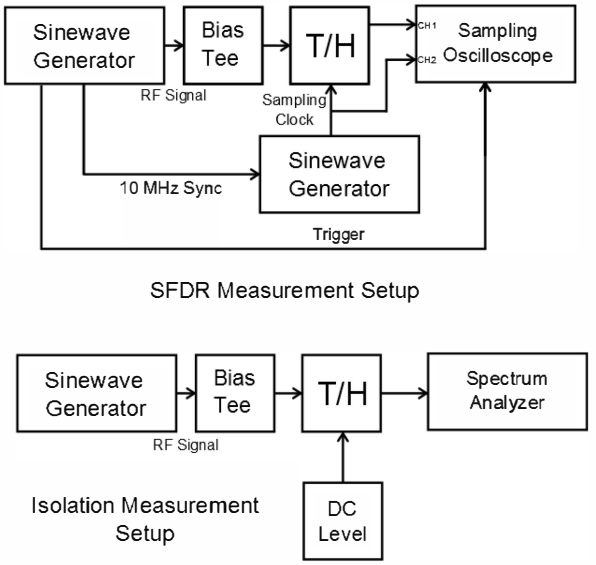

Fig. 2: Block diagram of the test setup.

In order to characterize the performance of the active cancellation block, the isolation of the transmission gate in the hold state should be measured. To measure this isolation, first, the spectrum of the output signal is recorded in the tracking mode. This should characterize the amplifiers and all other blocks in the signal path. Next, the state is changed to the hold mode, and the output spectrum is recorded again. The difference between the results of the first and second experiments is used to calculate the isolation. The input frequency is swept from 100MHz to 10GHz and the isolation is measured as shown in Fig.3. Based on this measurement, an isolation of better than 32dB is achieved at 1GHz.

In a separate measurement, to characterize the Spurious-Free Dynamic Range (SFDR) of the sampling block, an input signal with a frequency of 1GHz was sampled at frequencies 5GHz to 30GHz. This measurement was made by calculating 30-point DFT of 1GHz signal, sampled at 30GS/s over a

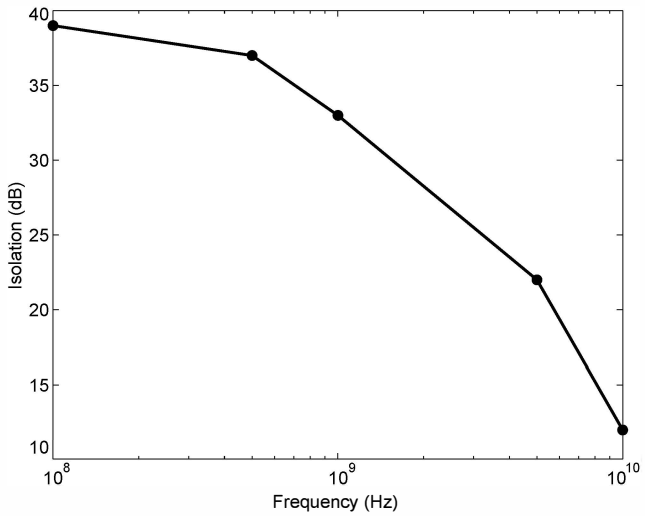

Fig. 3: Measured isolation by comparing the track and hold modes.

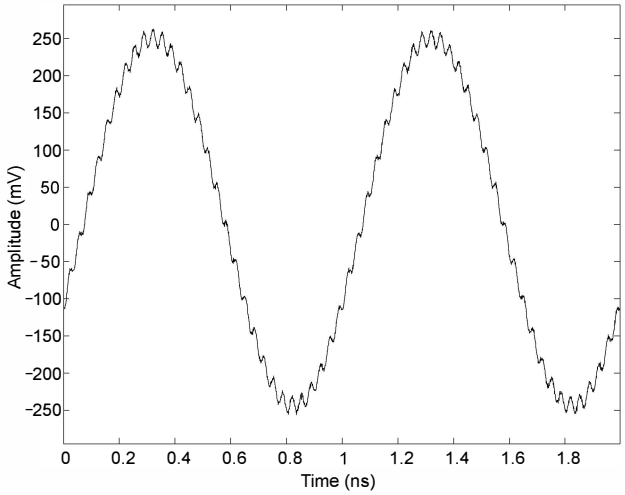

Fig. 4: Measured time domain waveform of a 1GHz input signal with real time sampling frequency of 30GS/s.

period of 1ns, averaged 128 times to reduce the noise of the oscilloscope. These points were taken in the middle of the hold-state in the sampled waveform with constant repetition rate. The time-domain waveform of the sampled signal is shown in Fig.4.

Fig.5 shows the 2nd and 3rd harmonic Spurious-Free Dynamic Range (SFDR2 and SFDR3) for the system using different sampling rates. The hold-state SFDRn denotes the ratio of the fundamental frequency magnitude over n^{th} harmonic spurious magnitude. As evident from Fig.5, 68dB SFDR3 and 67dB SFDR2 were observed for 1GHz signal sampled at 30GS/s. Moreover, SFDRn versus input signal power is measured to demonstrate the linearity of the T/H amplifier. As evident from Fig.6, 62dB SFDR3 and 55dB SFDR2 is observed for 5GHz signal sampled at 40GS/s.

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IC Specifications	This work	[1]	[2]
Process	45nm SOI CMOS	130nm CMOS	180nm SiGe BiCMOS
Die specifications	850µm × 450µm, 15 pins	1 mm^2	1.28 × l.15 mm^2
Supply Voltage	2.5V, 1V	1.8V	4V, 3.3V
Power consumption	415mW	270mW	640mW
Sampler			
Input	Single-ended	Differential	Differential
Maximum Sampling Rate	>40GS/s	30GS/s	50GS/s
SFDR3	>62dB@ Fin=5GHz, Fs=40GS/s	SFDR=40dB@ Fin=1GHz, Fs=30GS/s	SFDR=42dBc@Tone=30,30.1GHz, Fs=40GS/s
SFDR2	>55dB@ Fin=5GHz, Fs=40GS/s		
Isolation	>30dB @ Fin=1GHz	Not reported	Not reported
Droop Voltage	20µv/ns	10 mV/ns	Not reported

TABLE I: Comparison table with prior art.

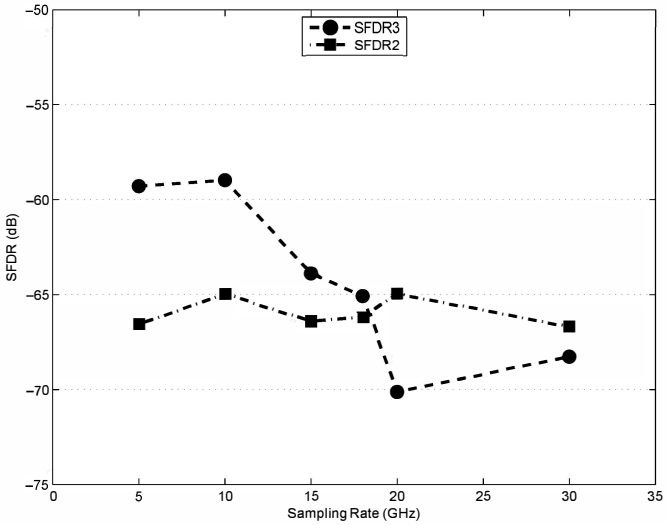

Fig. 5: Measured SFDR2 and SFDR3 versus sampling frequency.

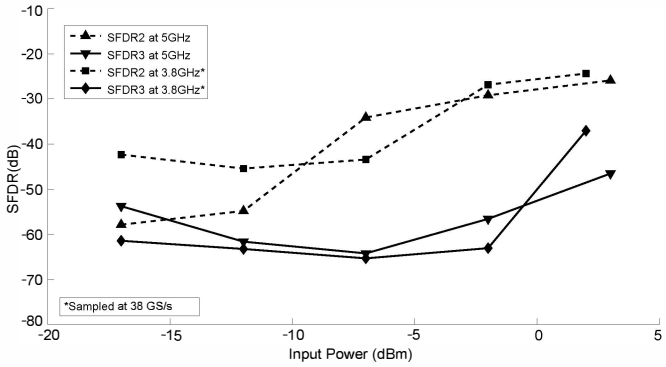

Fig. 6: Measured SFDR2 and SFDR3 versus input signal power at sampling frequency 40GS/s.

The results of this chip is compared with the prior art in table 1.

In addition to the above measurements, the droop voltage, which is a measure of decay of the capacitor voltage during the hold-state over a period of time, is reported. A droop voltage of 20μv/ns was observed for a sampled signal of 350mV. This is equivalent to 10-bit accuracy for a hold time of 10ns.

Finally, the chip micrograph is shown in Fig.7. The chip is fabricated in 45nm SOI technology and occupies an area of 850μm×450μm including pads.

IV. Acknowledgment

The authors acknowledges the help of Mr. Rafael Puhl in the measurements. They also acknowledge DARPA for fabrication support.

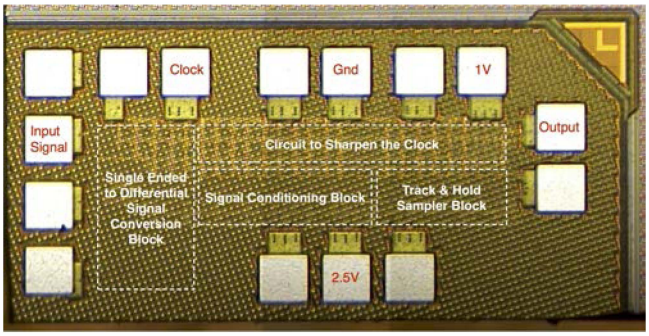

Fig. 7: Chip micrograph in 45nm.

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[2] Jaesik Lee, et al., "A 50GS/s Distributed T/H Amplifier in 0.18μm SiGe BiCMOS", *IEEE Solid-State Circuits Conference (ISSCC)*, pp. 466 - 616, 2007.