Impact of Layout on the Performance of Photodiodes in 0.18µm CMOS SOI

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Abstract: The impact of layout on the responsivity and bandwidth of photodiodes is studied and summarized. The photodiodes are fabricated in a 0.18µm CMOS SOI process technology. The measurements are performed at wavelengths near 850nm.

1. Introduction

Monolithically integrated optical receivers in CMOS technology have received great interests during the past few years [1]. As photodetectors and electronic circuits are implemented on the same chip, the receivers enjoy higher reliability, lower cost, and boosted performance due to the absence of off-chip parasitics such as bondwires. One of the major challenges in building monolithic optical receivers is to implement a high-performance photodetector in a conventional CMOS technology. In bulk CMOS processes, the slow diffusion current generated deep in the substrate significantly reduces the bandwidth of the photodiode. In contrast, photodiodes implemented in CMOS SOI process technologies exhibit a much larger bandwidth, because the buried oxide layer blocks the slow carriers generated deep in the substrate [2]. For example, in [3], we have reported a photodiode implemented in a conventional 0.18µm CMOS SOI process with a bandwidth exceeding 9GHz.

Recently, several papers [2,4] have addressed the impact of the layout on the performance of photodiodes fabricated in a bulk CMOS process. However, their results and conclusions do not necessarily apply to photodiodes in CMOS SOI process. In this paper, the impact of the layout on photodiodes implemented in CMOS SOI process technology will be studied. The photodiodes reported in this article are all fabricated in a conventional 0.18µm CMOS SOI technology without performing any post-processing.

2. Photodiode layout and measurement setup

The photodiodes studied in this work are P+/N-well diodes, with a cross section shown in Figure 1 [5]. For fair comparison, the outer dimensions of the photodiodes are kept same at 50µm by 50µm. The width of the polysilicon, the width of the metal, and the distance between two adjacent fingers will be varied to study their effects. Two types of measurements are performed in this work. In the first experiment, the bandwidth and the responsivity of the photodiode are measured. In the second experiment, the resistance and the capacitance of the photodiode are extracted from the measured S_{11} values. In the first experiment, a directly-modulated 850nm VCSEL is used as the laser source. The laser beam is coupled into a multimode fiber and directed to the photodiode from top of the chip. Both the VCSEL and photodiodes are biased externally using high-frequency bias-tees. An Agilent network analyzer, N5230C, is used to measure the frequency response of the photodiodes. The photo current is recorded to calculate the responsivity. In the second experiment, the input reflection parameter of the photodiode, S_{11}, is measured using the network analyzer. The contact resistance and capacitance are extracted from the S_{11} values.

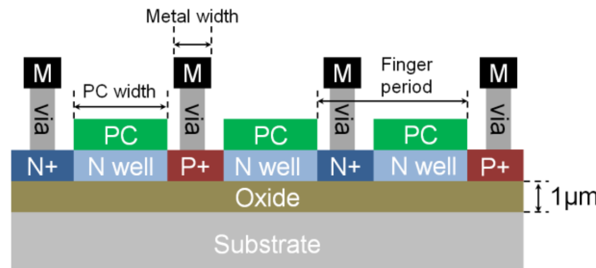

Figure 1: Structure of the P+/N well photodiode. Here "M" stands for metal and "PC" stands for polysilicon. The layout parameters that are studied in this work include the polysilicon width, metal width, and the finger period. The width of P+ region is equal to the width of N+ region.

3. Results

We first study the effect of the metal width. As shown in Figure 2(a), for a fixed polysilicon width of 0.4µm and the finger period of 1.5µm, we have not observed a significant change in the bandwidth as metal width increased from

0.3µm to 1.1µm. For the structure discussed in this work, the metal contact resistance is estimated to vary between 0.1Ω and 1Ω. Since this resistance is much smaller than the 50Ω load impedance of the measurement setup, it does not have a major effect on the bandwidth. However, as the metal becomes wider, less number of photons reaches the active silicon surface, which results in a lower responsivity. By increasing the metal width from 0.3µm to 1.1µm, the responsivity decreases by a factor of 3X.

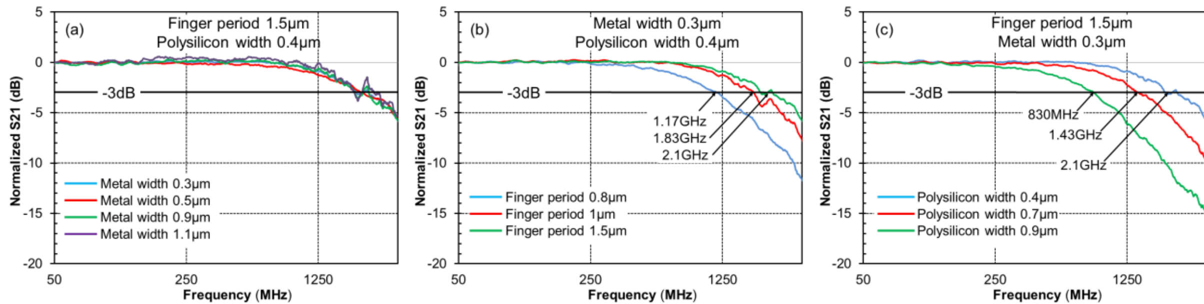

Figure 2: Effects of the layout structures on the performance of the photodiodes. (a) Photodiodes with different metal widths. (b) Photodiodes with different finger periods. (c) Photodiodes with different polysilicon width.

We next study the effect of the finger period. For a fixed polysilicon and metal width, the bandwidth of the photodiode rises from 1.17GHz to 2.1GHz as the finger period increases from 0.8µm to 1.5µm (Figure 2(b)). Meanwhile, the extracted capacitance for the photodiode decreases from 2.2pF to 1.1pF. This drop increases the RC-limited 3dB bandwidth from 1.4GHz to 2.8GHz. In this region the bandwidth is limited by the capacitance rather than the intrinsic speed. The capacitance decreases because the total number of P+/N-Well junctions reduces. By increasing the finger period from 0.8µm to 1.5µm, the area of the metal on the photodiode decreases, resulting in a 2.5X improvement in the responsivity.

We finally report the effects of the polysilicon width. For the P+/N-well diode studied in this work, the silicon area covered by the polysilicon is the N-well region. Therefore, increasing polysilicon width also increases N-well width and improves the responsivity. As shown in Figure 2(c), by increasing the polysilicon width from 0.4µm to 0.9µm, the photodiode bandwidth decreases from 2.1GHz to 830MHz. We have verified that the extracted photodiode capacitance remains constant at 1.1pF. This suggests that the reduction in the bandwidth results from the change in the intrinsic speed of the photodiode. For the lateral P+/N-well photodiode studied in this work, the photo current is composed of the drift current in the depletion region, the electron diffusion current in the P+ region, and the hole diffusion current in the N-well region. Since the N-well width directly impacts the hole diffusion current, it can be inferred that the speed of the hole diffusion current limits the bandwidth of the photodiode. In [4] the diffusion length for holes in N-well at 0.18µm technology node is estimated to be on the order of 10µm, much larger than the width of N-well in this study. Therefore, the majority of the holes generated in the N-well contribute to the total photo current. Since the width of the N-well increases the traveling time required for holes to reach the depletion region, the bandwidth is reduced.

4. Conclusions

In this work, we reported the effects of layout on the performance of photodiodes in a 0.18µm CMOS SOI process technology. It is observed that for an small polysilicon width the photodiode bandwidth is limited by the capacitance of the photodiode (RC limit), while for a large polysilicon width, the bandwidth is limited by the diffusion of the holes (intrinsic limit). To achieve a higher bandwidth, the width of the polysilicon should be kept small to increase the intrinsic speed, while the finger period should be made large to reduce the capacitance.

5. References

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