A Linearized, Low-Phase-Noise VCO-Based 25-GHz PLL With Autonomic Biasing

Bodhisatwa Sadhu, *Member, IEEE*, Mark A. Ferriss, Arun S. Natarajan, Soner Yaldiz, *Member, IEEE*, Jean-Olivier Plouchart, *Senior Member, IEEE*, Alexander V. Rylyakov, Alberto Valdes-Garcia, Benjamin D. Parker, Aydin Babakhani, Scott Reynolds, Xin Li, *Senior Member, IEEE*, Larry Pileggi, *Fellow, IEEE*, Ramesh Harjani, *Fellow, IEEE*, José A. Tierno, and Daniel Friedman, *Member, IEEE*

***Abstract*—This paper describes a new approach to low-phase-noise LC VCO design based on transconductance linearization of the active devices. A prototype 25 GHz VCO based on this linearization approach is integrated in a dual-path PLL and achieves superior performance compared to the state of the art. The design is implemented in 32 nm SOI CMOS technology and achieves a phase noise of −130 dBc/Hz at a 10 MHz offset from a 22 GHz carrier. Additionally, the paper introduces a new layout approach for switched capacitor arrays that enables a wide tuning range of 23%. More than 1500 measurements of the PLL across PVT variations were taken, further validating the proposed design. Phase noise variation across 55 dies for four different frequencies is $\sigma < 0.6$ dB. Also, phase noise variation across supply voltages of 0.7–1.5 V is 2 dB and across 60°C temperature variation is 3 dB. At the 25 GHz center frequency, the VCO FOM_T is 188 dBc/Hz. Additionally, a digitally assisted autonomic biasing technique is implemented in the PLL to provide a phase noise and power optimized VCO bias across frequency and process. Measurement results indicate the efficacy of the autonomic biasing scheme.**

***Index Terms*—Calibration, circuit noise, digitally controlled oscillators, electromagnetic coupling, feedback, high-speed integrated circuits, integrated circuit noise, K-band, linearity, linearization, local oscillators, millimeter-wave circuits, millimeter-wave communication, millimeter-wave integrated circuits, mutual coupling, negative feedback, nonlinear circuits, oscillators, phase-locked loop (PLL), phase noise, signal-to-noise ratio (SNR), 60 GHz, transconductance, tunable circuits and devices, tuning range, voltage-controlled oscillators (VCOs).**

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B. Sadhu was with the University of Minnesota, Minneapolis, MN 55455 USA. He is now with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: sadhu@us.ibm.com).

M. A. Ferriss, A. S. Natarajan, J.-O. Plouchart, A. V. Rylyakov, A. Valdes-Garcia, B. D. Parker, S. Reynolds, and D. Friedman are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

S. Yaldiz was with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA, and also with Carnegie Mellon University, Pittsburgh, PA 15213 USA. He is currently with Intel Corporation.

A. Babakhani was with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA. He is now with Rice University, Houston, TX 77005 USA.

X. Li and L. Pileggi are with Carnegie Mellon University, Pittsburgh, PA 15213 USA.

R. Harjani is with the University of Minnesota, Minneapolis, MN 55455 USA.

J. A. Tierno was with the IBM T. J. Watson Research Center, Yorktown Heights, 10598 NY. He is now with Apple Inc., Cupertino, CA 95015 USA.

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I. Introduction

PHASE noise in CMOS *LC* VCOs is fundamentally limited by the oscillation amplitude and the inherent device noise. In this work, we introduce a new approach based on *transconductance linearization* of the active devices that increases the signal swing while reducing the active device noise contribution in *LC* VCOs. Consequently, this provides a significant improvement in the VCO phase-noise performance. We implement this approach using a capacitive transformer-based signal feedback technique. Additionally, for the capacitor array within the VCO, we utilize a new layout approach based on interconnect inductance mitigation. Using these novel approaches, we are able to optimize the VCO for phase noise, power, and tuning range. Consequently, the implemented PLL incorporating the resulting linear transconductance VCO (LiT VCO) achieves both an excellent measured phase noise of −130 dBc/Hz at 22 GHz (10-MHz offset), and, in contrast to the 6.7% tuning range of the VCO-only result reported using a somewhat similar technique in [1], a large frequency tuning range (FTR) of 23% (21.8–27.5 GHz). This range covers operation over 22.8–26.4 GHz, with margin, meeting requirements for a 60-GHz superheterodyne radio [2].

Some results from this implementation were presented in [3]. This paper explains the linearization theory in detail and presents additional results. In addition, it presents a novel digitally assisted VCO biasing technique to autonomically optimize the power and/or the phase noise depending on the specific application requirements across frequency and process variation. The optimal bias is accurately predicted from the outputs of an on-chip peak detector, an on-chip frequency detector, and the VCO bias current based on the indirect sensing methodology outlined in [4]. Measurement results validate the efficacy of the proposed autonomic biasing scheme.

Section II of this paper describes the transconductance linearization technique for phase noise improvement. Implementation details of the VCO within a dual-path PLL are described in Section III. Measurement results characterizing the VCO are discussed in Section IV. The digitally controlled autonomic biasing technique for power and phase-noise optimization is described in Section V. Finally, conclusions are drawn in Section VI.

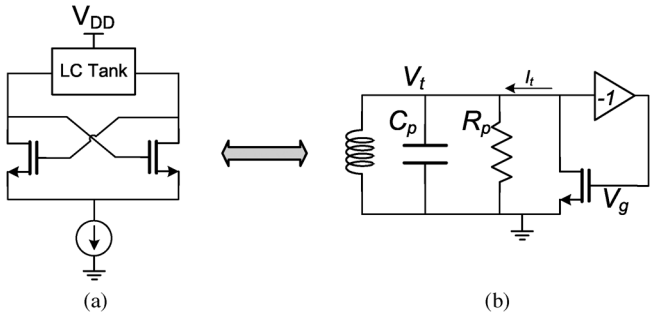

Fig. 1. Cross-coupled VCO: (a) full circuit and (b) half circuit.

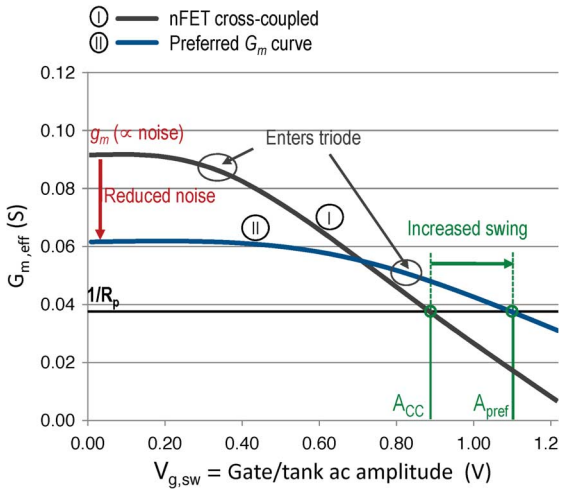

Fig. 2. Transconductance versus voltage swing showing a typical oscillator G_m curve and a preferred curve for improved phase noise.

II. Transconductance Linearization

This work explores the benefits of transconductance linearization for improved phase noise in LC VCOs. To understand the effect of transconductance linearization, we first consider the widely used FET based cross-coupled VCO topology shown in Fig. 1(a). For analysis, the circuit can be represented by an equivalent half circuit, shown in Fig. 1(b). The oscillation amplitude in this VCO is limited by the nonlinearity of the large-signal device transconductance (G_m).[1] To provide some intuition regarding the key drivers of the phase noise performance, we plot the effective large-signal transconductance $G_{m,eff}$ versus gate ac swing $(V_{g,sw})$ for the cross-coupled VCO in Curve I in Fig. 2. From this curve, we make two important observations.

1) *Oscillation amplitude*. As shown, the G_m drops with increasing oscillation amplitude $(= V_{g,sw})$. The equilibrium amplitude A_{CC} is reached when $G_m R_p = 1$. The main source of nonlinearity is the transistor entering the triode region.
2) *Active device noise*. Fig. 2 also shows the small-signal transconductance (g_m) corresponding to G_m for an infinitesimally small amplitude of oscillation, i.e. $g_m (= G_m(V_{g,sw} = 0))$. Note that this g_m determines the active device noise power at the oscillation zero crossings (when the oscillator's phase noise sensitivity is at its highest). As a result, with other factors remaining constant, the device g_m is a significant determinant of the VCO phase-noise performance.

[1]Here, G_m is defined as $G_m = I_\omega / V_\omega$, where I_ω and V_ω are the ac drain current and ac gate voltage at the frequency of oscillation ω.

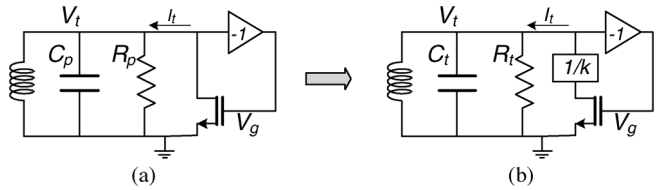

Fig. 3. Feedback concept for G_m linearlization using lower voltage swing on the drain node: (a) cross-coupled; (b) with feedback.

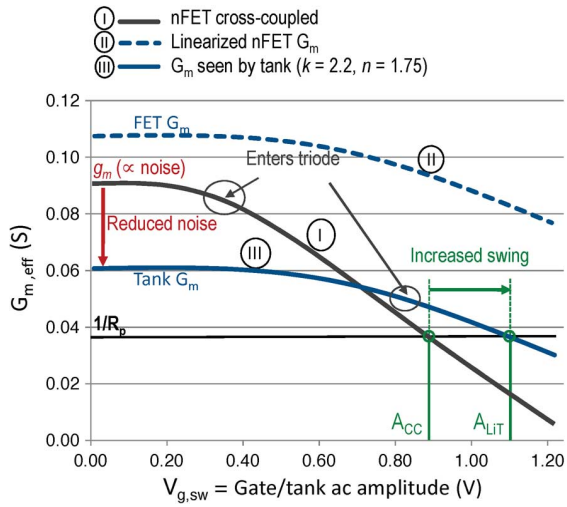

Fig. 4. Transconductance linearization in LiT VCO.

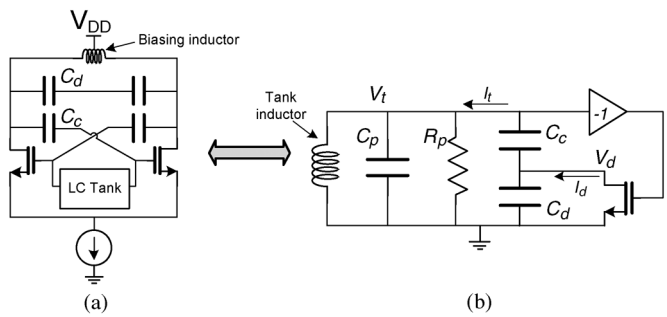

Fig. 5. LiT VCO: (a) full circuit and (b) half circuit.

From these two observations, we conclude that a more linear G_m curve could enable a larger amplitude of oscillation, as well as contribute lower active noise, improving the signal-to-noise ratio (SNR), and, consequently, the phase noise of the VCO. Such a linearized G_m curve, which is suitable for superior phase-noise performance,[2] is shown in Curve II in Fig. 2.

The desired transconductance linearization may be achieved using different feedback techniques. Transconductance linearization has been used for improving the phase noise in BJT-based oscillators by reducing the swing on the nonlinear base node [5]. However, this technique is not suitable for

[2]Note that this linearization signifies a direct tradeoff between the start-up margin, denoted by $g_m / G_{m,eq} = g_m \cdot R_p$, and the achieved phase noise in the oscillator.

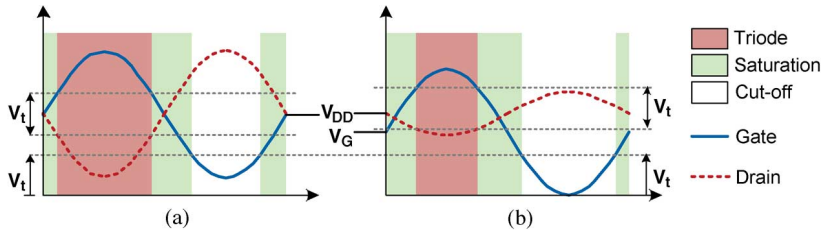

Fig. 6. Gate and drain waveforms for (a) a cross-coupled VCO and (b) a LiT VCO showing the reduction in triode operation.

MOSFET-based oscillators. In MOSFETs, since the drain node is primarily responsible for the large-signal nonlinear device transconductance, a conceptual feedback scheme shown in Fig. 3 can achieve the desired linearization. As shown in Fig. 3(b), only a fraction of the tank/gate amplitude is fed to the drain, thereby reducing the swing on the drain $V_d = V_t/k$. The resulting reduction in triode operation linearizes the G_m curve, as shown in Curve II (as compared with the cross-coupled VCO G_m shown in Curve I) in Fig. 4,[3] for a division factor of $k = 2.2$.

This feedback scheme can be realized by using a capacitive divider as shown in Fig. 5(a). The half circuit model for this LiT VCO is shown in Fig. 5(b). The capacitive divider ensures that the drain swing is a fraction $(1/k)$ of the swing across the LC tank $(V_{g,sw})$, where

$$k \approx \frac{C_c + C_d}{C_c}. \tag{1}$$

Moreover, the capacitive dc isolation allows the FET gate $(V_{\mathrm{g,bias}})$ to be biased lower than its drain (V_{DD}), further reducing triode operation. This reduction in triode operation based on the signal swings on the gate and drain nodes is shown diagrammatically in Fig. 6. Consequently, the FET nonlinearity is reduced, resulting in the more linear device G_m as shown in Curve II in Fig. 4 $(k = 2.2)$.

Also note that,due to the capacitive division, only a part of the FET ac current flows into the tank as shown in Fig. 4. From Fig. 5(b), where I_d is the FET drain current and I_t is the fraction of I_d flowing into the tank, at the resonant frequency, we have

$$I_t = \frac{I_d}{n}$$

where

$$n = \frac{Z_{C_d} + Z_{C_c} + R_p}{Z_{C_d}} = \frac{C_c + C_d + R_p.sC_d.C_c}{C_c}. \tag{2}$$

This reduces the effective G_m seen by the tank (to $G_{m,tank}$) as plotted in Curve III in Fig. 4 for $k = 2.2$ and $n = 1.75$. Note that this curve is very similar to the preferred curve plotted in Fig. 2. The resulting oscillation amplitude, A_{LiT}, using curve III in Fig. 4 for the LiT VCO, is larger than A_{CC} for a comparable cross-coupled VCO.

As shown in Fig. 7, the larger oscillation amplitude can be viewed as a voltage limit extension in the LiT VCO. In this way, the LiT VCO enables a power vs. phase noise trade-off beyond the voltage limit imposed in a cross-coupled VCO.

[3]Note that this also increases the small-signal transconductance (g_m) due to increased dc current consumption caused by the device not entering the triode region due to the smaller drain voltage swing.

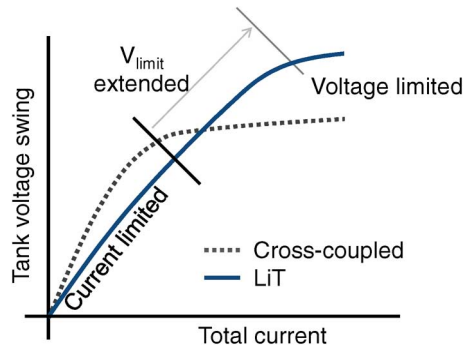

Fig. 7. Voltage-limited regime extension in LiT VCO.

Additionally, as expected, VCO phase noise contribution from the FETs is reduced through this technique: for the LiT VCO, the effective transconductance across the tank $(g_{m,tank})$ is lower than the device g_m by a factor n (i.e. $g_{m,tank} = g_m/n$). Therefore, at the zero crossings, the noise contribution of the active devices is reduced by the same amount as shown in Fig. 4. Additionally, by eliminating triode operation, the LiT VCO reduces degradation of the loaded tank Q. Consequently, the LiT VCO enables a larger tank amplitude and yet injects less noise into the tank as compared to the cross-coupled VCO, leading to significant improvements in phase noise.

The foregoing theory of LiT VCO operation enables design optimization by utilizing additional power to enable a larger tank amplitude, lower noise injection and improved loaded tank Q as compared to traditional cross-coupled VCOs. Also, design optimization of LiT VCOs can be performed in a similar way to that of cross-coupled VCOs. For example, based on G_m curves as shown in Fig. 4, any cross-coupled VCO optimized using the techniques described in [6] can be converted into a LiT VCO design. The target amplitude of oscillation, A_{LiT}, can be maximized to the tolerance limits imposed by the technology. G_m curves can then be constructed for the active device for different combinations of k and n and a global optimum for power, phase noise, tuning range and robustness can be determined.[4]

III. Implementation

The LiT VCO PLL has been implemented in IBM's 32-nm SOI CMOS process. The PLL was implemented for frequency synthesis as part of a potential sliding IF radio architecture as shown in Fig. 8. The required frequency bandwidth of

[4]For example, increasing k linearizes the G_m at the expense of power. Similarly, increasing n lowers the active device noise at the expense of power and start-up margin. Also, k and n are related through (1) and (2).

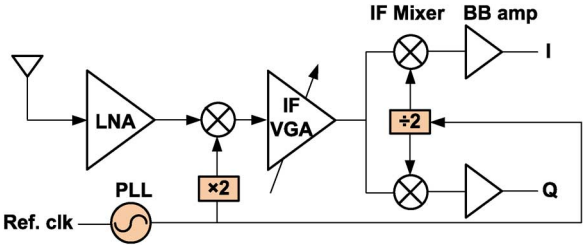

Fig. 8. Potential sliding IF 60-GHz receiver architecture using the LiT VCO PLL.

57–66 GHz is covered by a tuning range of 22.8–26.4 GHz using the 2.5× multiplier scheme as shown.

The PLL architecture, shown in Fig. 9, includes two separate fully differential control paths: an integral path consisting of a charge pump and capacitor and a proportional path consisting of charge pump and resistor (as well as a ripple capacitor). The divider consists of a static prescalar of division ratio of 8 or 16, followed by a fully synchronous divider which can divide from 2 to 128. The PFD consists of a classic tri-state phase detector. The charge pump currents, proportional path resistance, and integral path capacitance value are all made programmable in order to support a wide range of bandwidths and reference frequencies. More details on the PLL can be found in [7]. The LiT VCO design is optimized at $k = 2.2$ and $n = 1.75$ (Fig. 4). C_c, C_d and C_t are selected so as to obtain this k and n combination while adding minimum capacitive load to the tank.

Though this design was implemented in SOI technology, the VCO linearization technique is generally applicable to CMOS and is expected to provide improved performance even in bulk CMOS processes (compared with other topologies).[5]

A. Capacitor Array Design

For the targeted 60-GHz application, a large frequency tuning range (FTR) is a critical requirement [8]. Switched capacitors on the drain and tank are utilized (Fig. 9) to manipulate the feedback ratio and extend G_m linearization (and low phase-noise performance) over a large tuning range. The VCO frequency is less sensitive to capacitance variation on the drain node. As a result, the fine tuning capacitors and varactors are placed across the drain nodes for fine frequency control.

a) Parasitic interconnect inductance: At the high frequencies targeted for this design, achieving a large tuning range (in conjunction with a low $K_{\rm VCO}$) demands implementing a large switched capacitor array in the tank. For optimal phase noise, a small inductor is utilized [6]. Consequently, the capacitor array and the inductor occupy comparable areas (Fig. 10) and the interconnect inductance, especially that associated with connecting the capacitor array, significantly impacts VCO performance.

To mitigate this problem in the LiT VCO, the interconnect parasitics are minimized using a reduced-inductance layout technique. As shown in Fig. 10, the unit capacitors are arranged in a square, reducing the perimeter to area ratio of the structure. The top plates of these MIM capacitors are connected using a mesh to reduce parasitics by parallelization. The bottom-plate interconnects are interleaved into the top plate mesh and carry an opposing current so that the resulting mutual inductance subtracts from the self-inductance of the interconnections as shown in the inset of Fig. 10. Consequently, compared with the 100-pH tank inductor, the interconnects of the 70× 80 μm^2 capacitor array contribute only 12 pH of inductance. By limiting the inductive parasitics, parasitic oscillation modes are eliminated, and a large tuning range of 23% is obtained.

Discrete frequency tuning is achieved using a 3-bit coarse and a 4-bit fine switched capacitor array (Fig. 9). Varactors are used for continuous tuning and provide approximately 100 MHz of analog tuning range, achieving the desired low $K_{\rm VCO}$.

b) High voltage-swing switch: As discussed above, the LiT VCO topology exploits a large oscillation amplitude in order to obtain better phase-noise performance. Since the total voltage swing can be larger than $V_{\rm DD}$, there is a possibility for the switches in the switched capacitor array to turn on even when disabled. As a result, it is necessary to design the FET based switches in the switched capacitor array such that their turn-on, turn-off characteristics do not limit the realizable voltage swing.

To address this issue, an inverter is utilized for biasing, as shown in Fig. 11. This scheme forces the drain–source dc voltage to be low when the switch is *on* and high when the switch is *off* for effective operation. Resistors are used to isolate the nodes in the ac sense. The resistors are sized so that their contribution to the total phase noise is less than 2% and the area overhead of the capacitor array due to the resistors is also less than 2%.

Moreover, a series combination of two switches (2× wider than if one was used) is utilized as conceptually shown in Fig. 11 using nMOS switches.[6] The switches are physically placed between two symmetrical capacitor arrays as shown in Fig. 10. This approach allows the switch gate nodes (node B) to be opens in the small-signal sense and swing partially as shown. Consequently, the gate source voltage ($V_{\rm gs}$) swing is reduced, allowing the switches to remain off when so desired through the entire oscillation cycle as shown in Fig. 11. Notice that, even with the inverter bias, if a single switch approach was utilized, node B would have been at 0 V throughout the oscillation cycle, thereby potentially turning on the switch during the part of the cycle highlighted in the figure.

Also, by allowing node B to be a small signal open, the effective parasitic capacitance resulting from the series combination of the two C_{2X} capacitances of the two 2× switches is approximately equivalent to that of one 1× switch: $(C_{\rm 2X}\cdot C_{\rm 2X})/(C_{\rm 2X}+C_{\rm 2X}) = C_{\rm 2X}/2 \approx C_{\rm 1X}$. Therefore, there is minimal additional loading on the tank due to this technique.

c) Biasing: In the LiT VCO topology, the gate and drain nodes in the FET devices are decoupled from each other. As a result, it is possible to use a voltage-based bias for the LiT VCO, as shown in Fig. 9. Also, as shown in Fig. 9, an inductor is used to resonate (at $2f_0$) the parasitic capacitance at the tail node. The resulting source degeneration at $2f_0$ reduces the G_m cell noise contribution when one transistor is in cut-off. The tail inductor

[5]Note that, due to its lower junction capacitance, an SOI implementation is expected to provide a slightly better tuning range and a slightly lower parasitic capacitance modulation in comparison to bulk CMOS processes for all *LC* VCOs.

[6]nMOS switches are shown in Fig. 11 instead of the implemented pMOS switches for ease of understanding.

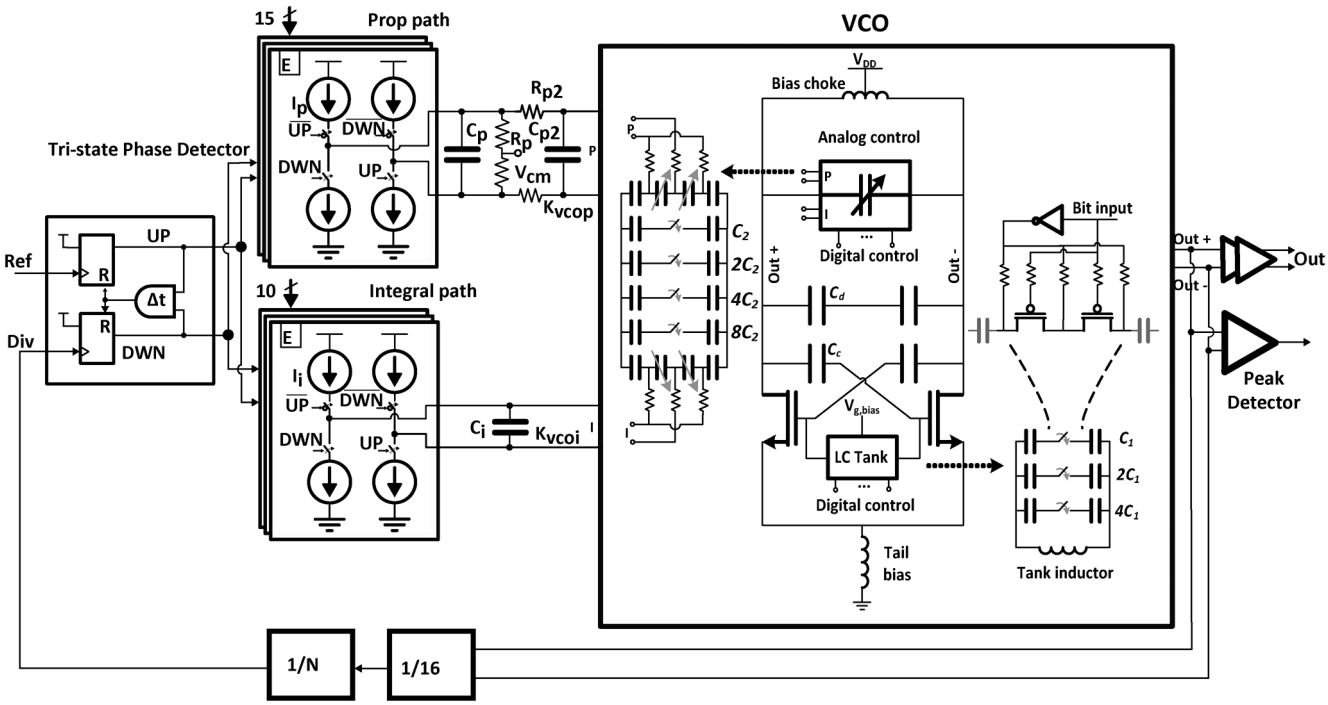

Fig. 9. Block diagram of the PLL showing the detailed VCO schematic including frequency tuning schemes.

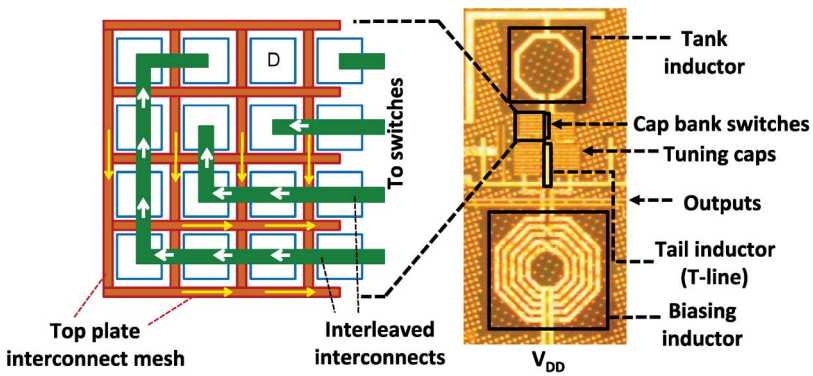

Fig. 10. Die photograph of the LiT VCO showing the capacitor array design details for minimizing interconnect inductance, and other implementation details.

is implemented using a transmission line to retain the symmetry in the overall the LiT VCO layout (see Fig. 10). A DAC digitally controls the VCO gate bias for performance optimization. This bias control also eliminates the tail current source which can normally be a significant source of noise. Also, only a fraction of the noise from the biasing choke (6 nH) (Fig. 9) flows into the tank, reducing the total noise from the biasing circuitry in the LiT VCO as compared to the cross-coupled topology.

IV. Measurement Results

The LiT VCO is implemented in the IBM 32-nm SOI CMOS process. Outputs from an open-drain CML buffer were measured using a 50-Ω system. The measurement setup is shown in Fig. 12.

Measurement results from the PLL are plotted in Figs. 13–20. Fig. 13 shows the phase noise versus frequency offset from a 22.6-GHz carrier with −4.4-dBm output power (single-ended). The differential output power is greater than 0 dBm over the entire frequency tuning range.

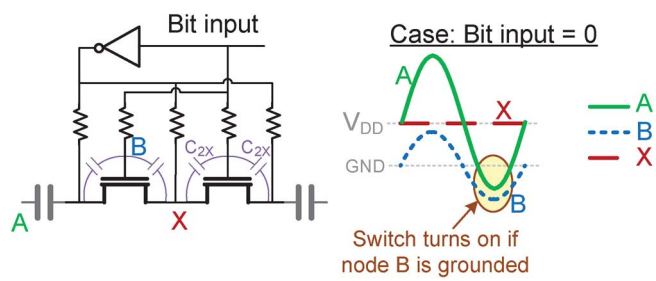

Fig. 11. Proposed switch scheme for the high-amplitude LiT VCO tank switched capacitors.

Fig. 14 shows the measured phase noise at 10 MHz offset over the tuning range for 3 dies at different radii on the wafer. The phase noise of the LiT VCO-based PLL varies from −130 dBc/Hz at 22 GHz to −126 dBc/Hz at 27 GHz. This performance is notably superior to other PLL's for 60 GHz applications (Table I).

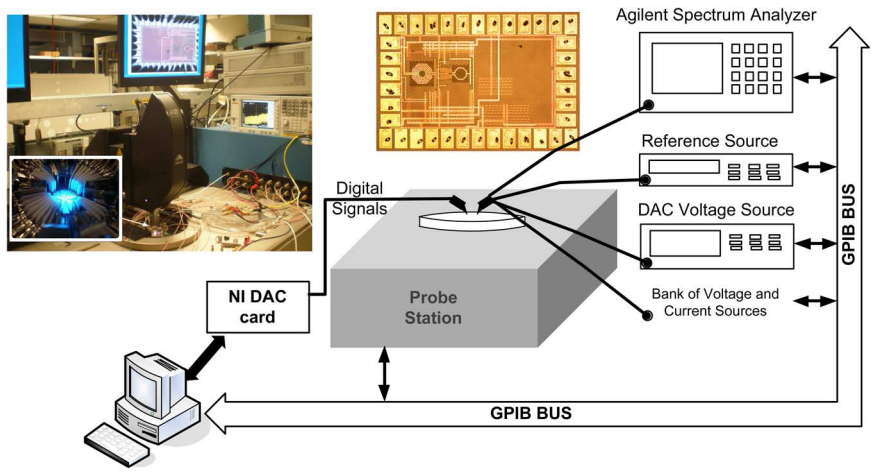

Fig. 12. Measurement setup for testing the LiT VCO PLL.

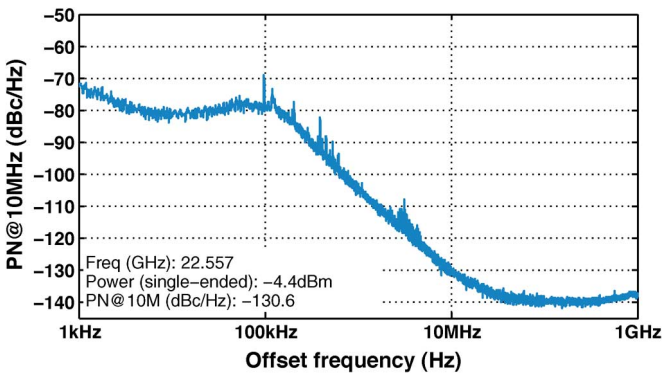

Fig. 13. Phase noise versus frequency offset from a 22-GHz carrier.

The measured tuning range of 21.8–27.5 GHz covers the required range (22.8–26.4 GHz) and is shown in Fig. 15 over all 3-bit coarse tuning combinations. The resulting 23% tuning range makes this a robust solution that is manufacturable in volume.

Die to die phase noise variation for 55 dies on a wafer is shown in Fig. 16. Measurements using 4 (out of 128 possible combinations) equally spaced switched capacitor settings on each die are denoted by 4 different markers. All other settings are kept identical. The measured phase noise variation (at 10-MHz offset) is $\sigma < 0.6$ dB across all dies. The PLL's performance robustness across temperature at three capacitor settings is shown in Fig. 17. The measured phase noise at 10-MHz offset degrades by about 3 dB going from 25 °C to 85 °C across the frequency bands. The center-band frequency drops by about 30 MHz.

The effect of varying $V_{\rm DD}$ and $V_{\rm g,bias}$ on the phase noise is shown in Fig. 18. For low $V_{\rm g,bias}$, the VCO is in the current limited regime. Phase noise (at 10-MHz offset) initially improves with increasing $V_{\rm g,bias}$ until the FET becomes nonlinear as it enters its triode region of operation (particularly for lower $V_{\rm DD}$), after which the phase noise degrades. This demonstrates the effect of triode operation on LiT VCO phase noise. Finally, the PLL's measured phase noise varies by only 2 dB across 800 mV of supply variation (from 0.7 to 1.5 V).

Table I and Fig. 19 compare the LiT VCO PLL performance with that of other PLLs designed for 60 GHz applications. Compared with other designs, the LiT VCO PLL demonstrates the lowest phase noise of −127.3 dBc/Hz at a 10-MHz offset from its center frequency, 24.7 GHz, a large tuning range of 23%, the lowest power consumption of 36 mW and the best $\rm FOM_T$ of 188.6 dBc/Hz. Finally, measured results show the design is robust, consistently maintaining excellent performance.

V. Digitally Assisted Autonomic Biasing

As seen earlier in Fig. 18 of Section IV, the LiT VCO phase noise is sensitive to bias ($V_{\rm g,bias}$) variations. As a result, optimized biasing of this VCO is critical to ensure its superior performance. Fig. 20 shows the phase noise at 10-MHz offset versus varying gate bias ($V_{\rm g,bias}$) for 55 different dies at different frequencies: 22.3, 23.5, 24.8, and 26.4 GHz. From Fig. 20, the following observations can be made.

- The phase noise performance varies across process at each of the frequencies of operation (also observed in Fig. 16).
- There is significant variation in the optimal bias point across frequencies. For example, if the LiT VCO is biased at 0.9 V in order to minimize the phase noise at the higher frequencies (e.g., at 26.4 GHz), the phase noise for this bias at the lower frequencies is far from optimal (≈4 dB worse at 22.3 GHz).
- There is also some die to die variation in optimal bias at each operating frequency (≈1 dB).

These observations suggest that the bias voltage can be optimized at each frequency and for each die to improve performance.

To mitigate the variations in VCO phase noise, automatic amplitude control techniques have been previously presented [9]–[11]. The goal of these control loops is to keep the oscillation amplitude constant across process, temperature, and frequency using an on-chip peak detector. However, as seen from the measured data in Fig. 21, the optimal phase noise is obtained across a wide range of amplitudes. These data are in line with the Leeson's model for phase noise in *LC* oscillators by establishing that the phase noise depends not only on the voltage swing, but also on other factors such as VCO current and oscillation frequency [12]. A few integrated phase noise/jitter sensors

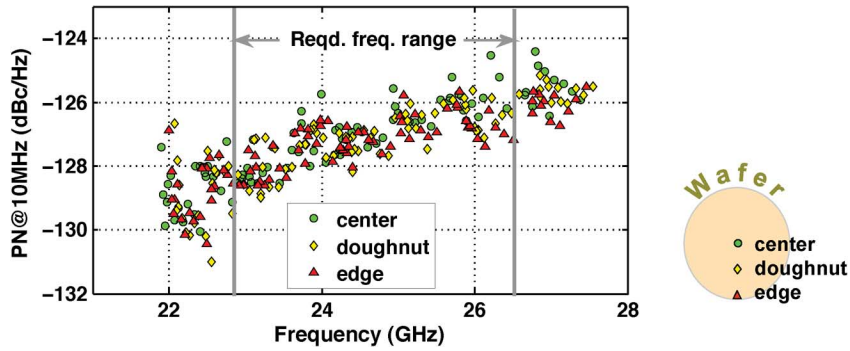

Fig. 14. Phase noise over the tuning range for different die locations on a wafer.

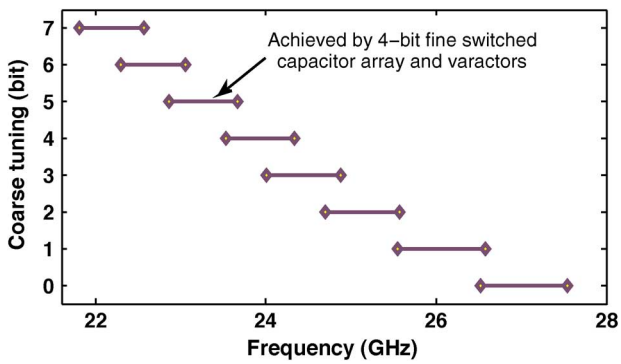

Fig. 15. Coarse frequency tuning showing frequency overlap.

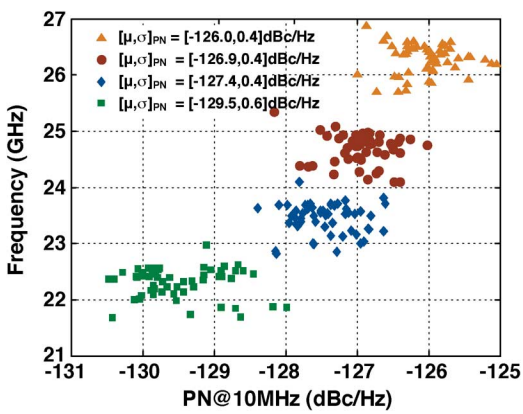

Fig. 16. Robustness of the LiT VCO design to process variations (die to die).

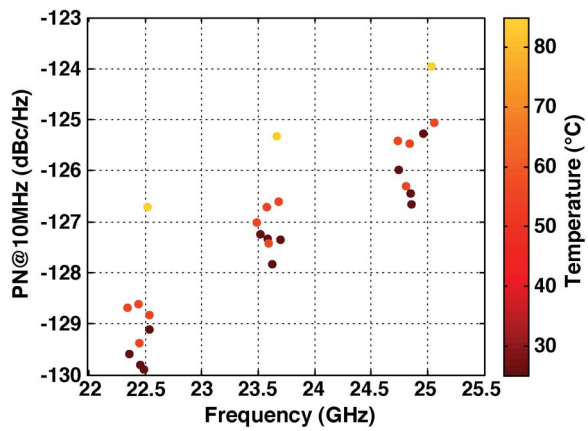

Fig. 17. Robustness of the LiT VCO design to temperature variations.

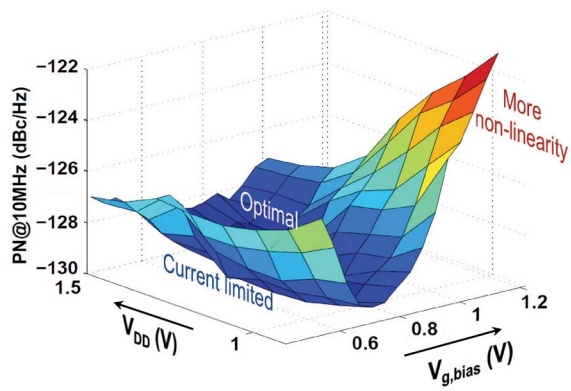

Fig. 18. Robustness of the LiT VCO design to supply variations at 22-GHz center frequency.

for on-chip testing and calibration have been presented in the literature [13], [14]. However, these sensors cannot be used for applications where the noise specification is close to or below the noise floor of the integrated sensor.[7]

Instead of directly measuring the phase noise, it has been proposed in [4] that phase noise can be predicted from other easily measurable parameters using linear regression. Similar methods based on alternate tests have been proposed in the past for other RF circuits [15], [16]. In this work, we implement a digitally assisted autonomic biasing mechanism based on this indirect phase-noise sensing technique which was previously demonstrated using simulation data [4]. In accordance with Leeson's model, we considered oscillation frequency (f_0), VCO current (I), and carrier amplitude (A), all of which are easier to measure using fully integrated subcircuits, as indirect sensor inputs. We also considered the bias tuning knob (t_B) and the frequency tuning knob (k_B). Using these parameters, the indirect sensor model can be expressed as follows:

$$L\{\Delta f\} = f(A, I, f_0, k_B, t_B) \tag{3}$$

[7]For example, the phase-noise sensor in [13] achieves −75-dBc sensitivity at 100-kHz offset from a 2-GHz carrier, corresponding to a sensitivity of −95 dBc at 10-MHz offset from a 20-GHz carrier, which is unusable for the present VCO. Similarly, the jitter sensor in [14] is limited by 1-ps resolution corresponding to −100 dBc/Hz for a 20-GHz VCO assuming a Lorentzian noise profile.

TABLE I
TABLE FOR COMPARISON WITH OTHER PLLS

Ref	Floyd, JSSC 08 [8]	Osorio, et al. ISSCC 11 [2]	Richard, et al. ISSCC 10 [18]	Murphy, et al. JSSC 11 [17]	Scheir, et al. ISSCC 09 [19]	Pellerano, et al. ISSCC 08 [20]	This work
FTR (GHz) (f_{osc}) (GHz)	16.0-18.8 (17.4)	21.7-27.9 (24.8)	17.5-20.9 (19.2)	42.1-53.1 (47.6)	57.0-66.0 (61.5)	39.1-41.6 (40.4)	**21.8-27.5 (24.7)**
PN @10MHz from f_{osc} (dBc/Hz)*	-123.9	-121.0	-126.0 (@21GHz)	-117.5	-95.0	-112.0	**-127.3**
Technology (nm)	130 BiCMOS	45 CMOS	65 CMOS	65 CMOS	45 CMOS	90 CMOS	**32 SOI**
PLL power (mW)	144	40	80	72	78	64	**36‡**
PN @ 10MHz from 24.7GHz (dBc/Hz)†	-120.9	-121.0	-124.6	-123.2	-102.9	-116.3	**-127.3**
VCO tuning range (%)	16.5	25	17.7	23.1	14.6	6.2	**22.9**
VCO FOM_T (dBc/Hz)§	182.8	185.9	___	186.7	___	___	**188.6**

* Calculated assuming 20-dB/decade degradation with offset frequency

† Calculated assuming 20-dB/decade degradation with oscillation frequency

‡ Includes the consumption of the micro-controller and sensors for digital calibration and optimization; the VCO consumes 24 mW

§ $\mathrm{FOM}_T = L(\Delta\omega) - 20 \cdot \log((\omega_0/\Delta\omega) \cdot (\mathrm{FTR}/10)) + 10 \cdot \log(P_{\mathrm{diss}}/1\ \mathrm{mw})$, where P_{diss} is the VCO power dissipation

where $f(\bullet)$ is a polynomial function. This indirect sensor model is obtained by following the methodology in [4] and is evaluated using an on-chip processing unit that includes a fixed-point arithmetic unit, registers to store sensor outputs, and a programmable memory to store model coefficients and instructions. In the following section, we describe the integrated sensor circuitry and the on-chip digital logic used to evaluate the indirect phase noise sensor. In Section V-B, we present how this technique can be applied to autonomic biasing to meet different objectives.

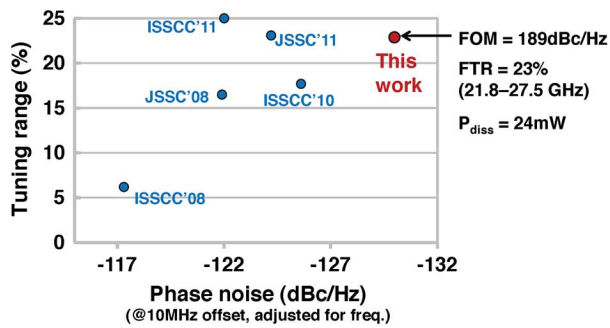

Fig. 19. Phase noise and tuning range comparison with other PLLs for 60-GHz applications.

A. Circuitry for Autonomic Biasing

The entire system for autonomic biasing, except the VCO current sensor, is implemented on-chip with the 32-nm SOI CMOS LiTVCO PLL as shown in Fig. 22. We plan to integrate the VCO current sensor in our future work. The building blocks of this system are described below.

1) *Peak detector*: A peak detector was implemented as shown in Fig. 23 using a differential to single-ended low pass filtered source follower configuration to measure the VCO output amplitude. A dummy peak detector was implemented for offset correction.
2) *ADC*: The outputs of the peak detector (and the dummy replica) are digitized using a 6-bit SAR ADC. The implemented ADC comprises a rail-to-rail comparator, a programmable resistor ladder, and digital circuitry to control the successive approximation algorithm.
3) *Frequency sensor*: A counter-based frequency sensor was implemented as shown in Fig. 24 to count the VCO output cycles using a reference clock. In order to sense the frequency, the ALU resets and starts both counters shown in Fig. 24. The reference counter uses a reference clock (f_{ref}) and counts up to a certain value (N_R) loaded into it by the ALU. As soon as this value is reached, the second counter (counting the divide-by-16 output cycles) is stopped, and its output (N_{out}) is read by the ALU. The VCO frequency is then calculated as $f_{\mathrm{VCO}} = 16 \cdot N_{\mathrm{out}}/N_R f_{\mathrm{ref}}$. The sensor achieves 16-MHz resolution using a 100-MHz clock reference.
4) *DAC*: A 5-bit resistor-based DAC was implemented for VCO bias control. The high and low voltage rails are programmable in order to change the bias actuation range and increase the resolution over a given bias range. The nominal bias voltage resolution used was 40 mV. The DAC was optimized for low power while contributing negligibly to the VCO phase noise.
5) *Arithmetic and logic unit*: The ALU comprises a 16-bit arithmetic and logic unit capable of addition, multiplication, push, pop, shift left, shift right, and compare operations. It features a 32-word data memory to store coefficients and computation by-products and a 256-word instruction memory. This ALU unit allows the calibration of sensor model by scanning in the list of instructions and coefficients after manufacturing.

A die photograph of the full PLL design, including the autonomic controller, is shown in Fig. 25. The entire system occupies a total area (excluding the probe pads) of 0.39 mm^2, where the area overhead due to integrated sensors and other digital circuits required for autonomic biasing is 12.7%. If this design were to be implemented as part of larger system, such as a transceiver, block-level placement, reuse and optimization would further reduce overhead.

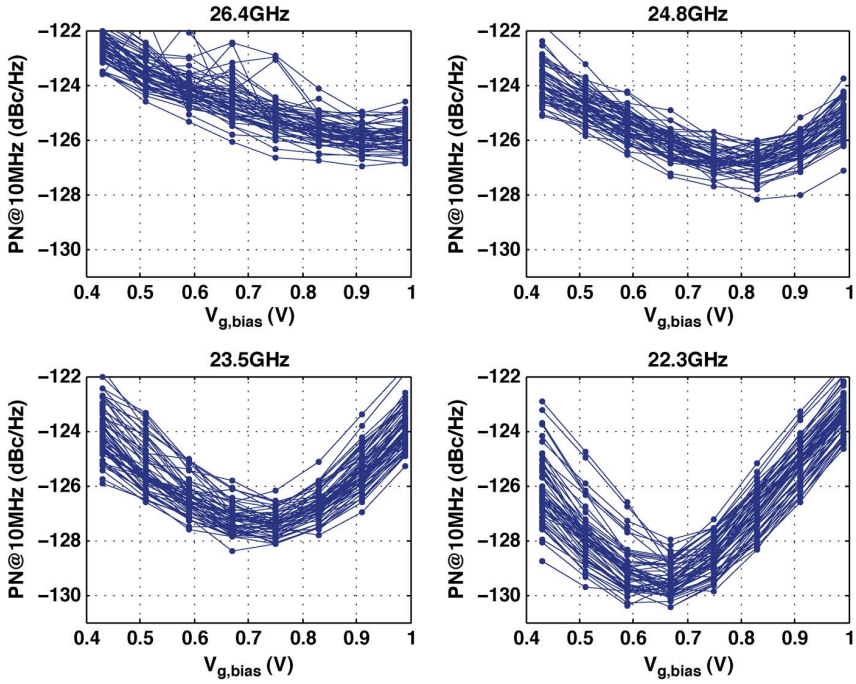

Fig. 20. Variation of optimal bias point with process and frequency.

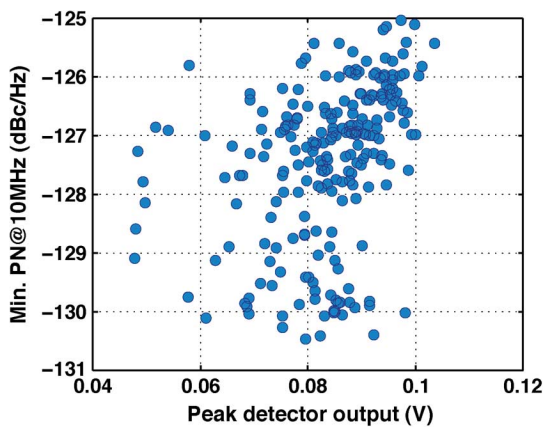

Fig. 21. Measured data showing the wide range of sensed amplitudes at which optimum phase noise is obtained.

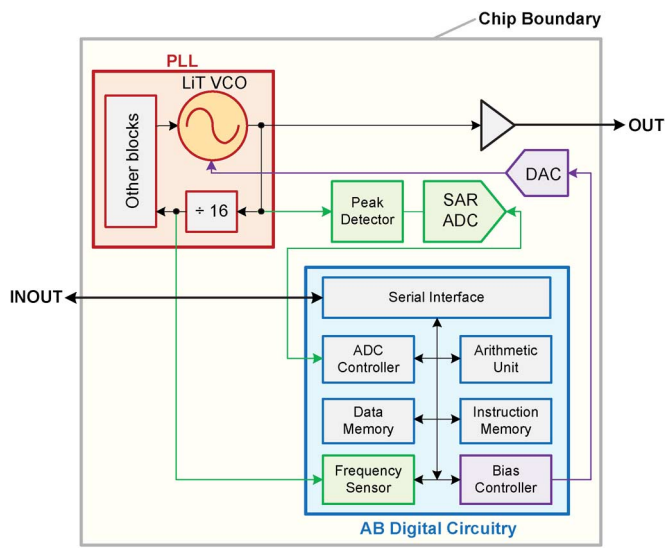

Fig. 22. Integrated system implemented in 32-nm SOI CMOS.

B. Autonomic Biasing Evaluation

Measurements of a subset of the PLLs were used to train the indirect phase noise sensor. The trained sensor was then able to predict the phase noise for the remaining PLLs with an rms error of 0.77 dB, where the coefficient of correlation is 0.92. Using the phase-noise predictor, two different autonomic biasing (AB) algorithms were considered.

1) *AB for minimum noise* selects the bias voltage that provides the lowest phase noise at each frequency for each die. This is achieved by sweeping the bias voltage and evaluating the indirect sensor model on-chip.
2) *AB for minimum power* selects the minimum bias voltage where the phase noise still meets the specification at each frequency for each die. This is an attractive scheme in a practical system implementation (e.g., for the PLL used within a 60-GHz receiver) where the phase noise specification at a given offset does not vary across the different frequency channels in a band.

The parametric yield and power dissipation of these autonomic biasing algorithms were compared against ideal biasing (IB) which employs a hypothetical, ideal phase-noise sensor and, therefore, can determine the true best achievable phase noise and the minimum bias voltage to achieve target phase noise. By parametric yield, we refer to the extent to which the algorithm can achieve a given phase-noise target over all frequency bands. By power dissipation, we mean the average power dissipated across frequency bands.

Fig. 26 presents the measured parametric yield achieved by IB and autonomic biasing for two different objectives for

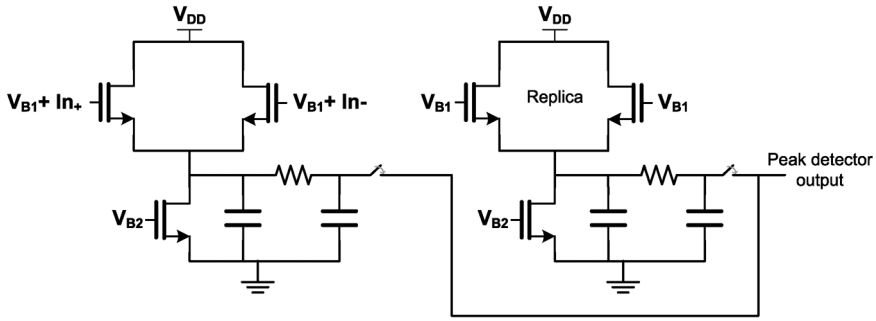

Fig. 23. Peak detector circuit used for sensing the output amplitude.

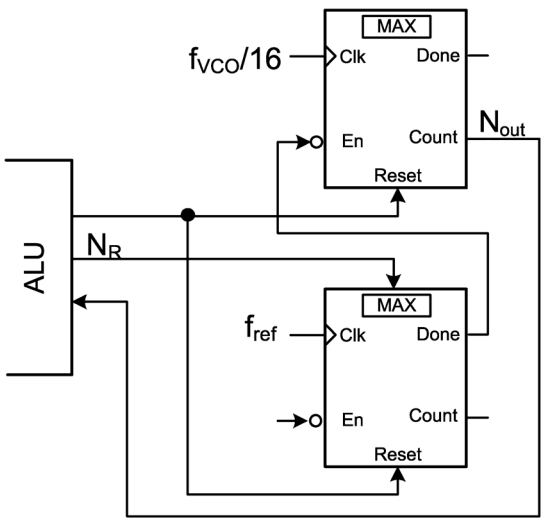

Fig. 24. Counter-based frequency sensor circuit used for sensing the VCO output frequency.

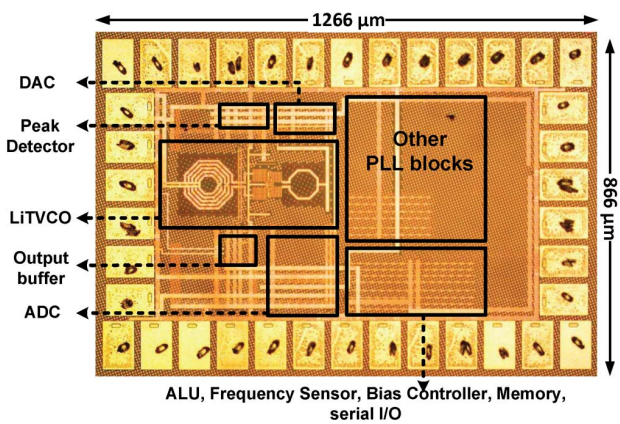

Fig. 25. Annotated die photograph showing the 32-nm SOI implementation of the LiT VCO PLL with the autonomic biasing circuitry.

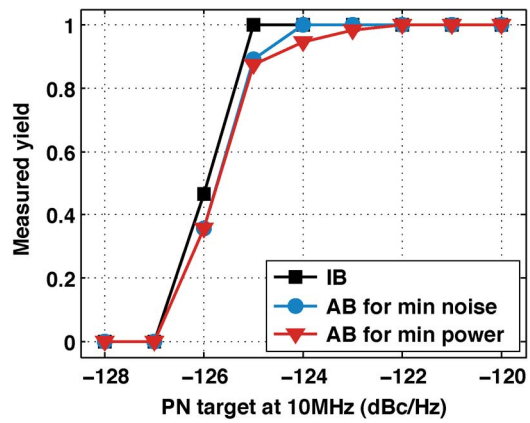

Fig. 26. Comparison of parametric yield achieved by ideal biasing for minimum power, autonomic biasing for minimum noise, and autonomic biasing for minimum power dissipation for varying phase noise target.

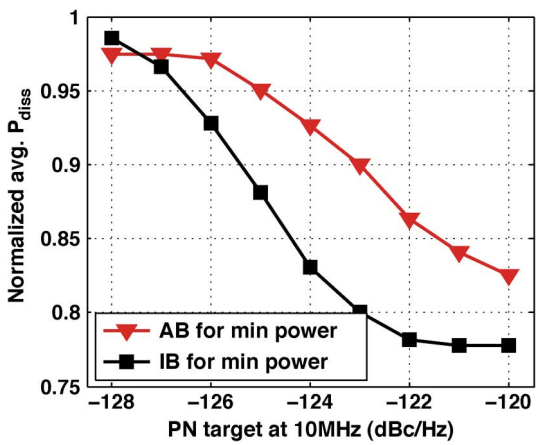

Fig. 27. Comparison of power dissipation achieved by ideal biasing for minimum power and autonomic biasing for minimum power dissipation for varying phase noise target.

varying phase noise targets. As ideal biasing utilizes an ideal phase noise sensor, it achieves the maximum possible yield for either objective. This figure shows that the parametric yield achieved by the realized autonomic biasing infrastructure is very close to the maximum achievable yield (IB). As the phase-noise specification becomes more aggressive, the parametric yield declines sharply for both algorithms, as the phase-noise specification can no longer be achieved for all frequency bands. Fig. 27 presents the normalized average power dissipation of ideal and autonomic biasing to minimize power dissipation for varying phase-noise targets. These results are normalized to the power dissipation of IB for minimum noise. IB for minimum power (square markers) demonstrates a potential of up to 23% reduction in power dissipation. Autonomic biasing for minimum power can exploit this potential by reducing power up to 17%. Overall, autonomic biasing based on indirect phase-noise sensing achieves performance that closely approaches the best achievable performance.

VI. Conclusion

In this paper, a low-phase-noise VCO integrated in a dual-path PLL for 60-GHz applications was presented. A novel G_m linearization technique was used to achieve a larger oscillation amplitude that, along with lower active device noise, resulted in significantly improved phase-noise performance. Additionally, a new capacitor array layout approach was used to reduce interconnect inductance, enabling a large 23% tuning range. A capacitor switch configuration capable of operating under high swing conditions was also described.

A technique for autonomic VCO biasing for performance optimization was demonstrated. The biasing technique is based on indirect performance sensing and uses the predicted behavior to optimize the VCO bias for desired performance.

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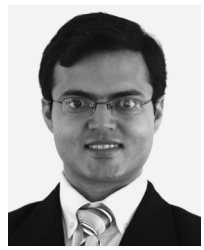


Bodhisatwa Sadhu (S'08–M'12) received the B.E.(Hons.) degree in electrical and electronics engineering from Birla Institute of Technology and Science, Pilani, India, in 2007, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2012. His dissertation focused on wideband circuits and architectures for software-defined radio applications.

He is currently a Post-Doctoral Researcher with IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. In 2007, he was with Broadcom Corporation, Bangalore, India, where he worked on system integration and verification of Ethernet switch SoCs. In fall 2010 and summer 2011, he was with the Mixed Signal Communications IC Design Group, IBM T. J. Watson Research Center, where he worked on the analysis and design of low-phase-noise frequency synthesizers for 60- and 94-GHz applications.

Dr. Sadhu was the recipient of the University of Minnesota Graduate School Fellowship in 2007, the 3M Science and Technology Fellowship in 2009, and the University of Minnesota Doctoral Dissertation Fellowship in 2011.

Mark A. Ferriss received the B.E. degree (first-class honors) in electrical engineering from University College Cork, Cork, Ireland, in 1998, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2008.

From 1998 to 2002, he was with Analog Devices, Limerick, Ireland, during which time he worked on digital-to-analog converters, switches, controllers, and phase-locked loops for fiber optic communications. In 2009, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA. His present research interests include self-healing RF communication circuits, analog-to-digital interface circuits, and digital phase-locked loops.

Arun S. Natarajan received the B.Tech. degree from the Indian Institute of Technology, Madras, India, in 2001, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2007, respectively, all in electrical engineering.

From 2007 to 2012, he was a Research Staff Member with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, and worked on millimeter-wave (mm-wave) phased arrays for multi-Gb/s data links and airborne radar and on self-healing circuits for increased yield in submicron process technologies. In 2012, he joined Oregon State University, Corvallis, OR, USA, as an Assistant Professor with the School of Electrical Engineering and Computer Science. His current research is focused on RF, mm-wave and sub-mm-wave integrated circuits and systems for high-speed wireless communication and imaging.

Dr. Natarajan was the recipient of the National Talent Search Scholarship from the Government of India [1995–2000], the Caltech Atwood Fellowship in 2001, the Analog Devices Outstanding Student IC Designer Award in 2004, and the IBM Research Fellowship in 2005, and serves on the Technical Program Committee of the IEEE Radio-Frequency Integrated Circuits Conference, IEEE Compound Semiconductor IC Symposium, and the 2013 IEEE International Microwave Symposium.

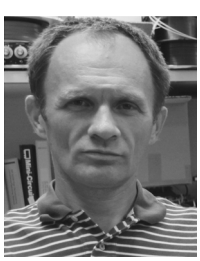
Soner Yaldiz (S'04–M'13) received the B.S. degree in microelectronics engineering from Sabanci University, Istanbul, Turkey, in 2004, the M.S. degree in electrical and computer engineering from Koc University, Istanbul, Turkey, in 2006, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2012. His thesis was on energy optimization for multicore systems using stochastic workload models. His dissertation focused on design methodologies for self-healing analog integrated circuits.

He has interned with Nvidia and IBM T. J. Watson Research Center. He is currently with Intel Corporation, OR, working on analog circuit design methodologies.

Jean-Olivier Plouchart (M'96–SM'06) received the Ph.D. degree in electronics from Paris VI University, Paris, France, in 1994.

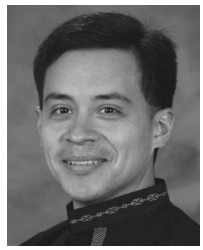
From 1989 to 1996, he was with Alcatel, France Telecom, and the University of Michigan, working on HBT and MESFET MMICs for communication applications. In 1996, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, as a Research Staff Member, where his work involved the design of SiGe BiCMOS and CMOS RFIC circuits for wireless LAN applications, as well as RF product designs for Motorola. In 2000, he led a team working on low-power high-performance SOI SoC technology and enablement, leading to the first demonstration of 130- and 90-nm SOI ASIC, and RF SOI circuits on high-resistivity substrate, as well as the enablement of the first 3.5-W 1-GHz Pentium class microprocessor. He also pioneered the design of millimeter-wave SOI CMOS from 30 to 94 GHz in standard microprocessor technology. Currently, he leads the development of nanometer high-speed circuit design and high-yield nanometer design at the IBM T. J. Watson Research Center. He holds 16 U.S. patents and has authored and coauthored over 84 publications and one book chapter. His research interests include solid-state technologies, the integration of RF transceivers, VCO, PLL and analog-to-digital converters with microprocessors for SoC applications, the RF to millimeter-wave measurement automation, and the Design For Yield in nanometer technologies.

Dr. Plouchart is a coauthor of the Best Student Paper Award at the 2002 IEEE Radio Frequency Integrated Circuit Conference. He served as the Chairman of the IEEE CSICS CMOS committee in 2009 and currently serves as a member of the AMS ITRS roadmap as well as the SRC AMS Technical Advisory Board.



Alexander V. Rylyakov received the M.S. degree from the Moscow Institute of Physics and Technology, Moscow, Russia, in 1989, and the Ph.D. degree from the State University of New York, Stony Brook, NY, USA, in 1997, both in physics.

From 1994 to 1999, he was with the Department of Physics, State University of New York, Stony Brook, NY, USA, where he was involved with the design and testing of integrated circuits based on Josephson junctions. In 1999, he joined IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, as a research staff member. His main current research interests are in the areas of digital phase-locked loops and integrated circuits for wireline and optical communication.



Alberto Valdes-Garcia received the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2006.

He joined IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, as a Research Staff Member. His present research work is on silicon-integrated millimeter-wave systems and carbon electronics. Since 2009 he serves as Technical Advisory Board member with Semiconductor Research Corporation (SRC), where he served as Chair of the Integrated Circuits and Systems Sciences Coordinating Committee in 2011 and 2012. Since 2013, he has also been an Adjunct Assistant Professor with Columbia University, New York, NY, USA. He holds six U.S. patents with more than 20 pending. He has authored and coauthored over 60 publications which have already received more than 950 independent citations in indexed journals. He is a coeditor of the book *60 GHz technology for Gbps WLAN and WPAN: From Theory to Practice* (Wiley, 20011).

Dr. Valdes-Garcia was the recipient of the 2005 Best Doctoral Thesis Award presented by the IEEE Test Technology Technical Council (TTTC) and the 2007 National Youth Award for Outstanding Academic Achievements, presented by the President of Mexico, and a corecipient of the 2010 George Smith Award presented by the IEEE Electron Devices Society. Within IBM, he has been a corecipient of two Research Division Awards (2012), an IBM Corporate Outstanding Innovation Award for the demonstration of wireless high definition video links with 60 GHz SiGe radios (2008), and the 2009 Pat Goldberg Memorial Award to the best paper in computer science, electrical engineering, and mathematics published by IBM Research for the work Operation of Graphene Transistors at GHz Frequencies. From 2006 to 2009, he served on the IEEE 802.15.3c 60 GHz standardization committee and from 2010 to 2012 in the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC). He served as guest editor for *IEEE Design & Test* in 2012.

Benjamin D. Parker received the B.S. degree from Bowdoin College, Brunswick, ME, USA, in 1979, and the M.S. degree from Brown University, Providence, RI, USA, in 1981, both in physics.

His graduate work dealt with the optical properties of adsorbed layers on metal surfaces. In 1986, he joined the GaAs group at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he worked on characterization of III–V semiconductors. In 1991, he joined the Mixed-Signal Communications IC Design Group, working on design and verification of digital circuits in high-speed serial communications.

Aydin Babakhani received the B.S. degree from Sharif University of Technology in 2003, and the M.S. and Ph.D. degrees from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2005 and 2008, respectively, all in electrical engineering.

He was a Postdoctoral Scholar with Caltech in 2009, and a Research Scientist with IBM T. J. Watson Research Center in 2010. In 2011, he joined Rice University, TX, USA, as an Assistant Professor with the Electrical and Computer Engineering Department. He is the Director of Rice Integrated Systems and Circuits (RISC) Laboratory. His current research is focused on RF, millimeter-wave (mm-wave), and sub-mm-wave radiating integrated circuits for wireless communication, radar, and medical imaging.

Dr. Babakhani was the recipient the Caltech Electrical Engineering Department's Charles Wilts Best Ph.D. Thesis Prize for his work on Near-Field Direct Antenna Modulation (NFDAM). From 2006 to 2008, he was the Vice Chair of the IEEE Microwave Theory and Techniques Society (MTT-S) Metro LA/SFV Joint Sections MTT-S Chapter 17.1. He was the recipient of the Microwave Graduate Fellowship in 2007, the Grand Prize in the Stanford-Berkeley-Caltech Innovators Challenge in 2006, Analog Devices Inc. Outstanding Student Designer Award in 2005, as well as the Caltech Special Institute Fellowship and Atwood Fellowship in 2003. He was also the Gold Medal winner of the National Physics Competition in 1998, and the Gold Medal winner of the 30th International Physics Olympiad in 1999, in Padova, Italy.

Scott Reynolds received the Ph.D. degree in electrical engineering from Stanford, Stanford, CA, USA, in 1987.

While at Stanford, he was a Fellow of the Office of Naval Research. He joined IBM in 1988 and has worked on a wide variety of IBM products, including ICs for disk drive channels, electrical and optical I/O, and RF communication. He has recently been engaged in development of silicon millimeter-wave ICs and packaging for high-data-rate wireless links and other applications. He holds more than 40 U. S. patents and was named an IBM Master Inventor in 2008. He has authored and coauthored many technical publications. He is currently a Research Staff Member and manages the RF Circuits & Systems Group, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA.

Dr. Reynolds was the recipient of the Best Paper Award at the International Solid State Circuits Conference in 2004 and 2006.

Xin Li (S'01–M'06–SM'10) received the B.S. and M.S. degrees in electronics engineering from Fudan University, Shanghai, China, in 1998 and 2001, respectively, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2005.

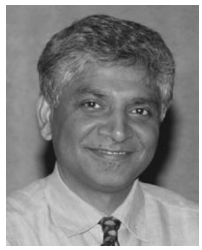
He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, USA. In 2005, he cofounded Xigmix Inc. to commercialize his doctoral research and served as the Chief Technical Officer until the company was acquired by Extreme DA in 2007. In 2011, Extreme DA was further acquired by Synopsis. His research interests include computer-aided design, neural signal processing, and power system analysis and design.

Dr. Xin Li has served as an associate editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS since 2012 and an associate editor of the *Journal of Low Power Electronics* since 2011. He served on the Technical Program Committee of Design Automation Conference (DAC) from 2011 to 2012, the Technical Program Committee of International Conference on Computer-Aided Design from 2008 to 2011, the Technical Program Committee of International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems from 2010 to 2012, the Technical Program Committee of International Conference on VLSI Design in 2009, and the IEEE Outstanding Young Author Award Selection Committee in 2006. He received the National Science Foundation Faculty Early Career Development Award in 2012, a Best Paper Award from DAC in 2010, and two IEEE/ACM William J. McCalla ICCAD Best Paper Awards in 2004 and 2011.

Larry Pileggi (F'02) received the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1989.

He is the Tanoto Professor of electrical and computer engineering with Carnegie Mellon University, Pittsburgh, PA, USA, and has previously held positions at Westinghouse Research and Development and the University of Texas at Austin. He has authored and coauthored over 250 conference and journal papers and holds 30 U.S. patents. His research interests include various aspects of digital and analog integrated circuit design and design methodologies.

Prof. Pileggi has been the recipient of various awards, including the SRC Aristotle award in 2008, the 2010 IEEE Circuits and Systems Society Mac Van Valkenburg Award, and the ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation in 2011.



Ramesh Harjani (S'87–M'89–SM'00–F05) received the B.S. degree from the Birla Institute of Technology and Science, Pilani, India, in 1982, the M.S. degree from the Indian Institute of Technology, New Delhi, India, in 1984, and the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, USA, in 1989, all in electrical engineering.

He is the Edgar F. Johnson Professor with the Department of Electrical and Computer Engineering at the University of Minnesota. Prior to joining the University of Minnesota, Minneapolis, MN, USA, he was with Mentor Graphics Corporation, San Jose, CA, USA. He cofounded Bermai, Inc., a startup company developing CMOS chips for wireless multimedia applications in 2001. He has been a Visiting Professor with Lucent Bell Labs, Allentown, PA, USA, and the Army Research Labs, Adelphi, MD, USA. He is an author/editor of four books. His research interests include analog/RF circuits for wired and wireless communications.

Dr. Harjani was the recipient of the National Science Foundation Research Initiation Award in 1991 and Best Paper Awards at the 1987 IEEE/ACM Design Automation Conference, the 1989 International Conference on Computer-Aided Design, the 1998 GOMAC and the 2007, 2010, and 2012 TECHCONs. His research group was the winner of the SRC Copper Design Challenge in 2000 and the winner of the SRC SiGe challenge in 2003. He served as an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART II: EXPRESS BRIEFS from 1995 to 1997, guest editors for the *International Journal of High-Speed Electronics and Systems* and for *Analog Integrated Circuits and Signal Processing* in 2004, and a guest editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2009 to 2011. He is currently a senior editor for the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (2011-2013) and the Technical Program Chair for the IEEE Custom Integrated Circuits Conference. He was the Chair of the IEEE Circuits and Systems Society technical committee on Analog Signal Processing from 1999 to 2000 and a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2001–2002.

José A. Tierno received the Engineering degree from the Universidad de la República, Montevideo, Uruguay, in 1988, and the M.S. degree in electrical engineering and Ph.D. degree in computer science from the California Institute of Technology, Pasadena, CA, USA, in 1989 and 1995, respectively.

From 1995 to 2012, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he was involved with digital circuits for communications. Since 2012, he has been with Apple Inc., Cupertino, CA, USA, as a Research Scientist. His main areas of interest are self-timed digital circuits and digital replacement of analog circuits.

Daniel Friedman (S'91–M'92) received the Ph.D. degree in engineering science from Harvard University, Cambridge, MA, USA in 1992.

After completing consulting work with MIT Lincoln Labs and postdoctoral work with Harvard University in image sensor design, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, in 1994. His initial work at IBM was the design of analog circuits and air interface protocols for field-powered RFID tags. In 1999, he joined the mixed-signal communications IC design group and turned his attention to analog circuit design for high-speed serializer/deserializer macros. He managed the mixed-signal team from 2000 to 2009, focusing efforts on serial data communication and clock synthesis applications. In 2009, he became Manager of the communication circuits and systems group, adding responsibility for teams in millimeter-wave wireless and digital communications IC design. He has authored or coauthored more than 40 technical papers in circuit topics including serial links, PLLs, RFID, and imagers. He holds more than 50 U.S. patents. His current research interests include high-speed I/O design, PLL design, and circuit/system approaches to enabling new computing paradigms.

Dr. Friedman was a corecipient of the Beatrice Winner Award for Editorial Excellence at the 2009 ISSCC and the 2009 JSSC Best Paper Award given in 2011. He has been a member of the ISSCC international technical program committee since 2008, and he has served as the Wireline sub-committee chair from ISSCC12 to the present.