Wireless Synchronization and Spatial Combining of Widely-Spaced mm-wave Arrays in 65nm CMOS

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***Abstract*—This paper presents the first wireless synchronization of a mm-wave array, eliminating the need for connecting wires between the array elements. Wireless injection locking of a single chip is successfully demonstrated and a frequency stability of 400Hz at a carrier frequency of 50GHz is achieved (stability of 8ppb). In addition, spatial power combining of two widely-spaced chips is demonstrated with frequency stability of 6kHz. The reported transceiver includes a receiving on-chip antenna, an LNA, an injection-locked VCO, a buffer amplifier, an I/Q generator, a phase-shifter, a power amplifier, and a transmitting on-chip antenna. The chip is fabricated in a 65nm CMOS process and occupies an area of 1.7mm × 3.8mm. This work sets the foundation for increasing the element spacing of an array through wireless injection locking, extending traditional array systems into the high-resolution, narrow-beamwidth regime.**

***Index Terms*—Wireless synchronization, injection locking, spatial coherent combining, on-chip antennas, mm-wave, silicon, CMOS.**

I. Introduction

CMOS-based mm-wave transceivers have received great attention in recent years. The promise of integrating mm-wave transceivers with commercial electronics opens up opportunities in wireless communication, automotive, medical, and security industries, to name a few. Prior research [1]–[6] demonstrated successful functionality of integrated mm-wave transceivers. Unfortunately, due to the lack of a locking mechanism, these transmitters were limited to single-chip operation without reaping the potential benefits of a coherent multi-chip system with widely-spaced elements. The advantages of a coherent multi-chip system with widely-spaced elements include increased transmission power, narrower beamwidth and larger aperture size. The increased transmission power extends the maximum detectable range in imaging radars, while narrower beamwidth and larger aperture size increase the angular resolution in imaging radars and enhance the security of the link in communication networks. Fig. 1 and 2 illustrate the concept of the various array configurations and their corresponding beamwidth.

In order to achieve coherency in a multi-chip system, traditional transmitters employ locking through a wired connection, either in the form of a phase-locked loop [7] [8] for continuous-wave systems, or a digital square-wave trigger signal for pulsed systems [9] [10]. Unfortunately, the wired connections limit the scalability of the array and are not suitable for building synchronous arrays via mobile objects such as satellites, UAVs, or airborne systems. A wireless locking architecture can resolve this issue. In [11], an optical signal generated by a free-space laser locks the on-chip oscillator. However, the narrow beamwidth of the laser limits the operation angle and requires high-precision alignment, making it unsuitable for low-cost, mobile applications. In contrast, mm-wave wireless locking exhibits wider operation angle. In [12], the authors demonstrated the possibility of generating a 1.875GHz local clock signal using a 15GHz wireless signal. However, the range of operation was limited to a few centimeters, and no radiation or spatial combining was performed.

This paper presents the complete theory, simulation and measurement of a mm-wave transceiver with wireless locking. In this work, single-chip wireless synchronization with frequency stability of 400Hz as well as spatial power combining of two widely-spaced chips with frequency stability of 6kHz are demonstrated. The undesired TX-RX feedback is mitigated using orthogonal antenna polarization and orthogonal radiation

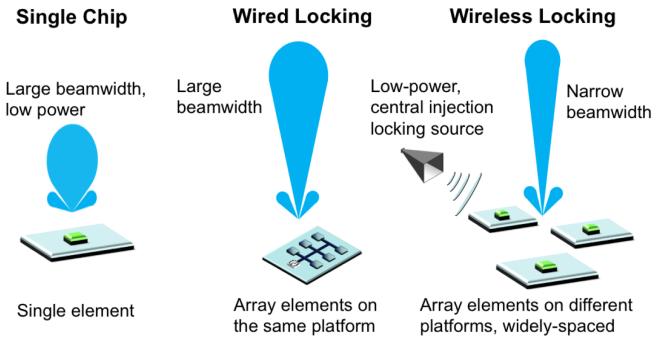

Fig. 1. Mm-wave arrays configured as single chip, multi-chip wired locking, and multi-chip wireless locking.

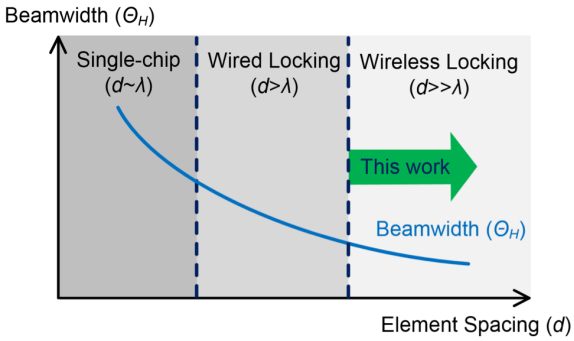

Fig. 2. Beamwidth vs. element spacing. A wireless locking system enjoys narrower beamwidth due to the widely-spaced array elements.

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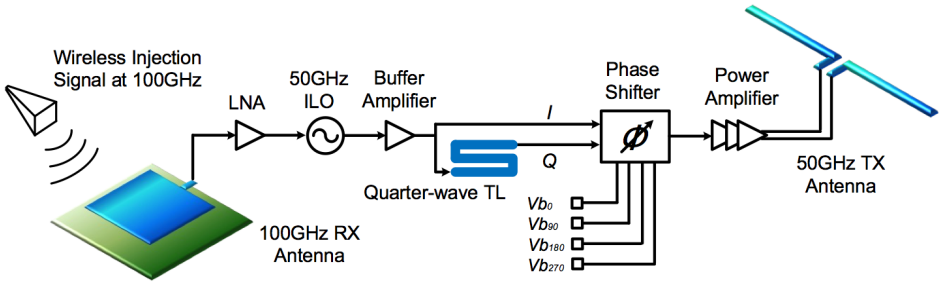

Fig. 3. Proposed transceiver architecture.

efficiency. The proposed system enables scaling of the size of an array by eliminating the need for wires to connect the injection source to the widely-spaced chips. As shown in Fig. 2, this work sets the foundation for increasing the element spacing of an array through wireless injection locking, extending traditional array systems into the high resolution, narrow-beamwidth regime. In addition, the proposed methodology can be used to build an array on a non-planar substrate or on a mobile platform.

This paper is organized as follows: Section II describes the concept of widely-spaced arrays and the proposed system architecture; section III presents the circuit design details; section IV shows the measurement results of both single-chip and multi-chip synchronization and provides a discussion of the results.

II. System Architecture

A. Concept of Widely-Spaced Arrays

The importance of element spacing is understood through the expression for beamwidth. For a large, broadside array system, the half-power beamwidth θ_H, in radians, can be approximated by the following formula [14]:

$$\theta_H \approx \frac{\lambda}{\pi d}\left(\frac{2.782}{N}\right) \tag{1}$$

where N is the number of array elements, d is the spacing between array elements and λ is the wavelength at the frequency of operation. From this equation, it is evident that the beamwidth is inversely proportional to the array size ($N\times d$). Wireless injection locking removes the area limitation of a single die by coherently locking the widely-spaced elements in a multi-chip system, making it possible to reduce the beamwidth of an array. In general, the resolution of an imaging array is equal to the half-power beamwidth of the antenna pattern [15] [16]. In reality, the resolution may be limited by the finite grating lobe rejection levels, which can be mitigated by methods such as adopting highly directive antennas or forming Chebyshev (equiripple) or binomial arrays (no sidelobes) [17]. The proposed system provides the required amplitude and phase control in these arrays through tuning the biases of the power amplifier and the phase shifter, respectively.

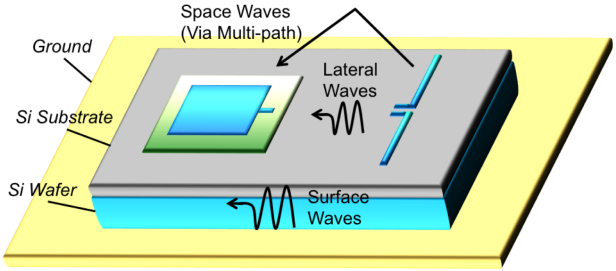

Fig. 4. Illustration of undesired feedback via lateral, surface, and space waves. This effect is mitigated through designing antennas with orthogonal polarization and radiation efficiency.

B. Architecture of Wireless Locking Transceiver

The transceiver architecture is shown in Fig. 3. It consists of a patch antenna that receives the wireless injection signal, a dipole antenna at the output that radiates the locked mm-wave signal, a four-stage power amplifier, a phase shifter, buffer amplifiers, and an injection-locked voltage-controlled oscillator (IL-VCO). The integration of IL-VCO and phase shifter allows for frequency and phase offset adjustment between array elements, respectively. In this design, a low-power 100GHz signal is used as the central injection source. The injected signal is first received by the on-chip patch antenna, amplified by the LNA, and then injected at the current source of a divider to produce a 50GHz reference signal. To compensate for the loss of the quadrature generator, the output of the IL-VCO is amplified by 12.5dB before being passing through the phase-shifter. Finally, the output of the phase shifter is amplified by the on-chip PA to 11dBm and radiated through the on-chip dipole antenna.

III. Antenna and Circuit Design

A. Orthogonal Antenna Design for the Elimination of Self-Oscillation

Traditional mm-wave transmitters utilize a silicon lens to collect and radiate the surface wave power [4] [9] [10] [18]. This significantly increases the cost and the complexity of the system. In this design, we achieve high radiation efficiency by selecting an optimal substrate thickness for a grounded microstrip antenna. At extremely thin substrates ($<<\lambda_0/10$), the radiation efficiency of a microstrip antenna is very low due to the high conductor loss [19]. It is therefore desirable to

increase the substrate thickness to be comparable to the wavelength. When the substrate thickness is $> \lambda_0/10$, the radiation efficiency becomes dominated by the surface wave power. According to the analysis in [20], The TM surface waves are in phase with the space waves and add constructively to the total radiated power, while the TE surface waves are out-of-phase and reduce the total radiated power. Since the TM_0 mode has a cutoff frequency at 0 Hz, the radiation efficiency increases as the substrate thickness increases until it reaches the optimum, which corresponds to the cutoff frequency of the TE_0 mode. In this design, 2.5D EM simulations using IE3D is used to find the optimal thickness. As shown in Fig. 5, the optimal thickness is 430 μm, which is equal to approximately 0.07 wavelengths in air. A dipole antenna is selected as the radiating element due to its small form factor. The length of the dipole is 900μm, which is equal to approximately 0.15 wavelengths in air at 50GHz.

As illustrated in Fig. 4, a wireless injection locking system suffers from multi-path and direct feedback from the TX to the RX antenna. Multi-path feedback is caused by space wave radiation while direct feedback is caused by lateral and surface wave coupling. If the feedback is strong enough, the receiver locks to its own transmitter instead of the external synchronization signal, resulting in an unstable system or injection pulling [21]. A simplistic design in which the TX and RX antennas are identical would lead to maximum feedback. We address this issue by designing the RX antenna to be orthogonal to the TX antenna in both radiation efficiency and polarization. This is achieved by designing the patch RX antenna with an M1 ground plane to change its effective substrate thickness to 8μm. In order to find the optimal patch length, we invoke Hammerstads formula [22] that states that the frequency of a resonant patch antenna with length L operating in the dominant TM_{10} mode is given by:

$$f_{10} = \frac{c}{\sqrt{\epsilon_r}} \frac{1}{2\,(L + \Delta L)} \tag{2}$$

where c is the speed of light, ϵ_r is the permittivity of silicon and ΔL is the length accounting for the fringing effect. In this design ΔL can be ignored due to the extremely thin effective substrate, and L is chosen to be 750μm to receive efficiently at 100GHz. Fig. 6 shows the simulated impedance of the patch of 57Ω at 100GHz. As shown in Fig. 7, the TX antenna transmits efficiently at odd harmonics of 50GHz while the RX antenna receives efficiently at even harmonics, achieving orthogonality and minimum space wave coupling. Furthermore, since the E-field of the receiver patch antenna is in the direction of the feed line and perpendicular to that of the transmitter dipole, as shown in Fig. 8, lateral and surface wave couplings are significantly reduced. Based on the numerical simulation results reported in Fig. 8, it is shown that by using a receiving patch antenna instead of a dipole, the isolation is improved by 60dB at 100GHz. The proposed TX and RX antenna design reduces surface wave, lateral wave and space wave coupling and therefore minimizes injection pulling and ensures the stability of the system.

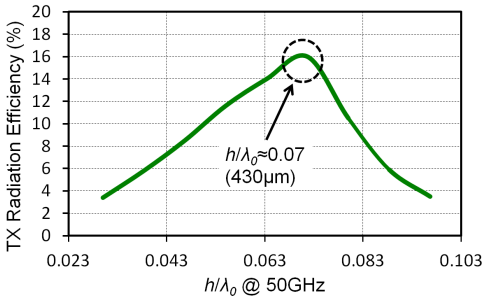

Fig. 5. Transmitting dipole antenna radiation efficiency vs. h/λ_0. The optimal thickness, as derived in [20], is approximately $0.07\lambda_0$, or $430\mu m$.

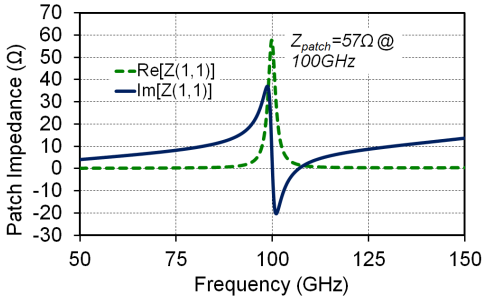

Fig. 6. Simulated impedance of the receiving patch antenna tuned at 100GHz.

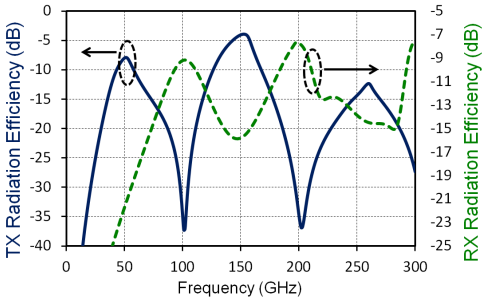

Fig. 7. Simulated radiation efficiencies of the TX dipole (solid) and the RX patch antennas (dashed). The TX peaks correspond to the RX valleys and vice versa, resulting in efficiency orthogonality.

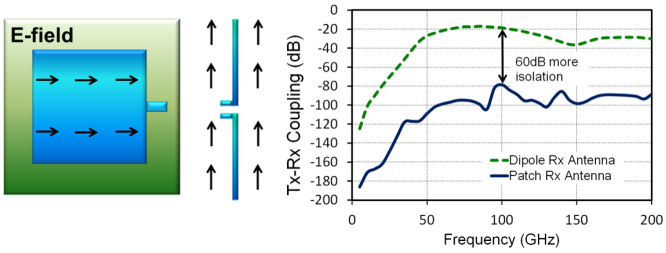

Fig. 8. Reducing the TX-RX coupling by using antennas that are orthogonal in polarization.

B. IL-VCO and LNA

Due to process, temperature, and voltage (PVT) variations, each chip will have slightly different free-running oscillation frequencies. Incorporating IL-VCOs can compensate for this difference, enabling coherent power combining. The schematics of the IL-VCO and the LNA are shown in Fig. 9. The IL-VCO utilizes a cross-coupled negative conductance topology

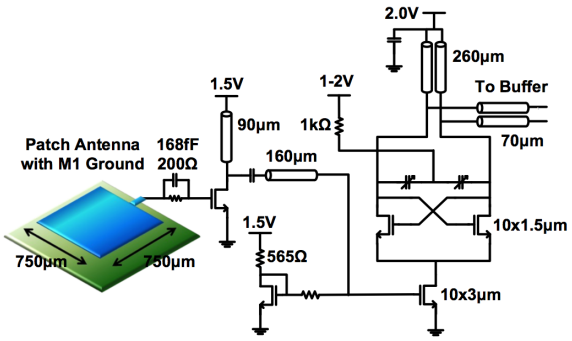

Fig. 9. Simplified schematic of the injection-locked receiver. The patch antenna uses an M1 ground to form efficiency orthogonality.

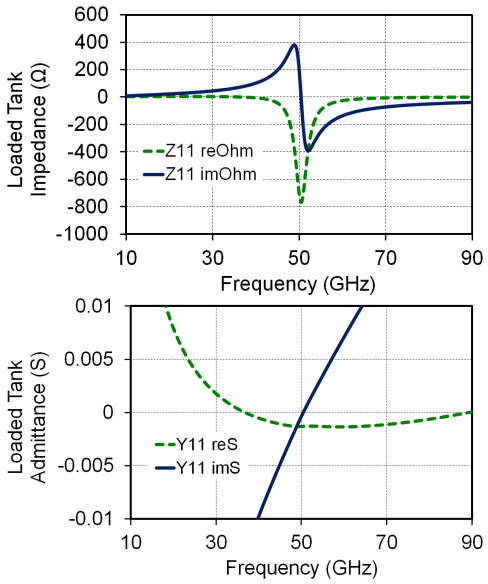

Fig. 10. VCO loaded small-signal tank impedance and admittance. The negative loaded conductance and zero susceptance at 50GHz ensure successful oscillator start-up.

with a tail current source, from which the wireless signal is injected. The IL-VCO operates from 51.3 to 52.1GHz. The width of each transistor is 15μm with 1μm per finger width. The varactors are implemented by thin-oxide MOS devices that provide an approximate capacitance of 22fF. The bias can be varied from 1V to 2V while the corresponding quality factor varies from 7 to 2. Higher tank Q provides higher output power while lower tank Q increases the locking range. Due to the low quality factor of the MOS varactor at this frequency, the matching network of the subsequent buffer stage is designed to keep the real part of the tank impedance high enough so oscillation can start. Fig. 10 shows the small-signal loaded tank admittance $Y_{tank} = -0.8mS\,(or Z_{tank} = -750\Omega)$ at 50GHz. The negative conductance and the zero susceptance ensure successful oscillation start-up at 50GHz until the nonlinearity of the large-signal Gm limits the oscillation amplitude. The IL-VCO delivers -3.5dBm power to the buffer load. To prevent an undesired common-mode oscillation, a 1kΩ resistor is placed in series with the frequency-tuning node to reduce the common-mode gain.

A single-ended LNA is conjugate-matched using stub transmission lines. It amplifies the 100GHz wireless signal by 2.3dB and injects the signal at the current source of the VCO. A resistor is included in the path of the current mirror to form a high impedance path such that the injected power is directed towards the VCO. In order to ensure stability, a parallel RC-network is used in the signal path. This topology acts as a high-pass filter such that the lower frequency signals around the GHz range are attenuated. The simulated noise figure, gain, and linearity are shown in Fig. 11. As can be seen from the graphs, the noise figure at 100GHz is 6.3dB, and the 1-dB compression point is 6.5dBm.

C. I/Q Generator and Phase Shifter

In an injection-locked oscillator, there is a phase difference between the injection signal and the free-running oscillator [21]. In general, the phase of free-running oscillators are random as it is determined by noise, and the phase of the injection signal depends on the distance between the injection source and the chip. To ensure coherent combining at a desired point in space, a phase-shifter in each transmitter is incorporated. As shown in Fig. 12, an active current-mode phase shifter with quadrature generation network is implemented. A quarter-wave transmission line is used to generate the quadrature signal. In order to prevent reflections, both I and Q signal paths are first matched to 100Ω using coupled transmission lines with $Z_0 = 100\Omega$. Then a 50Ω transmission line matches to the previous buffer amplifier, preventing any reflections at the split junction. The quadrature inputs are fed into the phase shifter, which takes the linear combination of the two phases in the current domain. The gain and phase are controlled by the weights of four input signals that have different phases (0°, 90°, 180°, 270°). The signal is attenuated by 3dB in this stage, which is compensated by subsequent amplification. Continuous phase-shifting is achieved by tuning analog voltages V_{b0}, V_{b90}, V_{b180}, and V_{b270}. Compared to passive phase shifters such as the trombone shifter [23] or the varactor-loaded transmission line [24], the implemented active phase shifter consumes less area, provides higher gain and enables continuous phase tuning. The resolution of the phase shifting is limited only by the resolution of the digital-to-analog converter (DAC). The phase simulation is shown in Fig. 12. Due to the extra quarter-wave transmission line for the quadrature path in the I/Q generation network, the Q voltage is attenuated by 0.9dB. This can be compensated in measurement by adjusting the bias voltages of the phase shifter.

D. Power Amplifier

The final stage of the transceiver is a four-stage PA shown in Fig. 13. The PA is designed with inter-stage matching using differential transmission lines that have side and bottom ground shields. Each stage is matched using a series capacitor, a series transmission line, and a shorted-stub shunt transmission line. The series capacitor and series transmission line rotate around the Smith Chart to the optimal conductance obtained from load-pull simulations, then the shunt transmission

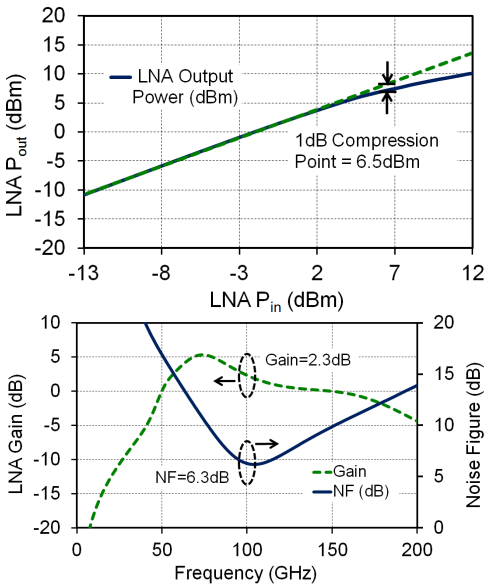

Fig. 11. Simulated LNA gain, noise figure, and 1-dB compression point.

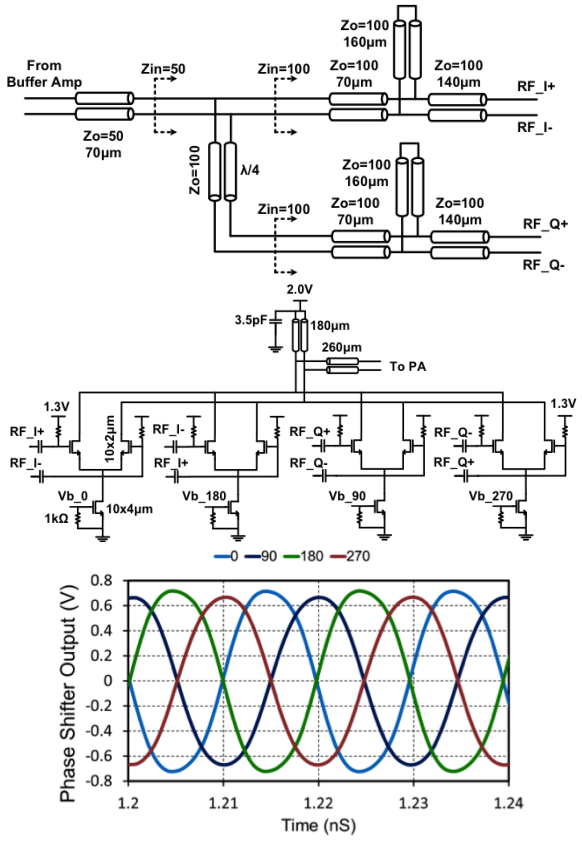

Fig. 12. Top: Schematic of the quadrature generator and the phase shifter. Bottom: Output of the phase shifter under the locked condition. The difference in magnitude is due to the quarter-wave line and can be compensated by adjusting the bias voltages V_{b0}, V_{b90}, V_{b180}, and V_{b270}.

line acts as an inductor to tune out the combined susceptance of the load and the transistor source, achieving resonance at 50GHz. The transistors are progressively sized to provide maximum gain and prevent saturation. Metal-insulator-metal

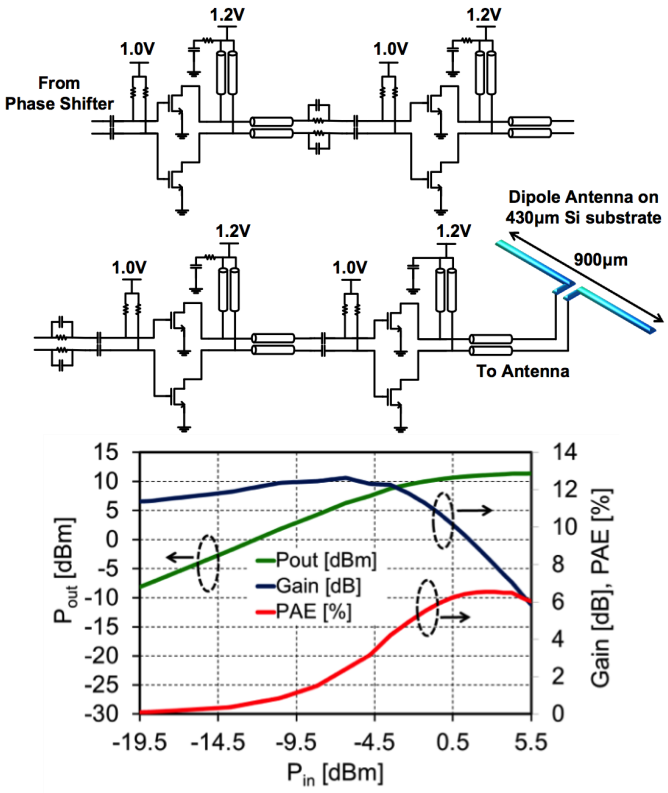

Fig. 13. Top: Schematic of the 4-stage PA and the dipole antenna. The dipole antenna is above a total substrate thickness of $430\mu m$. Bottom: Simulated large-signal behavior of the power amplifier. The PA achieves 12.5dB gain, 11dBm output power, and 6.5% maximum PAE.

(MIM) capacitors with values of 280fF act as DC-blocking capacitors to enable independent biasing at each stage. The capacitor has a self-resonant frequency of 120GHz, which is far above the operating frequency. The quality factor of the capacitor at the operating frequency of 50GHz is 37. Mm-wave amplifiers suffer from severe instability due to the use of high-gain transistors and high-quality factor resonant tanks.

At mm-wave frequencies, the PCB traces and wirebonds are comparable to the wavelength, making the on-chip bias nodes non-ideal AC grounds. As a result, the feedback from drain to gate, source to gate or even inter-stage feedback may cause instability. In order to improve stability, several measures are taken. First, a parallel RC tank is placed in series with the signal path. The R and C values are carefully selected to attenuate low GHz frequencies while passing the 50GHz signal. In addition, instead of using high-Q transmission lines, biasing resistors are used at the gate to reduce the quality factor at that node. Furthermore, each amplifier includes series RC circuits to form a lossy, low-impedance path between bias and ground to reduce the undesired feedback. In this design, each amplifier stage incorporates multiple series RC tanks in parallel to achieve a total of 7.2pF capacitance. The k-factor of each stage is simulated to ensure unconditional differential and common-mode stability. As shown in Fig. 13, the PA achieves 12.5dB gain, 11dBm output power, and 6.5% maximum PAE.

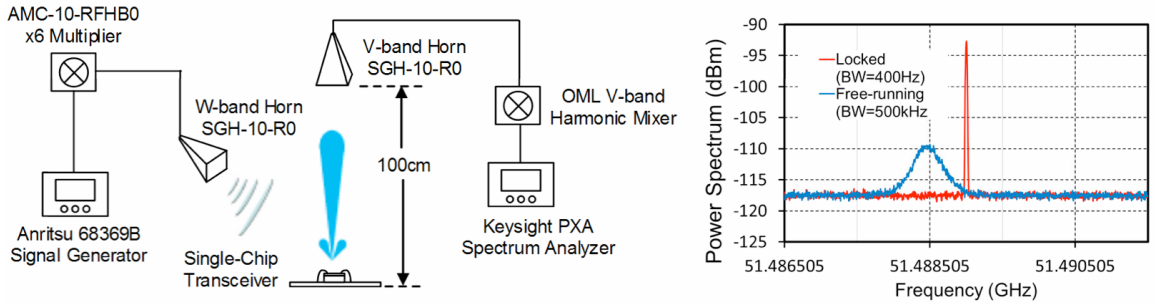

Fig. 14. Left: Measurement setup for single-chip wireless synchronization. Right: Spectrum of free-running vs. wirelessly injection-locked oscillator.

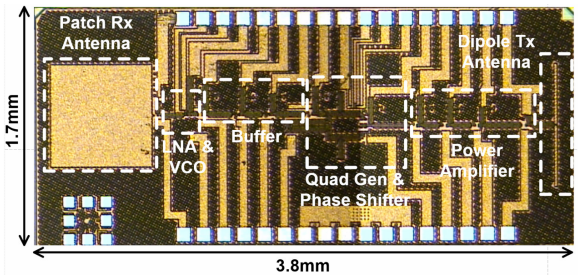

Fig. 15. Chip micrograph. The design was implemented in 65nm CMOS and occupies an area of 1.7mm × 3.8mm.

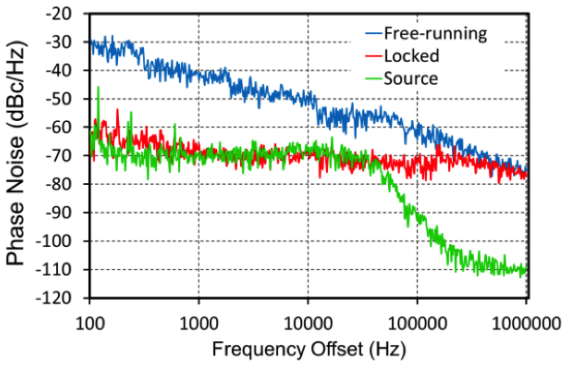

Fig. 16. Measured phase noise for free-running oscillator, locked oscillator and injection source.

IV. Measurement Results

A. Single-chip Wireless Synchronization

The chip was designed and implemented using IBM's 65nm bulk CMOS technology. The size of the chip including the on-chip antenna and bondpads is 1.7mm × 3.8mm. The chip micrograph and the measurement setup are shown in Fig. 15 and 14. A high-resistivity silicon wafer is attached in between the chip and the PCB ground, producing an effective substrate thickness of 430m. The chip consumes a total of 330mW. Tuning range of the IL-VCO was measured using OMLs V-band harmonic mixer and standard-gain horn antenna WR-15 M15RH. The tuning voltage was varied from 0 to 1.6V, and the observed oscillation frequency ranged from 51.3 to 52.1GHz, demonstrating a tuning range over 800MHz. The maximum detectable distance between the chip under test and the receiving horn antenna was 100cm. No lens was used in this measurement. Accounting for the respective mixer and cable losses of 40dB and 3.5dB, the calibrated received power was -51.5dBm. As a result, radiated power of -5dBm was calculated using the Friis formula.

In order to demonstrate wireless injection locking, an Anritsu 68369B signal generator was used in conjunction with Millitechs AMC-10-RFHB0 6 multiplier and a W-band, pyramidal horn antenna SGH-10-RO to inject the locking signal to the chip. The output power of the multiplier was 10dBm. The distance of the horn antenna and the chip was about 5cm. The simulated gain of the patch antenna at $(45°, 0)$ is -7.7dBi. From the Friis formula, the received power injected at the IL-VCO is calculated to be -24dBm. Fig. 16 shows the spectrum of the IL-VCO in the free-running and injection-locked modes. Based on this measurement, the 3dB spectral bandwidth of the locked and unlocked signals are 400Hz and 500kHz, respectively. 400Hz at 50GHz translates to a frequency stability of 8ppb. The IL-VCO tuning range and its locking range were shown in [13]. The IL-VCO frequency is exactly half of the injected frequency, demonstrating successful wireless locking. The locking range of the transceiver is >3MHz. Fig. 16 shows the phase noise measurements of the free-running transceiver, the locked transceiver, and the signal generator. The phase noise is significantly reduced (40dB at 100Hz offset; 23dB at 1kHz offset) upon injection of the wireless signal, enabling rapid scaling of the transceiver array.

B. Spatial Power Combining using Wireless Injection Locking

Upon characterization of the single-chip locking, we proceed to demonstrate spatial power combining of two widely-spaced chips using wireless injection locking. The measurement setup is shown in Fig. 17. The measurement horn antenna was placed 40cm from the center of the two radiating chips such that they are within the main lobe of the horn antenna. To compensate for the conversion loss of the W-band mixer, PL-60 lenses are used between each chip and the receiving horn to increase the received power. In a similar fashion, the 2nd harmonic wireless injection path also uses two lenses to focus the power towards each chip. As shown in the graph, the two chips are spaced 13cm apart $(\sim 22\lambda_0)$, and the receiving horn antenna is placed 40cm away from the center point of the two chips. Each chip is placed on an angled platform of 25 in order to direct the transmission power towards the receiving horn. During the experiment, we first

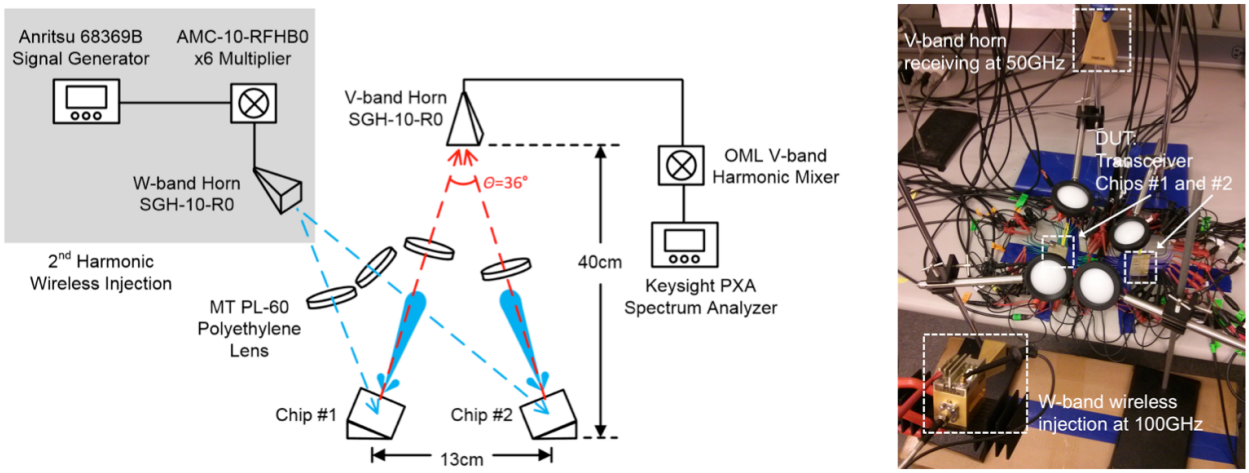

Fig. 17. Left: Measurement setup for power combining. Right: Photo of power combining measurement setup.

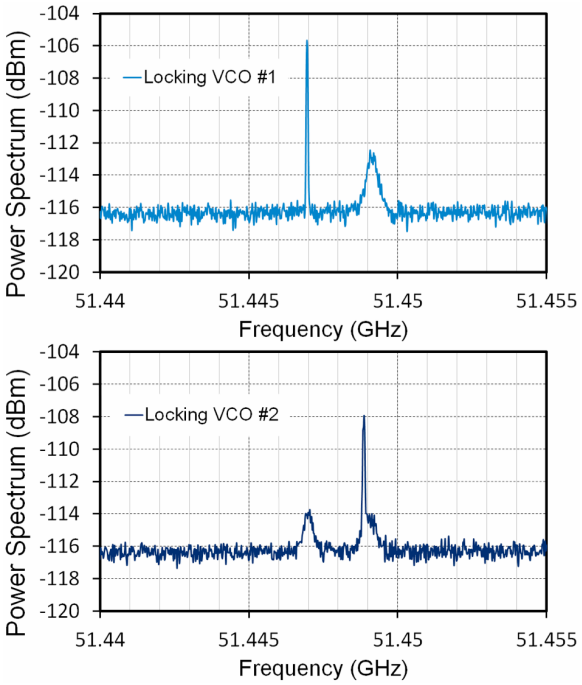

Fig. 18. Demonstration of individual locking.

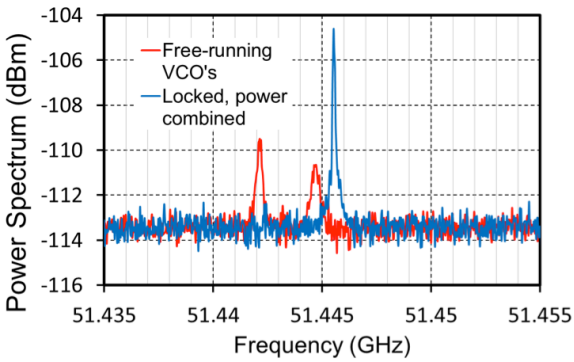

Fig. 19. Measured spectrum of free-running and power-combined signals (RBW=100kHz).

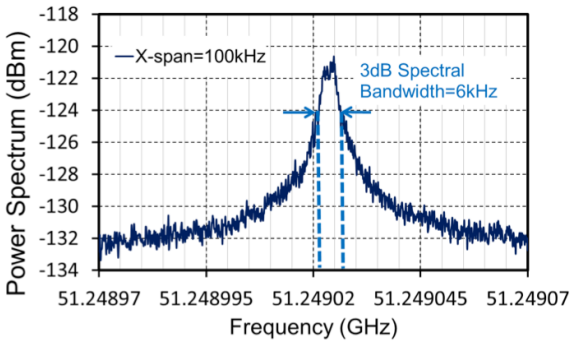

Fig. 20. Measured 3dB spectral bandwidth of the combined signal (RBW=1kHz).

tune each IL-VCO such that their free-running frequencies are distinctly apart. Then with the fixed hardware setup, we vary the injection frequency to lock each chip individually. This is shown in Fig. 18, where each chip is in turn injection locked. Upon verification of individual locking, we then tune the IL-VCOs such that their free-running frequencies are as close as possible, followed by injection of the wireless signal. Fig. 19 shows the overlaid spectrum of the two free-running VCOs prior to tuning them to be close, and the locked, power-combined signal (RBW=100kHz). As can be seen, the spectrum sharpened significantly upon injection of the wireless signal, demonstrating successful power combining.

The combining efficiency can be characterized by measuring the spectral bandwidth. In Fig. 20 (RBW=100kHz), we zoom in to the power-combined signal and measure a 3dB spectral bandwidth of 6kHz, equivalent to frequency stability of 120ppb. In this experiment, the spectral bandwidth is mainly limited by the measurement equipment. Better locking may be achieved by injecting more power or increasing the frequency tuning resolution of the VCO. In addition, other factors such as the phase noise of each chip, power and phase noise of the injected signal, the phase difference between the chips, and the polarization loss between the transmitters and the receiver

TABLE I
COMPARISON WITH STATE-OF-THE-ART SILICON MM-WAVE TRANSCEIVERS

	[9]	[10]	[3]	This work
Architecture	Pulsed	Pulsed	Continuous-wave	Continuous-Wave
Locking Mechanism	Wired digital-to-impulse	Wired asymmetric VCO	Incoherent	Wireless injection
Process	130nm BiCMOS	130nm BiCMOS	90nm BiCMOS	65nm CMOS
Frequency (GHz)	220	30	530	100/50
Lenses	Yes	Yes	Yes	No
Chip Spacing	1.1cm	5cm	N/A	13cm
Inter-chip Spatial Combining	Yes	Yes	No	Yes
Power Consumption (mW)	220	106	156	330
Die Area (mm2)	0.47	2.85	4.2	6.46

may also affect the spectral bandwidth of the combined signal.

V. CONCLUSION

In this work, demonstration of a coherent multi-chip system with widely-spaced elements using wireless injection locking is reported for the first time. Wireless injection locking of a single chip results in a 3dB bandwidth of 400Hz at a carrier frequency of 50GHz, or stability of 8ppb. In addition, spatial power combining using two widely-spaced chips is demonstrated with 6kHz 3dB bandwidth. The chip is implemented in IBM's 65nm bulk CMOS process and occupies an area of $6.5mm^2$. Table I provides a performance comparison between state-of-the-art mm-wave transceivers. This work sets the foundation for increasing the element spacing of an array through wireless injection locking, extending traditional array systems into the high-resolution, narrow-beamwidth regime. Furthermore, the wireless nature makes the proposed methodology suitable for building an array on non-planar substrates or on mobile platforms.

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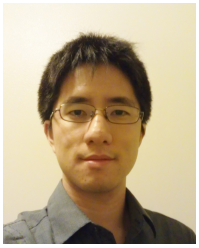

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