Cost-Effective Radiation Hardening Technique for Combinational Logic

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Abstract— **A radiation hardening technique for combinational logic circuits is described. The key idea is to exploit the asymmetric logical masking probabilities of gates, hardening gates that have the lowest logical masking probability to achieve cost-effective tradeoffs between overhead and soft error failure rate reduction. The technique, which decouples the physical from the logical aspects of soft error susceptibility of a gate, uses a novel gate (transistor) sizing technique that is both efficient and accurate (in comparison to SPICE). A full set of experimental results demonstrate the cost-effective tradeoffs that can be achieved.**

I. Introduction

When high-energy neutrons (present in terrestrial cosmic radiation) or alpha particles (that originate from impurities in the packaging materials) strike a sensitive region in a semiconductor device, the resulting single-event upset (SEU) can alter the state of the system resulting in a soft error. Soft errors in memories (both static and dynamic) have traditionally been a much greater concern than soft errors in combinational logic circuits (for the same minimum feature size) since memories contain by far the largest number and density of bits susceptible to particle strikes. In the next decade, technology trends—smaller feature sizes, lower voltage levels, higher operating frequencies, reduced logic depth—are projected to cause an increase in the soft error failure rate in core combinational logic in integrated circuits [4], [14], [18].

Radiation hardening techniques for fault avoidance (fault intolerance) to increase reliability primarily rely on conservative design practices such as the use of high reliability components, the exclusion of radiation-sensitive circuit styles (such as dynamic logic and non-CMOS styles), and the incorporation of sufficient functional margin in circuit designs to account for anticipated shifts in circuit characteristics [6], [12], [19]. Such techniques have been historically used for space and mission critical applications (e.g., traffic control, banking, medicine). In such applications, the primary objective is to achieve very high reliability with cost and performance as secondary concerns.

However, the overhead (area, power, delay) costs of traditional radiation hardening approaches (often exceeding 100%) are unacceptable for high-volume mainstream applications, where cost and performance are the primary objectives. Traditionally for mainstream applications, soft error failure rates have been tolerable with no need for fault avoidance and fault detection/tolerance. As the soft error failure rate in mainstream application environments increases, there is a need for low overhead solutions to meet the demands of the highly competitive and cost sensitive mainstream commercial market [1]. Whereas traditional fault avoidance techniques for mission critical applications target all modeled faults, fault avoidance techniques for mainstream applications need to target soft error failure rate reductions in a cost-effective manner.

This paper describes a new technique for designing radiation-hardened combinational logic circuits that spans the middle ground between no protection/no overhead and very high protection/very high overhead. Rather than focus on all modeled faults, radiation hardening is targeted towards the nodes that have the highest soft error susceptibility, i.e., the nodes that contribute the most to the soft error failure rate of the logic circuit. This allows cost-effective tradeoffs between radiation hardening overhead and soft error failure rate reduction.

The proposed approach belongs to a class of techniques for radiation hardening that increase (or maximize) the critical charge (Q_{crit}) for nodes in a design. Q_{crit} is the minimum amount of charge that needs to be deposited by a particle strike to produce a SEU [6]. A node is hardened by adding capacitance (to increase Q_{crit}), or drive (to dissipate deposited charge), or a combination of both. For elementary CMOS gates, this is achieved by sizing gates (or just transistors), i.e., by altering the W/L ratios of the transistors in the gates. The proposed algorithm uses an efficient fault simulation-based technique to identify and rank the critical nodes that contribute significantly to the soft error failure rate of a combinational logic block. A fast and accurate technique is used to size these critical gates to render them immune to SEUs with specified worst-case characteristics. All the gates are processed in a single pass to optimize the design to meet soft error failure rate reduction requirements. The proposed technique is compatible with other optimization techniques that specifically target area, delay, and/or power reduction. It can also be used to complement other fault avoidance and fault detection/tolerance techniques such as the use of silicon-on-insulator substrates, error detection and correction codes, etc. to further reduce the soft error failure rate. Experimental results for 180nm and 130nm process technologies are presented to show that the proposed technique reduces the soft error failure rate significantly with minimal impact to overhead.

The rest of this paper is organized as follows. In Sec. II, we motivate the problem in greater detail and discuss the key ideas that are presented in this paper. In Sec. III, we formulate the problem of gate sizing for SEU immunity and present a technique that achieves this objective. In Sec. IV, we present the proposed algorithm for soft error failure rate reduction in combinational circuits. In Sec. V, we present and discuss simulation results for several combinational benchmark circuits. Section VI is a conclusion.

II. MOTIVATION

Since radiation bombards a chip fairly uniformly in space and time, the probability of a particle strike at a combinational node is roughly proportional to its active area. Following a strike, the characteristics of a SEU vary greatly depending on which node it occurs at in the combinational logic circuit. For a specific application, the first step in radiation hardening is to select a range of incident particle energies over which the probability of occurrence of a particle is significant enough to require hardening. We defer a discussion on how this range can be selected to Sec. V in this paper. Once a range of particle energies is chosen, the two factors that determine whether a particle strike at a node produces a SEU at that node are (1) the critical charge of the node and (2) the drive strength of the gate that drives the node. In this section, we begin by discussing how transistor sizing within a gate to alter its drive strength affects the vulnerability of the gate to SEUs. The focus is on the magnitude and duration of the SEU that results from a particle strike, as a function of charge and drive strength. The masking factors that influence how a SEU propagates through a logic circuit are described. We discuss how sensitization, one of the masking factors, can be used to rank and size the gates in a logic circuit to decrease the soft error failure rate.

A. Sizing and SEU vulnerability

Consider a 2-input nand gate driving a lumped capacitance C_p at its output N. The total capacitance at N is:

$$C_{total} = C_{unit}\,(W/L) + C_p \tag{1}$$

Here, (W/L) is the size of a single nMOS transistor in the nand gate.† C_{unit} is the unit output capacitance (includes nMOS and pMOS) obtained by dividing the output capacitance of the nand gate by the size of the nMOS transistor in the nand gate. C_p is the lumped parasitic capacitance (interconnect and fanout) at N. We focus on the voltage $V_{out}(t)$ at N, since its magnitude and duration will determine how a SEU propagates through gates in the transitive fanout of the nand gate to the primary outputs/latches/flip-flops.

The charge deposition due to a particle strike at N is modeled by a double exponential current pulse $I_{in}(t)$ at the site of the particle strike [5], [15]:

$$I_{in}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \tag{2}$$

where Q is the charge (positive or negative) deposited as a result of the particle strike, τ_α is the collection time-constant of the junction, and τ_β is the ion-track establishment time-constant. τ_α and τ_β are constants that depend on several process-related factors.

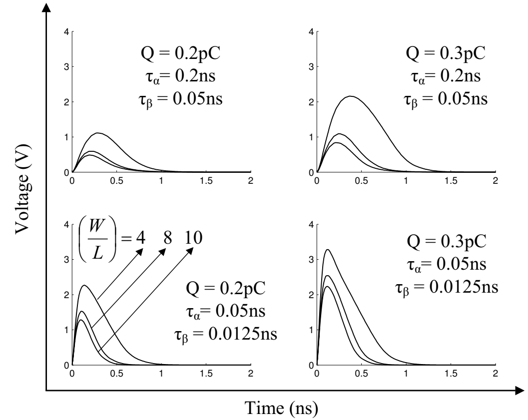


Fig. 1. SEU effects$\left(Q, \frac{W}{L}, (\tau_\alpha, \tau_\beta)\right)$

With this model, Fig. 1 presents how sizing affects the vulnerability of the nand gate to particle strikes. The output response of the nand gate (determined using SPICE simulations) to a SEU that produces a $0 \rightarrow 1$ transient at the output—for combinations of values of transistor sizing, process parameters τ_α and τ_β, as well as deposited charge—is presented. In each sub-figure, it is clear that as the size of the nMOS transistors (that dissipate the deposited charge) increases, the magnitude and duration of the SEU transient diminish rapidly. In other words, transistors (i.e., gates) can be sized to dissipate (sink) the injected charge as quickly as it is deposited, so that the transient does not achieve sufficient magnitude and duration to propagate to the fanout. Besides τ_α and τ_β, the maximum charge Q for which SEU immunity is desired (i.e., the range of incident particle energies) has to be considered to determine this optimal transistor size.

B. Masking factors

A simple and direct solution to radiation harden a logic circuit would be to size all the gates over a range of particle energies. However, the overhead costs of such an approach will be prohibitive. Selective hardening of the most sensitive gates can be performed, to significantly harden the logic circuit with lower overhead costs. The factors that affect the capability of a SEU to propagate through the logic circuit and cause a soft error can be used for this purpose. Whereas the rate at which a SEU at a node occurs depends on incident particle energy distribution, the drive strength of the gate, and the critical charge, there are three masking factors that determine whether

†Although we refer to transistor sizes and use W/L in the formulation, we limit ourselves to symmetric gate sizing in this paper for reasons explained in Sec. III-A. Thus, scaling a single transistor is equivalent to scaling all transistors (nMOS and pMOS) in the gate by the same ratio.

this SEU can propagate to the primary outputs/latches/flip-flops and result in a soft error:

1) Logical masking occurs in the absence of a functionally sensitized path from the gate to the primary outputs/latches/flip-flops.
2) Electrical masking occurs if the SEU is attenuated as it propagates along a sensitized path to the primary outputs/latches/flip-flops.
3) Latching-window masking occurs if a SEU reaches the primary outputs/latches/flip-flops at an instant other than the clocking window

Note that the rate at which soft errors are generated at a primary output/latch/flip-flop due to SEUs at a particular gate diminishes as each masking factor increases. Note also that each masking factor has to be considered independent of the other two. While these three factors present a natural barrier to soft errors in logic circuits [13], technology trends such as smaller feature sizes, lower voltage levels, higher operating frequencies, and reduced logic depth are causing these barriers to diminish significantly. In [16], it was shown that as a result of these factors, the soft error susceptibility of internal nodes (which is the contribution of the node to the overall soft error failure rate) in a logic circuit can vary by an order of magnitude or more. This provides an opportunity to significantly reduce the soft error failure rate at reduced cost, since nodes with high soft error susceptibility can be hardened, while those with very low soft error susceptibility can be ignored. By selectively hardening only those nodes that are most susceptible to SEUs, the soft error failure rate in logic circuits can be significantly reduced at a fraction of the cost of conventional techniques that try to harden all nodes.

C. *Asymmetric sensitization*

The central idea in this paper is to decouple sensitization, which determines the propagation probability of a SEU in Boolean terms, from the electrical and physical properties of SEU vulnerability at a gate in a logic circuit. Consider the three masking factors introduced in Sec. II-B. Logical masking depends on the input pattern that is being applied to the circuit, i.e., whether or not there is a sensitized path from the gate to the primary outputs/latches/flip-flops. The probability of logical masking at the gate is given by:

$$P_{logical\ masking} = 1 - P_{sensitization} \tag{3}$$

where $P_{sensitization}$ is the probability of sensitization, i.e., the probability that there exists one (or more) functionally sensitized paths from the gate to the primary outputs/latches/flip-flops. Consider the node G_3 shown in Fig. 5. If a is set to logic 0, the effects of a SEU at G_3 are logically masked from the primary output G. Similarly, if either (or both) G_5 and G_6 evaluate to logic 1, a SEU at G_3 will be logically masked from primary output H, since one or more side inputs along the SEU's propagation path are set to controlling values. Logical masking leads to a high asymmetry—for SEUs of the same magnitude—in the soft error susceptibility of gates in combinational logic. A similar observation from testing theory is that fault detectability can vary by orders of magnitude across a design. Electrical masking depends on the electrical properties of the intermediate gates along a sensitized path, i.e., on their drive strengths. Similar to logical masking, SEUs at gates several levels of logic deep are likely to have a higher probability of electrical masking. Results from [2] suggest that while electrical masking does produce an observable effect, it does not significantly reduce the observed soft error failure rate. It follows that the probability of electrical masking does not exhibit an asymmetry similar to the probability of logical masking—for SEUs of the same magnitude—across all gates in a logic circuit. Finally, latching-window masking depends on the frequency of operation of the circuit. The probability of latching-window masking is essentially the same—for SEUs of the same magnitude—across all the nodes in a logic block. In summary, besides gate sizing, sensitization probability is the one factor that contributes significantly to the asymmetry in the soft error susceptibility of gates in a combinational circuit. In this paper, we use this asymmetric distribution in sensitization (logical masking) probabilities to rank and radiation harden the most susceptible gates in a design.

To illustrate this skew, the sensitization probability distribution profile for six benchmark circuits is presented in Fig. 2. Sensitization probability on the x-axis is divided into ten intervals from 0 to 1, and the y-axis shows the number of nodes with a sensitization probability in each interval. The primary outputs, which are always sensitized, are omitted from the histograms. It is clear from the figure that less than 20% of the gates on average have a high sensitization probability (> 0.8) in logic circuits.

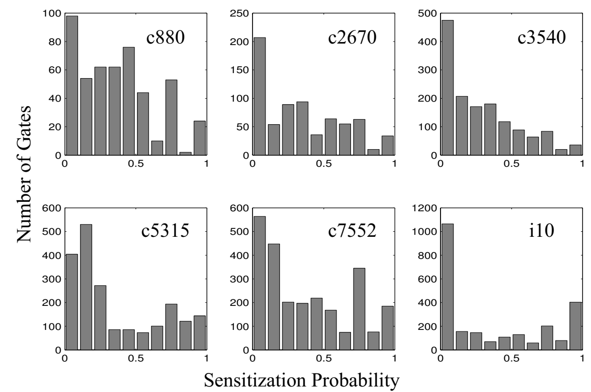


Fig. 2. Sensitization probability distribution

D. *Accuracy versus efficiency*

There is a tradeoff between the accuracy of radiation hardening techniques and their computational efficiency. While it can be argued that addressing the soft error robustness of a logic circuit following physical design when maximum information is available is very accurate, the computational cost renders such techniques prohibitive. There is a need for techniques to incorporate SEU-robustness metrics into the design cycle at higher levels of abstraction, i.e., earlier in the

design cycle, to realize inherently robust circuits. By modeling SEU effects at the gate-level, the computational bottleneck can be significantly alleviated. Post-mapping transformations of the kind proposed in this paper can significantly improve the soft error robustness of integrated circuits. They can also lessen the investment in such strategies at lower levels of the design process, thereby decreasing the number of iterations in the design cycle.

III. Sizing for SEU Immunity

In this section, we describe an efficient method to compute the minimum transistor size $(W/L)_{min}$ required to limit the maximum value of the transient pulse $V_{out}(t)$ at N to a pre-specified value. This builds on the efficient simulation techniques presented in [22]. For the rest of this discussion, we assume this limit on the peak value is $0.5V_{DD}$ (that is V_{IH} for gates in the transitive fanout). Note that the method is equally applicable for any other limit on the peak value of V_{out}. Without loss of generality, we describe a technique to size the nMOS transistors in a logic gate for SEU immunity. The method is equally applicable to sizing the pMOS transistors in a gate. While the pMOS and nMOS transistors can be sized independently in a logic gate, this has implications for gate sizing that are discussed in Sec. III-A.

The voltage $V_{out}(t)$ following a particle strike is given by the solution to the following differential equation:

$$C_{total}\left(\frac{\mathrm{d}V_{out}}{\mathrm{d}t}\right) = I_{in}(t) - (W/L)\cdot I_D(V_{out}) \qquad (4)$$

where C_{total} is the total capacitance at N (Eqn. 1), $I_{in}(t)$ is the current from the particle strike (Eqn. 2), and (W/L) is the aspect ratio of a single nMOS transistor in the gate. I_D is the effective drain current through the nMOS transistor network in the gate and is a function of V_{out}. It is assumed that the pMOS transistors are off, since the inputs to the gate are such that N evaluates to logic 0 when the SEU occurs. The cross-coupled nature (time t and voltage V_{out}) of the differential Eqn. 4 implies that there is no closed form expression for the instant t_{max} when $V_{out}(t)$ reaches $0.5V_{DD}$. However, since t_{max} occurs after the injected current $I_{in}(t)$ reaches its maximum, it is possible to use the following iterative procedure to compute t_{max}.

The first step is to determine a suitable search interval for t_{max}. The maximum value of $I_{in}(t)$ occurs at a time instant t_{start} that is given by

$$t_{start} = \left(\frac{\tau_\alpha\cdot\tau_\beta}{\tau_\alpha-\tau_\beta}\right)\cdot\ln\left(\frac{\tau_\alpha}{\tau_\beta}\right) \qquad (5)$$

from Eqn. 2. t_{start} can be used as the beginning of the search interval for t_{max}, since $t_{max} \geq t_{start}$. t_{max} is located in the interval $[t_{start}, t_{ref}]$, where t_{ref} is bounded by the clock period of the logic circuit. If $0.5V_{DD}$ is the maximum value of $V_{out}(t)$ at time t_{max}, two conditions must be satisfied by Eqn. 4. The first condition is that the slope $\mathrm{d}V_{out}/\mathrm{d}t$ must equal 0 at t_{max}, i.e.,

$$I_{in}(t_{max}) - (W/L)_{min}\cdot I_D(0.5V_{DD}) = 0 \qquad (6)$$

where $(W/L)_{min}$ is the minimum transistor size required to limit the peak of the SEU transient to $0.5V_{DD}$. Rearranging,

$$\left(\frac{W}{L}\right)_{min} = \frac{I_{in}(t_{max})}{I_D(0.5V_{DD})} \qquad (7)$$

The second condition is given by charge conservation over the interval $[0, t_{max}]$. In other words, the integral of both sides of Eqn. 4 over the interval $[0, t_{max}]$ must be equal, i.e.,

$$\begin{aligned}(C_{unit}(W/L)_{min}+C_p)\int_0^{0.5V_{DD}}\mathrm{d}V_{out} = \\ \int_0^{t_{max}} I_{in}(t)\,\mathrm{d}t - (W/L)_{min}\int_0^{t_{max}} I_D(V_{out})\,\mathrm{d}t\end{aligned} \qquad (8)$$

Since $I_D(V_{out})$ is a non-linear equation that depends on $V_{out}(t)$, the following approximation is used to simplify the integral. We assume that the voltage $V_{out}(t)$ rises from 0 to the peak value of $0.5V_{DD}$ linearly, i.e.,

$$V_{out}(t) = 0.5V_{DD}\cdot\left(\frac{t}{t_{max}}\right) \text{ for } 0 \leq t \leq t_{max} \qquad (9)$$

As a result, I_D is just a function of time t and Eqn. 8 is directly integrated to get a non-linear equation in $(W/L)_{min}$ and t_{max}. Note that this assumption is accurate since the nMOS transistors are in the linear region of operation ($V_{out} \leq 0.5V_{DD}$). With this approximation, Eqn. 7 and Eqn. 8 can be solved using the bisection method [17] over the interval $[t_{start}, t_{ref}]$ to determine both unknowns t_{max} and $(W/L)_{min}$ simultaneously. The number of iterations to determine $(W/L)_{min}$ using the bisection method for an error tolerance of 0.001ns and t_{ref} of 1ns is 10. A comparison between the results obtained using this method and SPICE is presented in Fig. 3. The solid curve represents the results obtained using the above method while the dotted curve represents the results obtained using SPICE. It is clear that the results obtained using the proposed sizing method are in excellent agreement with SPICE, at significantly less computational cost.

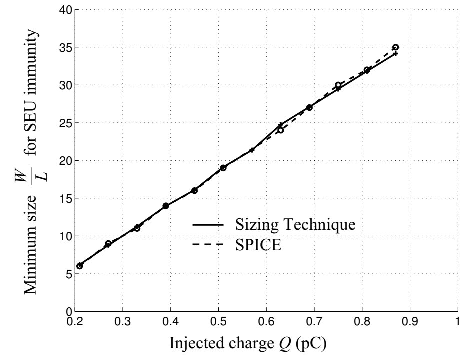


Fig. 3. Sizing for SEU immunity

A. Continuous, symmetric gate sizing

Since the nMOS (pMOS) network of a CMOS gate can be sized independently of the pMOS (nMOS) network, the

above algorithm can be extended to size CMOS gates asymmetrically. This disadvantage of skewing transistor sizes significantly is that the $1 \rightarrow 0$ ($0 \rightarrow 1$) delay through the gate can be significantly affected. For example, increasing the W/L of the nMOS transistors adds to the diffusion capacitance and can significantly increase the pull-up time of a gate if the pMOS transistors are not adequately resized. If the rising transition through the gate lies on the critical path, this can significantly impact performance. This paper only discusses symmetric gate sizing for radiation hardening.

IV. Proposed algorithm

In this section, we formulate the gate sizing problem for SEU immunity. We show how the gate sizing technique presented in Sec. III can be used to size critical nodes in a logic circuit to reduce the soft error failure rate significantly with minimal impact to overhead.

A. Problem statement

Given a mapped combinational circuit composed of gates from a technology library. For each gate g in the circuit, several different sizes $1, 2, \ldots, k$ are available in the library, each of which implements the same logic function but differs in one or more of the following aspects—area, delay, drive strength, and power consumption. The gate sizing problem for SEU immunity is to select optimum sizes for each (or a subset) of the gates in the combinational logic circuit such that the objective function—defined by the susceptibility of the logic circuit to SEUs (i.e., the soft error failure rate of the logic circuit)—is minimized.

B. Proposed algorithm

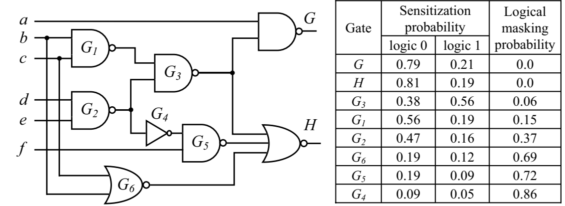
The pseudo-code for the proposed procedure for radiation hardening is presented in Fig. 4. While coverage is the only objective considered for the rest of this paper, other constraints can also be directly integrated into the formulation as explained in Sec. IV-C.

```
netlist – technology mapped version of the logic circuit
coverage – desired reduction in soft error failure rate
constraints – overhead; possibly area, delay, and/or power
sensitizationQ – priority queue of gates

FAULT-SIMULATE(netlist);
for each gate g ∈ netlist
    do ENQUEUE(sensitizationQ, g, P_sensitization(g))
while coverage is not met and constraints are not violated
    do SIZE-SEU-IMMUNITY(EXTRACT-MAX(sensitizationQ))
       UPDATE-COVERAGE-CONSTRAINTS(netlist)
       DEQUEUE(sensitizationQ)
```

Fig. 4. Radiation-Harden($netlist$, $coverage$, $constraints$)

The first step is to rank all the gates in the circuit in descending order of their sensitization probability using the method Fault-Simulate as follows. Since the probability of logical masking of a node depends on the probability of each input pattern being applied to the circuit, an efficient way to calculate the probability of logical masking is to simply simulate the system with a typical workload for some number of clock cycles. For each clock cycle, fault simulation can be performed on each gate to determine if it is sensitized to one or more outputs/latches/flip-flops. Nodes which are only sensitized for a very few input patterns will have a negligible effect on the overall soft error rate (since their probability of being sensitized is extremely low) and can hence can be ignored for radiation hardening. A less accurate alternative to simulating the system with a typical workload would be to just apply random patterns at the primary inputs to get a rough estimate. Fault simulation was run on the circuit in Fig. 5 in this manner and the logic 0 and logic 1 sensitization probabilities were computed as shown in the figure. Note that the fraction of cycles where a node may assume a logic 0 value may differ significantly from the fraction of cycles when the node assumes a logic 1 value. As a direct consequence, there can be a significant difference between the logic 0 and logic 1 sensitization probabilities of a gate, especially if there is reconvergent fanout in the logic circuit (e.g., G_2). Since this paper focuses on continuous, symmetric gate sizing, the logic 0 and logic 1 sensitization probabilities are collapsed (summed) when the gates are inserted into the priority queue $sensitizationQ$.



Gate	Sensitization probability		Logical masking probability
	logic 0	logic 1	
G	0.79	0.21	0.0
H	0.81	0.19	0.0
G3	0.38	0.56	0.06
G1	0.56	0.19	0.15
G2	0.47	0.16	0.37
G6	0.19	0.12	0.69
G5	0.19	0.09	0.72
G4	0.09	0.05	0.86

Fig. 5. Identifying and ranking critical gates

Gates are dequeued from $sensitizationQ$ in decreasing order of their collapsed sensitization probability (increasing order of logical masking probability). The gates are processed in decreasing order ($G, H, G_3, G_1, \ldots$ for Fig. 5) till the $coverage$ objective is met or any of the $constraints$ are violated. The gate sizing routine Size-SEU-Immunity symmetrically sizes both the nMOS and the pMOS transistors in a library gate using the technique from Sec. III. Once the minimum size for SEU immunity is determined for a gate, the transistor sizes (both nMOS and pMOS) are updated as follows:

$$(W/L)_{updated} = \max\left\{(W/L)_{original}, (W/L)_{min}\right\}$$

Note that the scaling of the gate is done such that the ratio of the sizes of the nMOS and pMOS transistors in the original library gate remains unchanged.

The routine Update-Coverage-Constraints first updates coverage, which is defined as follows:

$$\text{Coverage} = \left(\frac{\sum\limits_{\text{(candidates } g_c)} P_s(g_c)}{\sum\limits_{\text{(all gates } g)} P_s(g)} \right) \cdot 100\% \qquad (10)$$

where $P_s(\cdot)$ returns the collapsed sensitization probability of a gate. Candidate gates g_c are all the gates that may be sized for SEU immunity as they are dequeued from $sensitizationQ$. Thus, the percentage of propagated SEUs over all the cycles is reduced (in %) by an amount that equals coverage for the worst case parameters, since the gates have been sized such that the SEUs will not propagate even if a sensitized path exists. Note that 90% (50%) coverage corresponds to an order of magnitude (factor of 2) reduction in the soft error failure rate for the chosen charge range (worst-case SEU parameters). For the circuit in Fig. 5, $\sum_{\text{(all gates } g)} (P_s(g))$ is 5.05—only gates $\{G, H, G_3\}$ may need to be sized for 50% coverage, while all the gates except G_5 and G_4 may need to be sized for 90% coverage. In Sec. V, we present simulation results that show that only 54.3% of the gates on average need to be considered candidates for sizing to achieve 90% coverage.

C. Design constraints

Sizing the transistors in a gate affects the three major design constraints: area, power consumption, and delay that can be integrated into the method UPDATE-COVERAGE-CONSTRAINTS. Since the constraints are updated after each gate is sized, the algorithm terminates as soon as one of the constraints is violated. Area information is obtained from physical layout of the standard cell library. Area changes in discrete steps as $(W/L)_{min}$ increases. This is because in most standard cell libraries, gates of drive strength 1 and 2, 3 and 4, etc. usually have the same cell area. Power changes continuously as the gate is sized. However, switching activity at each of the gates can be obtained during FAULT-SIMULATE and can be used to estimate the increase in power after each gate is sized using a simple load model. If either area or power constraints are violated and RADIATION-HARDEN terminates, the reduction in the soft error failure rate will be maximized since the gates were processed in order of criticality from $sensitizationQ$.

Delay is the most difficult constraint to handle, since sizing changes not only the drive strength of a gate, but also the input and output capacitances. The effects of sizing a gate are thus not localized from a delay perspective, since all the gates in the transitive fanin and transitive fanout are impacted by the change in capacitance. The load-dependent nature of delay means that the problem of gate sizing for delay is NP-complete [7]. Recomputing delay after each gate is sized may be computationally expensive, so it may be done only if the gate is on a critical path. Techniques, such as the one presented in [3], can also be used to decrease the delay of the circuit following the proposed sizing procedure. The gates that have actually been sized for SEU immunity are flagged such that their sizes are not further reduced (i.e., these sizes serve as a lower bound so that SEU immunity is not compromised).

V. SIMULATION RESULTS

The SPICE libraries used were from the TSMC 180nm and 130nm process technologies. The combinational benchmark circuits were chosen from the LGSynth91 suite [21]. We used $\tau_\alpha = 0.2$ns and $\tau_\beta = 0.05$ns in all our simulations [5]. We built a technology library that comprised inverters, and 2-input and 3-input nand and nor gates for synthesis of the benchmarks.

Upper bounds for the charge used for gate sizing are determined as follows. The term linear energy transfer (LET) is used to describe the sensitivity of a process technology to SEUs. A particle with a LET of 1 MeV·cm^2/mg deposits approximately 10 fC/μm of electron-hole pairs along its track [6], [14]. The LET of very few ionizing particles in silicon is higher than 15 MeV·cm^2/mg [9], [20]. The LET of a particle is multiplied by the charge collection depth to obtain the total electron-hole pairs generated by a strike. For process technologies of 180nm and higher, the charge collection depth does not change significantly and is typically 2 microns in bulk and epitaxial substrates [10], [14]. This gives an upper bound of 0.3pC for 180nm process technologies. For smaller feature sizes, the charge collection efficiency decreases due to higher doping densities [10], [11]. In [8], an inverse linear relation between collected charge and doping density was reported. Since the doping density at 130nm is usually more than twice the doping density at 180nm, the charge collection depth at 130nm is approximately 1 micron. This gives an upper bound of 0.15pC for 130nm process technologies.

Under the first major heading in Table 1, we provide details about the circuits that were chosen—name, number of primary inputs, number of primary outputs, and number of gates. Under the second major heading, we report the number of gates that were targeted for sizing. This remains constant, since we use logical masking as the criterion to determine coverage.

Under the third major heading, we report the area, power, and delay overhead when the gates in the circuit are sized to obtain 90% coverage (an order of magnitude reduction in the soft error failure rate) for a 180nm process technology. The charge used to simulate SEUs were 0.2pC and 0.3pC respectively. The overhead is normalized w.r.t to the area, power, and delay of the original circuit after technology mapping and is reported as a percentage in all the cases. The area numbers are derived from the technology library, while power and delay are given by

$$\text{Power} = f\left(W/L, C_{total}\right)$$
$$\text{Delay} = g\left(W/L, C_{total}\right)$$

where f and g are obtained from extensive simulation of the library cells. It is clear that an order of magnitude reduction in the soft error failure rate, i.e., 90% coverage, for worst case charge 0.3pC may be obtained with area, power, and delay overhead of 22.5%, 21.4%, and 12.2% on average. Further reductions can be achieved using other technology-dependent transformations following the proposed one.

Under the fourth major heading, we report results for a 130nm process technology. The charges that were used to simulate SEUs were 0.1pC and 0.15pC respectively. Similarly, for the worst case charge of 0.15pC, 19.4%, 18.0%, and 4.6% in area, power, and delay overhead are incurred on average.

TABLE I

RADIATION HARDENING OVERHEAD FOR A 90% REDUCTION IN SOFT ERROR FAILURE RATE

Name (PIs, POs, Gates)	Targeted Gates	180nm Technology				130nm Technology			
		Charge	Overhead (%)			Charge	Overhead (%)		
		(pC)	Area	Power	Delay	(pC)	Area	Power	Delay
b9 (41, 21, 211)	103	0.20	4.9	6.9	4.7	0.10	4.5	5.7	2.5
		0.30	16.5	22.2	3.9	0.15	15.2	18.5	0.0
c880 (60, 26, 512)	327	0.20	4.0	4.0	2.3	0.10	4.0	3.8	0.5
		0.30	25.9	25.0	10.6	0.15	25.1	23.7	4.3
c2670 (233, 140, 756)	418	0.20	1.4	1.1	0.6	0.10	1.2	0.9	0.4
		0.30	14.2	11.7	8.6	0.15	13.7	11.0	4.7
c3540 (50, 22, 1467)	815	0.20	7.8	9.6	10.3	0.10	7.6	8.7	2.7
		0.30	28.4	34.9	19.8	0.15	27.8	32.3	5.3
c5315 (178, 123, 2115)	1293	0.20	3.5	4.0	1.2	0.10	3.2	3.5	0.4
		0.30	19.3	20.7	12.9	0.15	18.5	18.8	3.1
c7552 (207, 108, 2534)	1485	0.20	3.8	4.2	5.8	0.10	3.7	3.9	2.8
		0.30	20.9	21.9	14.4	0.15	20.4	20.5	5.4
i10 (257, 224, 2646)	1212	0.20	3.5	3.2	4.5	0.10	3.3	2.7	2.6
		0.30	16.1	13.2	15.0	0.15	15.0	11.4	9.7
Average Overhead (%)		0.20	4.1	4.7	4.2	0.10	3.9	4.2	1.7
		0.30	22.5	21.4	12.2	0.15	19.4	18.0	4.6

VI. CONCLUSION

In the future, as designs become more complex and as the soft error failure rate of logic circuits becomes unacceptably high, there will be a need for gate-level techniques for radiation hardening. The gate sizing technique for radiation hardening presented in this paper targets soft error failure rate reduction by selectively sizing the most sensitive nodes in a logic circuit. An area for future research is to investigate how the proposed technique can be integrated with other technology-dependent optimization algorithms with multiple objectives.

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