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EDUCATION

PhD, Electrical and Computer Engineering **expected in 2008**

Department of Electrical and Computer Engineering, Rice University, Houston, TX

Master of Science, Electrical and Computer Engineering **May 2004**

Department of Electrical and Computer Engineering, Rice University, Houston, TX

Bachelor of Science in Electrical and Computer Engineering **June 2000**

Department of Electrical Engineering, University of Belgrade, Belgrade, Serbia

RELEVANT COURSES

Wireless Communications	Digital Signal Processing	Design of Digital Systems
VLSI Design I/II	Statistical Signal Processing	Computer Systems Architecture
Advanced VLSI Design	Systems for Digital Signal Processing	Computer Aided Design for VLSI
Digital Audio and Video Systems	Digital Image Processing	Power Electronics I/II

WORK EXPERIENCE

CGGVeritas, Houston

Imaging engineer

May 2007 - present

Signal processing, mathematical modelling, and numerical simulations in connection with the analysis, and interpretation of three-dimensional and four-dimensional seismic data. Applying principles and techniques of mathematics and signal processing on sub-salt images in order to determine locations of petroleum and mineral deposits.

Texas Instruments, Dallas

Summer co-op

June – September 2005

ICI cancellation algorithms for 3.9G OFDM DVB-H receiver

Design and implementation of Inter-Carrier Interference (ICI) cancellation/equalization algorithms for high Doppler 3.9G OFDM DVB-H receivers. Register Transfer Level (RTL) design of division-free Minimum Mean Square Error (MMSE) ICI canceller/equalizer is proposed that can be integrated in existing FPGA/ASIC prototype of DVB-H receiver.

Used tools: Matlab (design and performance evaluation of different ICI cancellation schemes), and Mentor Graphics Verilog tool for RTL design.

Summer co-op

May – August 2004

FFT-based chip-level equalizer (CLE) for 3rd generation (3G) mobile receivers

Design and evaluation of FFT-based CLE algorithm for different antenna configurations (single and multiple antennas at the base-station and mobile handset). Fixed-point C code for RTL design is proposed.

Used tools: Matlab and C programming - performance evaluation of proposed algorithm and fixed-point arithmetic precision using System C libraries.

Rice University, Houston

Research assistant in ECE Department

August 2001 – present

1.) *Soft sphere detection with bounded search for high-throughput MIMO OFDM receivers (spring '06 – present, funded by Nokia and NSF)*

Design and implementation of soft sphere detector (SSD) for emerging and future wireless receivers.

Proposed SSD with variable bound per candidate-search level supports four transmit/receive antennas with 16QAM and achieves detection throughput of about 72 Mbps. Soft sphere detector is interfaced with outer LDPC decoder in order to achieve excellent quality of service. The goal is a hardware (ASIC) design of parallel SSDs iteratively interfaced with LDPC decoder targeting hundreds of Mb/s data rates desired for the future MIMO-OFDM downlink receivers. Iterative detection/decoding scheme based on soft sphere detection is also applied in the SC-FDMA uplink receiver (base-station site) for the 3GPP-LTE (3rd Generation Partnership Project Long Term Evolution) standard.

2.) *Low Density Parity Check (LDPC) decoder design for IEEE 802.11n receiver (fall '04 – spring '06, funded by Nokia)*

Design and implementation of layered belief propagation LDPC decoding algorithm that achieves two times faster convergence than conventional standard belief propagation. Proposed decoder is structured – variety of code rates (between 1/2 and 5/6) and codeword sizes (between 648 and 2592) are supported with a single processor core, and it is fully compatible with the IEEE 802.11n standard. The decoding throughput of more than 1GB/s is achieved thanks to the pipelining of layers (component codes). A prototype decoder architecture has been implemented on Xilinx FPGA, and it is also synthesized as an ASIC solution using 0.13-micron CMOS technology.

3.) *Reconfigurable and customizable processor design for channel equalization algorithms in 3G MIMO downlink (spring '03 - spring '04, funded by Nokia and Texas Instruments)*

Design and utilization of flexible application-specific instruction processors (ASIPs) for 3rd generation (3G) mobile handsets. Channel equalization techniques based on iterative Conjugate Gradient (CG) and Least Mean Square (LMS) algorithms are proposed. Processing modifications for slow and fast fading wireless channels are applied in MIMO context (multiple transmit/receive antennas) and implemented on identical high-speed/low-power ASIP. A semi-automatic software-hardware co-design flow is used that allows fast conversion from C/C++ application code to the VHDL and ASIC design of ASIP processor.

Used tools: C/C++ programming (floating/fixed-point performance evaluation), Transport Triggered Architecture (TTA) tools (design-space exploration and VHDL representation of an ASIP processor), Mentor Graphic's ASIC design-flow (gate-level synthesis of ASIP processor using 0.35-micron TSMC CMOS technology).

4.) *VLSI-ASIC design of multi-user detection based on on-line arithmetic (fall '02 - spring '03, funded by AMD and Rice University)*

Design of wireless CDMA multi-user detector in 0.5-micron CMOS technology is proposed. Arithmetic operations (additions and multiplications) are based on the on-line arithmetic principles in order to improve detection speed of mobile users. The chip has been fabricated and fully tested.

Used tools: Magic layout tool for ASIC design.

5.) *Performance of IEEE 802.11b WLAN in emulated mobile channels (summer '02 - fall '02, funded by NSF and Spirent Communications)*

Performed experiments to empirically measure the performance of an IEEE 802.11b system in a broad spectrum of emulated mobile environments. The goal is to contribute to the evolution of currently existing wireless standards by measuring the effects of different wireless channel phenomena on IEEE 802.11b WLAN cards.

COMPUTER SKILLS

- **Computer Systems:** Windows XP, Unix-Linux
- **Programming Languages:** C/C++, VHDL/Verilog, Assembly
- **Engineering Applications:** Matlab/Simulink, Xilinx FPGA Tools, Mentor Graphics ASIC Tools, Magic, ORCAD, LabView, TI Code Composer Studio.

PUBLICATIONS

- **P. Radosavljevic**, and J. R. Cavallaro, “Design of block-structured LDPC codes for iterative receivers with soft sphere detection”, *accepted for publication in the 33rd IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, March-April 2008.
- K. Amiri, **P. Radosavljevic** and J. R. Cavallaro, “Architecture and algorithm for a stochastic soft-output MIMO detector”, in *41st annual IEEE Asilomar Conference on Signals, Systems, and Computers*, November 2007.
- **P. Radosavljevic**, and J. R. Cavallaro, “Probabilistically bounded soft sphere detection for MIMO-OFDM receivers: algorithm and system architecture”, *IEEE Transactions on Circuits and Systems-I: Regular Papers* (submitted in December 2007).
- A de Baynast, **P. Radosavljevic**, J. R. Cavallaro, and V. Stolpmann, “Tight upper bound on convergence rate of LDPC decoding with turbo-schedules”, *IEEE Communications Letter* (submitted in August 2007).
- M. Karkooti, **P. Radosavljevic**, and J. R. Cavallaro, “Configurable LDPC decoder architectures for regular and irregular codes”, *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology (JVSPS)*, accepted for publication, July 2007.
- **P. Radosavljevic**, and J. R. Cavallaro, “Soft sphere detection with bounded search for high-throughput MIMO receivers,” in *40th annual IEEE Asilomar Conference on Signals, Systems, and Computers*, November 2006.
- M. Brogioli, **P. Radosavljevic**, and J. R. Cavallaro, “A general hardware/software co-design methodology for embedded signal processing and multimedia workloads,” in *40th annual IEEE Asilomar Conference on Signals, Systems, and Computers*, November 2006.
- **P. Radosavljevic**, M. Karkooti, A de Baynast, and J. R. Cavallaro, “Tradeoff analysis and architecture design of high throughput irregular LDPC decoders,” *IEEE Transactions on Circuits and Systems-I: Regular Papers*, November 2006.
- **P. Radosavljevic**, A de Baynast, M. Karkooti, and J. R. Cavallaro, “Multi-rate high-throughput LDPC decoder: tradeoff analysis between decoding throughput and area,” in *17th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC)*, September 2006.
- **P. Radosavljevic**, A de Baynast, M. Karkooti, and J. R. Cavallaro, “High-throughput multi-rate LDPC decoder based on architecture-oriented parity check matrices,” in *14th European Signal Processing Conference (EUSIPCO)*, September 2006.
- M. Karkooti, **P. Radosavljevic**, and J. R. Cavallaro, “Configurable high throughput irregular LDPC decoder architecture: tradeoff analysis and implementation,” in *17th IEEE International Conference on Application-specific Systems Architectures and Processors (ASAP)*, September 2006.
- M. Brogioli, **P. Radosavljevic**, and J. R. Cavallaro, “Hardware/software co-design for 3.5G mobile receivers: meeting real-time processing deadlines for HSDPA,” in *IEEE Real-Time and Embedded Technology and Applications Symposium*, August 2006.
- C. K. Sestok, and **P. Radosavljevic**, “Frequency-domain ICI estimation shortening and cancellation in OFDM receivers,” in *IEEE International Symposium on Broadband Multimedia Systems and Broadcasting*, April 2006.
- **P. Radosavljevic**, A. de Baynast, and J. R. Cavallaro, “Optimized message passing schedules for LDPC decoding,” in *39th annual Asilomar Conference on Signals, Systems, and Computers*, November 2005.
- A. de Baynast, **P. Radosavljevic**, J. R. Cavallaro, and A. Sabharwal, “On turbo-schedule for LDPC decoding,” in *43rd annual Allerton Conference on Communication, Control and Computing*, September 2005.
- A de Baynast, **P. Radosavljevic**, and J. R. Cavallaro, “Chip level LMMSE equalizer for multi-user MIMO systems in fast fading environments,” in *IEEE Global Telecommunications Conference (Globecom)*, December 2004.
- **P. Radosavljevic**, J. R. Cavallaro, and A. de Baynast, “ASIP architecture implementation of channel equalization algorithms for MIMO systems in WCDMA downlink,” in *IEEE Vehicular Technology Conference (VTC)*, September 2004.
- C. Steger, **P. Radosavljevic**, and P. Frantz, “Performance of IEEE 802.11b wireless LAN in an emulated mobile channel,” in *IEEE Vehicular Technology Conference (VTC)*, April 2003.

PATENTS

- **P. Radosavljevic**, Kyeong. J Kim, and J. R. Cavallaro, “QRD-QLD searching based sphere detection for emerging MIMO downlink OFDM receivers”, Nokia patent/filed for US patent NC61218US (854.0066.U1(US)), Dec. 2007
- **P. Radosavljevic**, M. Karkooti, A. de Baynast, and J.R. Cavallaro, “Scalable structured high throughput LDPC decoding”, Nokia patent/filed for US patent NC55520US (854.0057.U1 (US)), Oct. 2007.
- **P. Radosavljevic**, M. Karkooti, A. de Baynast, and J.R. Cavallaro, “Novel design of block-structured PCMs for semi-parallel high throughput LDPC decoder, Nokia patent/filed for US patent NC55364US (854.0058.U1 (US)), Oct. 2007.
- **P. Radosavljevic**, A. de Baynast, J.R. Cavallaro, and B. Aazhang, "Fixed point implementation of LMMSE equalizer for multi-user MIMO system based on CG algorithm and vectorial covariance matrix estimation," Nokia patent NC17733, Dec. 2004.

REFERENCES

References are available upon request.

IMMIGRATION STATUS

H-1B: authorized to work in the United States.