ELEC423, VLSI Design II Final Report Spring 1998 Han Kim and Leel Favichia

1. Description of Omnilab Equipment and Interconnection

To test the “Vanilla” 8-Bit ALU, we first had to generate a vector files based on the test vectors we generated in the design phase of the circuit. (IRSIM test vectors) Using the conversion script “convert”, we obtained a “.pin” and “.in” files, which mapped inputs and ouputs of the chip to interface with the stimulus channel and display channel of the Omnilab equipment. For reference, printouts of those two files are attached as next two pages of the report.

Using the printouts of “.pin” and “.in” files, we wired the breadboard according to the pin configuration. We double-checked the correctness of the wiring, then proceeded to the actual testing.

No special hook up or customization was needed; our chip had a separate channels of input and output pins, plus it does not require as external storage device such as DRAMs to check out its functionality. Only correct wiring of the breadboard was required for the hardware setup.

2. Number and Types of Test Vectors

We used three different types of vector files; normal, supplemental, and worst. Each vector file themselves contain many different patterns to test certain functionalities of the chip (ADD, SUB, MULT, OR, NOT, AND, and SHFT).

First file, “normal”, is the test that we have used in the design phase of the circuit. That file contains twelve separate tests to verify functionality of every single operation that “Vanilla” can perform - 2-NOTs, 2-ORs, 2-ANDs, 2-SUBs, ADD, 2-SHTs, and a MULT. We chose those patterns to be test specific functionality (carries inside of the 8-bit adder, many shifts for the multiplier, etc), and believe that they are good enough for covering the functionality of the circuit.

Second file, “supplemental”, contains some additional test vectors to test ADD, SUB, and MULT. functions. These tests are somewhat more stringent (more carries, and addition, etc) than the “normal” test, and test specifically for functionality of adder and multiplier, which is the most complex part of the circuit.

Thired file, “worst”, is basically the “normal” testing pattern with a “worst” condition clock; the two-phase non-overlapping clock in the “normal” is replaced with an overlapping clock, which should worsen some timing issues in some circuits such as shift registers.

We also attached the copies of “.cmd” files from which we generated the test stimulus files in this report.

3. Numbers of Functional Chips

After testing all five chips with three separate tests we described above, we verified that all 5 chips are functional and passed all the logic and speed tests. They all pass in slow speed mode and fast speed mode. Therefore, the yield is 100% in this sample size.

4. Complete Functionality

This chip shows a complete functionality in three tests performed and in the sample size of 5 chips. We can conclude that there was not a problem in design nor in process. There was not any glitches of any sort whatsoever from the output of the chip, and the chip showed a good performance from very low clock speed (1.5MHz) to highest clock speed allowed by the tester (~34mhz).

5. Possible Reasons for Chips to be Non-Functional

None

6. Comparison Results with Irsim Results: Simulation Vs. Fabricated Chip

The actual chip showed same behavior as in irsim simulation. For those output waveforms both in irsim and the tester, we attached them in the report. Basically, the chip behaved in an exact same manner functionality wise. It was outputting the results predicted and verified by irsim during the design phase.

We wanted to do further testing on ADD, and MULT, so we devised another test pattern to specifically test those two functions, and they also work exactly the same as the irsim simulation.

An interesting observation that we made during the simulation is that for “worst” test condition, where we would use overlap clock scheme, instead of non-overclock scheme, for which the device was designed for, is that for the MULT, the irsim shows unknown state for P_OUT1 and P_OUT7. But, in the acutal chip, it outputs a correct state, which is “0” and “1” for P_OUT1 and P_OUT7 respectively. The explanation that we came with that phenomenon is that in logic simulation, when the timing between two overlapping clock got very close (non-existent to be exact), some timing issues in the shift-registers got worse, so that shift-register in simulation might have been trying to ouput both “0” and “1” on the same bus, thus resulting in unkonwn state for those two bits. But, in real situation, the circuit must have resolved those issues, and stronger drive from true data probably overwritten old data, in time for those output to be outputted to the dataout bus. This “worst” test also resulted in good performance up until 34 MHz, which is the limit for the tester. This indicates the robustness in our design, and probably indicate that the actual speed of the circuit is better than 34 MHz.

To check the results from irsim and the actual chip, expected correct outputs are written on the “.cmd” files themselves. We verified that all the outputs match that of “.cmd” solutions and the waveform outputs of the irsim simulation results.

7. Speed Response of the Chip

The chip was placed under varous test speeds to ensure the functionality of the circuit in various frequencies. The chip basically performed flawlessly (no glitches) up until 34 MHz, which is the limit for the Omnilab tester that we were using.

Even on the “worst” condition test, which creates an overlapping clock A and B, the chip functioned flawlessly, which was not expected from the simulation.