```
clock Vdd 1

ana cin x0 y0 asc not0 and0 co0 as0


V x0  0 1 0 1 0 0 1 1

V y0  1 1 0 0 1 0 1 0

V asc 0 0 0 0 1 1 1 1

V cin 0 1 0 0 1 1 0 0

R


| the above command file exerts a certain combination of control signals
| (asc and cin) at each clock cycle to test the different operations of the
| alu; for more information about the signals required for each operation,
| refer to the alu functional description.
```