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M370 71 102 187 2 CMOSN L=2.0U W=3.0U
M371 184 140 0 2 CMOSN L=2.0U W=4.0U
M372 71 185 188 2 CMOSN L=2.0U W=3.0U
M373 188 184 0 2 CMOSN L=2.0U W=3.0U
M374 187 140 0 2 CMOSN L=2.0U W=3.0U
M375 189 0 1 3 CMOSP L=4.0U W=3.0U
M376 189 190 0 2 CMOSN L=2.0U W=3.0U
M377 189 191 0 2 CMOSN L=2.0U W=3.0U
M378 0 192 189 2 CMOSN L=2.0U W=3.0U
M379 193 189 0 2 CMOSN L=2.0U W=3.0U
M380 194 0 1 3 CMOSP L=4.0U W=3.0U
M381 194 190 0 2 CMOSN L=2.0U W=3.0U
M382 0 195 194 2 CMOSN L=2.0U W=3.0U
M383 196 0 1 3 CMOSP L=4.0U W=3.0U
M384 0 197 196 2 CMOSN L=2.0U W=3.0U
M385 198 0 1 3 CMOSP L=4.0U W=3.0U
M386 0 197 198 2 CMOSN L=2.0U W=3.0U
M387 199 0 1 3 CMOSP L=4.0U W=3.0U
M388 200 0 1 3 CMOSP L=4.0U W=3.0U
M389 199 190 0 2 CMOSN L=2.0U W=3.0U
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M390 0 197 200 2 CMOSN L=2.0U W=3.0U
M391 201 0 1 3 CMOSP L=4.0U W=3.0U
M392 0 197 201 2 CMOSN L=2.0U W=3.0U
M393 190 197 0 2 CMOSN L=2.0U W=3.0U
M394 0 192 194 2 CMOSN L=2.0U W=3.0U
M395 0 194 202 2 CMOSN L=2.0U W=3.0U
M396 196 191 0 2 CMOSN L=2.0U W=3.0U
M397 198 191 0 2 CMOSN L=2.0U W=3.0U
M398 196 203 0 2 CMOSN L=2.0U W=3.0U
M399 204 196 0 2 CMOSN L=2.0U W=3.0U
M400 205 196 0 2 CMOSN L=2.0U W=3.0U
M401 206 196 0 2 CMOSN L=2.0U W=3.0U
M402 0 192 198 2 CMOSN L=2.0U W=3.0U
M403 0 195 200 2 CMOSN L=2.0U W=3.0U
M404 0 195 201 2 CMOSN L=2.0U W=3.0U
M405 191 195 0 2 CMOSN L=2.0U W=3.0U
M406 0 198 207 2 CMOSN L=2.0U W=3.0U
M407 0 198 208 2 CMOSN L=2.0U W=3.0U
M408 199 203 0 2 CMOSN L=2.0U W=3.0U
M409 209 199 0 2 CMOSN L=2.0U W=3.0U
M410 0 192 200 2 CMOSN L=2.0U W=3.0U
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M412 0 210 197 2 CMOSN L=2.0U W=3.0U
M413 0 200 205 2 CMOSN L=2.0U W=3.0U
M414 0 200 207 2 CMOSN L=2.0U W=3.0U
M415 209 201 0 2 CMOSN L=2.0U W=3.0U
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M417 205 0 1 3 CMOSP L=4.0U W=4.0U
M418 207 0 1 3 CMOSP L=4.0U W=4.0U
M419 193 0 1 3 CMOSP L=4.0U W=4.0U
M420 202 0 1 3 CMOSP L=4.0U W=4.0U
M421 206 0 1 3 CMOSP L=4.0U W=4.0U
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M423 209 0 1 3 CMOSP L=4.0U W=4.0U
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M425 0 212 192 2 CMOSN L=2.0U W=3.0U
M426 190 197 1 3 CMOSP L=2.0U W=5.0U
M427 191 195 1 3 CMOSP L=2.0U W=5.0U
M428 203 192 1 3 CMOSP L=2.0U W=5.0U
M429 204 1 213 2 CMOSN L=2.0U W=4.0U
M430 205 1 214 2 CMOSN L=2.0U W=4.0U
M431 207 1 215 2 CMOSN L=2.0U W=4.0U
M432 193 1 216 2 CMOSN L=2.0U W=4.0U
M433 202 1 217 2 CMOSN L=2.0U W=4.0U
M434 206 1 218 2 CMOSN L=2.0U W=4.0U
M435 208 1 219 2 CMOSN L=2.0U W=4.0U
M436 209 1 220 2 CMOSN L=2.0U W=4.0U
M437 197 210 1 3 CMOSP L=2.0U W=5.0U
M438 195 211 1 3 CMOSP L=2.0U W=5.0U
M439 192 212 1 3 CMOSP L=2.0U W=5.0U
M440 221 0 210 3 CMOSP L=2.0U W=4.0U
M441 222 0 211 3 CMOSP L=2.0U W=4.0U
M442 223 0 212 3 CMOSP L=2.0U W=4.0U
M443 221 1 210 2 CMOSN L=2.0U W=4.0U
M444 222 1 211 2 CMOSN L=2.0U W=4.0U
M445 223 1 212 2 CMOSN L=2.0U W=4.0U
M446 204 0 213 3 CMOSP L=2.0U W=3.0U
M447 205 0 214 3 CMOSP L=2.0U W=3.0U
M448 207 0 215 3 CMOSP L=2.0U W=3.0U
M449 193 0 216 3 CMOSP L=2.0U W=3.0U
M450 202 0 217 3 CMOSP L=2.0U W=3.0U
M451 206 0 218 3 CMOSP L=2.0U W=3.0U
M452 208 0 219 3 CMOSP L=2.0U W=3.0U
M453 209 0 220 3 CMOSP L=2.0U W=3.0U
M454 107 214 1 3 CMOSP L=2.0U W=3.0U
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M456 106 213 0 2 CMOSN L=2.0U W=3.0U
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M458 1 215 102 3 CMOSP L=2.0U W=3.0U
M459 102 215 0 2 CMOSN L=2.0U W=3.0U
M460 107 214 0 2 CMOSN L=2.0U W=3.0U
M461 59 218 1 3 CMOSP L=2.0U W=3.0U
M462 1 217 61 3 CMOSP L=2.0U W=3.0U
M463 61 217 0 2 CMOSN L=2.0U W=3.0U
M464 64 216 0 2 CMOSN L=2.0U W=3.0U
M465 53 220 1 3 CMOSP L=2.0U W=3.0U
M466 1 219 56 3 CMOSP L=2.0U W=3.0U
M467 56 219 0 2 CMOSN L=2.0U W=3.0U
M468 59 218 0 2 CMOSN L=2.0U W=3.0U
M469 53 220 0 2 CMOSN L=2.0U W=3.0U
M470 1 106 105 3 CMOSP L=2.0U W=7.0U
M471 105 106 0 2 CMOSN L=2.0U W=4.0U
M472 139 105 160 2 CMOSN L=2.0U W=3.0U
M473 139 106 160 3 CMOSP L=2.0U W=6.0U
M474 160 106 107 2 CMOSN L=2.0U W=3.0U
M475 160 105 107 3 CMOSP L=2.0U W=6.0U
M476 1 107 224 3 CMOSP L=2.0U W=5.0U
M477 1 225 226 3 CMOSP L=2.0U W=4.0U
M478 1 227 225 3 CMOSP L=2.0U W=5.0U
M479 1 224 226 3 CMOSP L=2.0U W=5.0U
M480 226 227 137 3 CMOSP L=2.0U W=5.0U
M481 226 107 137 3 CMOSP L=2.0U W=5.0U
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M483 137 227 228 2 CMOSN L=2.0U W=3.0U
M484 224 107 0 2 CMOSN L=2.0U W=4.0U
M485 137 225 229 2 CMOSN L=2.0U W=3.0U
M486 229 224 0 2 CMOSN L=2.0U W=3.0U
M487 228 107 0 2 CMOSN L=2.0U W=3.0U
M488 230 141 1 3 CMOSP L=2.0U W=4.0U
M489 231 232 230 3 CMOSP L=2.0U W=4.0U
M490 233 234 231 3 CMOSP L=2.0U W=4.0U
M491 1 233 139 3 CMOSP L=2.0U W=7.0U
M492 233 141 0 2 CMOSN L=2.0U W=4.0U
M493 233 232 0 2 CMOSN L=2.0U W=4.0U
M494 233 234 0 2 CMOSN L=2.0U W=4.0U
M495 139 233 0 2 CMOSN L=2.0U W=4.0U
M496 1 107 235 3 CMOSP L=2.0U W=4.0U
M497 1 138 235 3 CMOSP L=2.0U W=4.0U
M498 235 107 236 2 CMOSN L=2.0U W=4.0U
M499 236 138 0 2 CMOSN L=2.0U W=4.0U
M500 1 235 232 3 CMOSP L=2.0U W=7.0U
M501 232 235 0 2 CMOSN L=2.0U W=4.0U
M502 1 107 237 3 CMOSP L=2.0U W=4.0U
M503 1 238 237 3 CMOSP L=2.0U W=4.0U
M504 237 107 239 2 CMOSN L=2.0U W=4.0U
M505 239 238 0 2 CMOSN L=2.0U W=4.0U
M506 1 237 234 3 CMOSP L=2.0U W=7.0U
M507 234 237 0 2 CMOSN L=2.0U W=4.0U
M508 1 238 240 3 CMOSP L=2.0U W=4.0U
M509 1 138 240 3 CMOSP L=2.0U W=4.0U
M510 240 238 241 2 CMOSN L=2.0U W=4.0U
M511 241 138 0 2 CMOSN L=2.0U W=4.0U
M512 1 240 141 3 CMOSP L=2.0U W=7.0U
M513 141 240 0 2 CMOSN L=2.0U W=4.0U
M514 1 238 242 3 CMOSP L=2.0U W=5.0U
M515 1 243 244 3 CMOSP L=2.0U W=4.0U
M516 1 138 243 3 CMOSP L=2.0U W=5.0U
M517 1 242 244 3 CMOSP L=2.0U W=5.0U
M518 244 138 227 3 CMOSP L=2.0U W=5.0U
M519 244 238 227 3 CMOSP L=2.0U W=5.0U
```

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M520 243 138 0 2 CMOSN L=2.0U W=4.0U
M521 227 138 245 2 CMOSN L=2.0U W=3.0U
M522 242 238 0 2 CMOSN L=2.0U W=4.0U
M523 227 243 246 2 CMOSN L=2.0U W=3.0U
M524 246 242 0 2 CMOSN L=2.0U W=3.0U
M525 245 238 0 2 CMOSN L=2.0U W=3.0U
M526 1 156 247 3 CMOSP L=2.0U W=5.0U
M527 1 248 249 3 CMOSP L=2.0U W=4.0U
M528 1 102 248 3 CMOSP L=2.0U W=5.0U
M529 1 247 249 3 CMOSP L=2.0U W=5.0U
M530 249 102 138 3 CMOSP L=2.0U W=5.0U
M531 249 156 138 3 CMOSP L=2.0U W=5.0U
M532 248 102 0 2 CMOSN L=2.0U W=4.0U
M533 138 102 250 2 CMOSN L=2.0U W=3.0U
M534 247 156 0 2 CMOSN L=2.0U W=4.0U
M535 138 248 251 2 CMOSN L=2.0U W=3.0U
M536 251 247 0 2 CMOSN L=2.0U W=3.0U
M537 250 156 0 2 CMOSN L=2.0U W=3.0U
C538 74 1 13.0F
C539 102 1 31.0F
C540 249 0 89.0F
C541 248 0 53.0F
C542 102 0 254.0F
C543 247 0 86.0F
C544 156 0 108.0F
C545 227 0 107.0F
C546 244 0 89.0F
C547 243 0 53.0F
C548 138 0 204.0F
C549 242 0 86.0F
C550 238 0 81.0F
C551 1 0 4672.0F
C552 240 0 52.0F
C553 237 0 52.0F
C554 235 0 52.0F
C555 233 0 79.0F
C556 230 0 13.0F
C557 234 0 42.0F
C558 232 0 47.0F
C559 141 0 104.0F
C560 137 0 142.0F
C561 226 0 88.0F
C562 225 0 52.0F
C563 224 0 88.0F
C564 107 0 336.0F
C565 106 0 133.0F
C566 160 0 124.0F
C567 139 0 150.0F
C568 105 0 95.0F
C569 56 0 90.0F
C570 53 0 96.0F
C571 61 0 91.0F
C572 59 0 87.0F
C573 64 0 89.0F
C574 220 0 68.0F
C575 219 0 100.0F
C576 218 0 68.0F
C577 217 0 100.0F
C578 216 0 68.0F
C579 215 0 100.0F
C580 223 0 31.0F
C581 222 0 30.0F
C582 221 0 31.0F
C583 214 0 68.0F
C584 213 0 100.0F
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C585 212 0 39.0F
C586 211 0 39.0F
C587 210 0 39.0F
C588 209 0 87.0F
C589 208 0 69.0F
C590 207 0 81.0F
C591 203 0 45.0F
C592 206 0 75.0F
C593 205 0 87.0F
C594 204 0 68.0F
C595 202 0 69.0F
C596 201 0 60.0F
C597 200 0 62.0F
C598 199 0 60.0F
C599 198 0 57.0F
C600 197 0 49.0F
C601 196 0 67.0F
C602 195 0 52.0F
C603 194 0 54.0F
C604 193 0 75.0F
C605 192 0 53.0F
C606 191 0 48.0F
C607 190 0 48.0F
C608 189 0 53.0F
C609 186 0 89.0F
C610 185 0 53.0F
C611 184 0 86.0F
C612 140 0 201.0F
C613 164 0 107.0F
C614 181 0 89.0F
C615 180 0 53.0F
C616 71 0 211.0F
C617 179 0 86.0F
C618 175 0 81.0F
C619 177 0 52.0F
C620 174 0 52.0F
C621 172 0 52.0F
C622 72 0 152.0F
C623 170 0 79.0F
C624 167 0 13.0F
C625 171 0 42.0F
C626 169 0 47.0F
C627 74 0 106.0F
C628 70 0 140.0F
C629 163 0 88.0F
C630 162 0 52.0F
C631 161 0 87.0F
C632 108 0 132.0F
C633 159 0 21.0F
C634 158 0 11.0F
C635 157 0 63.0F
C636 155 0 53.0F
C637 154 0 58.0F
C638 153 0 45.0F
C639 32 0 284.0F
C640 152 0 53.0F
C641 151 0 58.0F
C642 150 0 45.0F
C643 25 0 270.0F
C644 149 0 53.0F
C645 148 0 58.0F
C646 147 0 45.0F
C647 18 0 261.0F
C648 68 0 164.0F
C649 146 0 53.0F
```

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C650 144 0 58.0F
C651 142 0 45.0F
C652 7 0 249.0F
C653 145 0 107.0F
C654 143 0 102.0F
C655 43 0 217.0F
C656 134 0 89.0F
C657 133 0 53.0F
C658 132 0 86.0F
C659 73 0 195.0F
C660 112 0 107.0F
C661 129 0 89.0F
C662 128 0 53.0F
C663 66 0 216.0F
C664 127 0 86.0F
C665 123 0 100.0F
C666 125 0 52.0F
C667 122 0 52.0F
C668 120 0 52.0F
C669 118 0 79.0F
C670 115 0 13.0F
C671 119 0 42.0F
C672 117 0 47.0F
C673 69 0 101.0F
C674 65 0 149.0F
C675 111 0 88.0F
C676 110 0 52.0F
C677 109 0 87.0F
C678 75 0 124.0F
C679 67 0 152.0F
C680 101 0 89.0F
C681 100 0 53.0F
C682 99 0 86.0F
C683 79 0 107.0F
C684 96 0 89.0F
C685 95 0 53.0F
C686 55 0 194.0F
C687 94 0 86.0F
C688 90 0 97.0F
C689 92 0 52.0F
C690 89 0 52.0F
C691 87 0 52.0F
C692 58 0 111.0F
C693 85 0 79.0F
C694 82 0 13.0F
C695 86 0 42.0F
C696 84 0 47.0F
C697 63 0 104.0F
C698 52 0 129.0F
C699 78 0 88.0F
C700 77 0 52.0F
C701 76 0 87.0F
C702 46 0 210.0F
C703 62 0 81.0F
C704 60 0 81.0F
C705 57 0 80.0F
C706 54 0 80.0F
C707 51 0 80.0F
C708 50 0 220.0F
C709 10 0 89.0F
C710 49 0 31.0F
C711 48 0 222.0F
C712 47 0 32.0F
C713 27 0 85.0F
C714 45 0 32.0F
```

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C715 42 0 35.0F
C716 44 0 54.0F
C717 41 0 70.0F
C718 39 0 20.0F
C719 38 0 176.0F
C720 37 0 67.0F
C721 36 0 35.0F
C722 35 0 91.0F
C723 33 0 45.0F
C724 34 0 93.0F
C725 31 0 56.0F
C726 29 0 36.0F
C727 28 0 91.0F
C728 26 0 45.0F
C729 24 0 56.0F
C730 22 0 35.0F
C731 21 0 91.0F
C732 19 0 45.0F
C733 20 0 87.0F
C734 17 0 56.0F
C735 15 0 46.0F
C736 13 0 35.0F
C737 12 0 91.0F
C738 8 0 45.0F
C739 14 0 77.0F
C740 11 0 123.0F
C741 9 0 102.0F
C742 6 0 56.0F
C743 4 0 88.0F
*  GND  0
*  Vdd  1
*  NMOS 2
*  PMOS 3
*  CMOSN        2
*  CMOSP        3
*  clearacc     4
*  j_pclatch_0/j_pcbit_3/norhell_0/6_13_14#     5
*  j_pclatch_0/j_pcbit_3/6_58_27#       6
*  b3   7
*  j_pclatch_0/j_pcbit_3/6_4_15#        8
*  j_pclatch_0/j_pcbit_3/storebar       9
*  in3  10
*  j_pclatch_0/store    11
*  j_pclatch_0/j_pcbit_3/6_168_28#      12
*  tout3        13
*  j_pclatch_0/j_pcbit_3/enaccbar       14
*  enacc        15
*  j_pclatch_0/j_pcbit_2/norhell_0/6_13_14#     16
*  j_pclatch_0/j_pcbit_2/6_58_27#       17
*  b2   18
*  j_pclatch_0/j_pcbit_2/6_4_15#        19
*  in2  20
*  j_pclatch_0/j_pcbit_2/6_168_28#      21
*  tout2        22
*  j_pclatch_0/j_pcbit_1/norhell_0/6_13_14#     23
*  j_pclatch_0/j_pcbit_1/6_58_27#       24
*  b1   25
*  j_pclatch_0/j_pcbit_1/6_4_15#        26
*  in1  27
*  j_pclatch_0/j_pcbit_1/6_168_28#      28
*  tout1        29
*  j_pclatch_0/j_pcbit_0/norhell_0/6_13_14#     30
*  j_pclatch_0/j_pcbit_0/6_58_27#       31
*  b0   32
*  j_pclatch_0/j_pcbit_0/6_4_15#        33
```

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*  in0  34
*  j_pclatch_0/j_pcbit_0/6_168_28#      35
*  tout0        36
*  j_pclatch_0/j_pccontrol_0/NAND_OUT   37
*  clka 38
*  ldacc        39
*  j_pclatch_0/j_pccontrol_0/6_90_81#   40
*  readalu      41
*  bus0 42
*  out0 43
*  readbus      44
*  bus1 45
*  out1 46
*  bus2 47
*  out2 48
*  bus3 49
*  out3 50
*  assigbar     51
*  as3  52
*  assig        53
*  jgate_8/passbar      54
*  not3 55
*  notsig       56
*  jgate_7/passbar      57
*  co3  58
*  orsig        59
*  jgate_3/passbar      60
*  srsig        61
*  jgate_2/passbar      62
*  and3 63
*  andsig       64
*  as2  65
*  not2 66
*  co2  67
*  y3   68
*  and2 69
*  as1  70
*  not1 71
*  co1  72
*  y2   73
*  and1 74
*  cin3 75
*  all_3/abar   76
*  all_3/bbar   77
*  all_3/xor2_0/6_58_35#        78
*  xor3 79
*  all_3/xor2_0/6_46_85#        80
*  all_3/xor2_0/6_128_79#       81
*  all_3/or3_0/6_11_11# 82
*  all_3/or3_0/6_8_11#  83
*  all_3/or3_0/b        84
*  all_3/or3_0/6_39_47# 85
*  all_3/or3_0/c        86
*  all_3/r_and_0/r_nand_0/NAND_OUT      87
*  all_3/r_and_0/r_nand_0/6_45_5#       88
*  all_3/and_1/nand_0/NAND_OUT  89
*  x3   90
*  all_3/and_1/nand_0/6_45_5#   91
*  all_3/and_0/nand_0/NAND_OUT  92
*  all_3/and_0/nand_0/6_45_5#   93
*  all_3/xor_1/ABAR     94
*  all_3/xor_1/BBAR     95
*  all_3/xor_1/6_27_28# 96
*  all_3/xor_1/6_39_23# 97
*  all_3/xor_1/6_44_17# 98
```

```
*  all_3/xor_0/ABAR     99
*  all_3/xor_0/BBAR     100
*  all_3/xor_0/6_27_28# 101
*  asc  102
*  all_3/xor_0/6_39_23# 103
*  all_3/xor_0/6_44_17# 104
*  mux_2/pickabar       105
*  path 106
*  carry        107
*  cin2 108
*  all_2/abar   109
*  all_2/bbar   110
*  all_2/xor2_0/6_58_35#        111
*  xor2 112
*  all_2/xor2_0/6_46_85#        113
*  all_2/xor2_0/6_128_79#       114
*  all_2/or3_0/6_11_11# 115
*  all_2/or3_0/6_8_11#  116
*  all_2/or3_0/b        117
*  all_2/or3_0/6_39_47# 118
*  all_2/or3_0/c        119
*  all_2/r_and_0/r_nand_0/NAND_OUT      120
*  all_2/r_and_0/r_nand_0/6_45_5#       121
*  all_2/and_1/nand_0/NAND_OUT  122
*  x2   123
*  all_2/and_1/nand_0/6_45_5#   124
*  all_2/and_0/nand_0/NAND_OUT  125
*  all_2/and_0/nand_0/6_45_5#   126
*  all_2/xor_1/ABAR     127
*  all_2/xor_1/BBAR     128
*  all_2/xor_1/6_27_28# 129
*  all_2/xor_1/6_39_23# 130
*  all_2/xor_1/6_44_17# 131
*  all_2/xor_0/ABAR     132
*  all_2/xor_0/BBAR     133
*  all_2/xor_0/6_27_28# 134
*  all_2/xor_0/6_39_23# 135
*  all_2/xor_0/6_44_17# 136
*  as0  137
*  not0 138
*  conot        139
*  y1   140
*  and0 141
*  j_buff_0/j_latch_3/6_6_35#   142
*  j_buff_0/j_latch_3/storebar  143
*  j_buff_0/j_latch_3/6_22_31#  144
*  j_buff_0/j_latch_3/store     145
*  j_buff_0/j_latch_3/6_58_35#  146
*  j_buff_0/j_latch_2/6_6_35#   147
*  j_buff_0/j_latch_2/6_22_31#  148
*  j_buff_0/j_latch_2/6_58_35#  149
*  j_buff_0/j_latch_1/6_6_35#   150
*  j_buff_0/j_latch_1/6_22_31#  151
*  j_buff_0/j_latch_1/6_58_35#  152
*  j_buff_0/j_latch_0/6_6_35#   153
*  j_buff_0/j_latch_0/6_22_31#  154
*  j_buff_0/j_latch_0/6_58_35#  155
*  y0   156
*  j_buff_0/j_control_0/6_138_176#      157
*  j_buff_0/j_control_0/6_242_208#      158
*  buffread     159
*  cin1 160
*  all_1/abar   161
*  all_1/bbar   162
*  all_1/xor2_0/6_58_35#        163
```

```
*  xor1 164
*  all_1/xor2_0/6_46_85#        165
*  all_1/xor2_0/6_128_79#       166
*  all_1/or3_0/6_11_11# 167
*  all_1/or3_0/6_8_11#  168
*  all_1/or3_0/b        169
*  all_1/or3_0/6_39_47# 170
*  all_1/or3_0/c        171
*  all_1/r_and_0/r_nand_0/NAND_OUT      172
*  all_1/r_and_0/r_nand_0/6_45_5#       173
*  all_1/and_1/nand_0/NAND_OUT  174
*  x1   175
*  all_1/and_1/nand_0/6_45_5#   176
*  all_1/and_0/nand_0/NAND_OUT  177
*  all_1/and_0/nand_0/6_45_5#   178
*  all_1/xor_1/ABAR     179
*  all_1/xor_1/BBAR     180
*  all_1/xor_1/6_27_28# 181
*  all_1/xor_1/6_39_23# 182
*  all_1/xor_1/6_44_17# 183
*  all_1/xor_0/ABAR     184
*  all_1/xor_0/BBAR     185
*  all_1/xor_0/6_27_28# 186
*  all_1/xor_0/6_39_23# 187
*  all_1/xor_0/6_44_17# 188
*  decoden_0/6_44_11#   189
*  decoden_0/6_88_145#  190
*  decoden_0/6_120_145# 191
*  decoden_0/6_144_187# 192
*  decoden_0/6_256_271# 193
*  decoden_0/6_44_27#   194
*  decoden_0/6_112_187# 195
*  decoden_0/6_44_43#   196
*  decoden_0/6_80_187#  197
*  decoden_0/6_44_59#   198
*  decoden_0/6_44_75#   199
*  decoden_0/6_44_91#   200
*  decoden_0/6_44_107#  201
*  decoden_0/6_276_323# 202
*  decoden_0/6_152_145# 203
*  decoden_0/6_212_323# 204
*  decoden_0/6_224_271# 205
*  decoden_0/6_288_271# 206
*  decoden_0/6_244_323# 207
*  decoden_0/6_308_323# 208
*  decoden_0/6_320_271# 209
*  decoden_0/6_74_279#  210
*  decoden_0/6_106_279# 211
*  decoden_0/6_138_279# 212
*  decoden_0/6_208_465# 213
*  decoden_0/6_222_489# 214
*  decoden_0/6_240_465# 215
*  decoden_0/6_254_489# 216
*  decoden_0/6_272_465# 217
*  decoden_0/6_286_489# 218
*  decoden_0/6_304_465# 219
*  decoden_0/6_318_489# 220
*  msb  221
*  mid  222
*  lsb  223
*  abar 224
*  bbar 225
*  midxor       226
*  xor0 227
*  all_0/xor2_0/6_46_85#        228
```

```
*  all_0/xor2_0/6_128_79#       229
*  all_0/or3_0/6_11_11# 230
*  all_0/or3_0/6_8_11#  231
*  all_0/or3_0/b        232
*  all_0/or3_0/6_39_47# 233
*  all_0/or3_0/c        234
*  all_0/r_and_0/r_nand_0/NAND_OUT      235
*  all_0/r_and_0/r_nand_0/6_45_5#       236
*  all_0/and_1/nand_0/NAND_OUT  237
*  x0   238
*  all_0/and_1/nand_0/6_45_5#   239
*  all_0/and_0/nand_0/NAND_OUT  240
*  all_0/and_0/nand_0/6_45_5#   241
*  all_0/xor_1/ABAR     242
*  all_0/xor_1/BBAR     243
*  all_0/xor_1/6_27_28# 244
*  all_0/xor_1/6_39_23# 245
*  all_0/xor_1/6_44_17# 246
*  all_0/xor_0/ABAR     247
*  all_0/xor_0/BBAR     248
*  all_0/xor_0/6_27_28# 249
*  all_0/xor_0/6_39_23# 250
*  all_0/xor_0/6_44_17# 251
.MODEL CMOSN NMOS LEVEL=2 LD=0.240703U TOX=407.000000E-10
+ NSUB=3.133604E+15 VTO=0.711043 KP=4.879000E-05 GAMMA=0.3801
+ PHI=0.6 UO=575.027 UEXP=0.129885 UCRIT=24726.9
+ DELTA=0.82016 VMAX=63588.7 XJ=0.250000U LAMBDA=2.474695E-02
+ NFS=6.455307E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=29.040000 CGDO=3.063325E-10 CGSO=3.063325E-10 CGBO=5.135289E-10
+ CJ=1.130300E-04 MJ=0.699680 CJSW=5.235300E-10 MJSW=0.263078 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.60 um
.MODEL CMOSP PMOS LEVEL=2 LD=0.250000U TOX=407.000000E-10
+ NSUB=6.222000E+15 VTO=-0.80612 KP=2.113000E-05 GAMMA=0.5357
+ PHI=0.6 UO=249.519 UEXP=0.226251 UCRIT=18368.3
+ DELTA=1.75689 VMAX=40684.7 XJ=0.250000U LAMBDA=5.307119E-02
+ NFS=3.574015E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=87.160000 CGDO=3.181644E-10 CGSO=3.181644E-10 CGBO=6.682147E-10
+ CJ=2.493100E-04 MJ=0.551790 CJSW=2.815500E-10 MJSW=0.311229 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.04 um
*
* From N13L  SPICE LEVEL 2 PARAMETERS   1991 nwell
*
* so far, b3 is longest.
*  vlsi project - find longest path in alu
* 12/11/97

*  Set BASIC VOLTAGE levels
*vdd <Vdd> <GND>  dc 5
vdd 1     0      dc 5
*  set substrate voltages : P-sub = Vdd;  N-sub = GND
*vs1 <CMOSP> <Vdd>  dc 0
vs1 3       1      dc 0
*vs2 <CMOSN> <GND>  dc 0
vs2 2       0      dc 0

*  -----------------------------------

*  Set other constant circuit inputs, for example b, cin:
*  None here.
*vxo  <x1> <GND> dc 0
vxo  175  0     dc 0
*vxt  <x2> <GND> dc 0
vxt  123  0     dc 0
```

```
*vxth  <x3> <GND> dc 0
vxth  90   0     dc 0

*vyz <y0> <GND> dc 5
vyz 156  0     dc 5
*vyo <y1> <GND> dc 5
vyo 140  0     dc 5
*vyt <y2> <GND> dc 5
vyt 73   0     dc 5
*vyth <y3> <GND> dc 5
vyth 68   0     dc 5

*virz <lsb> <GND> dc 0
virz 223   0     dc 0
*viro <mid> <GND> dc 5
viro 222   0     dc 5
*virt <msb> <GND> dc 0
virt 221   0     dc 0

*vclk <clka> <GND> dc 5
vclk 38     0     dc 5

*vrbus <readbus> <GND> dc 0
vrbus 44        0     dc 0
*vralu <readalu> <GND> dc 5
vralu 41        0     dc 5
*vcl <clearacc> <GND> dc 0
vcl 4          0     dc 0
*vld <ldacc> <GND> dc 5
vld 39      0     dc 5
*ven <enacc> <GND> dc 0
ven 15      0     dc 0
*vbr <buffread> <GND> dc 0
vbr 159        0     dc 0


*  ------------------------------------

*  Set Circuit Input which will change, for example a:
*  input pulse between node and GND (initially 0 ) of:
*  pulse (init_value pulse_value delay rise_time fall_time pulse_width period)
*vxz <x0> <GND> 0 pulse(0 5 0ns 0.1ns 0.1ns 10000ns 10ns)
vxz 238  0     0 pulse(0 5 0ns 0.1ns 0.1ns 10000ns 10ns)


*  ------------------------------------



*  Do analysis: give increments and total time for analysis.
.tran .1ns 50ns

*  If running in batch mode spice -b, then ascii plots are made
*  Plot Voltages
*.plot tran v(<y0>) v(<x0>) v(<b0>) v(<b1>) v(<b2>) v(<b3>) v(<co3>)
.plot tran v(156)  v(238)  v(32)   v(25)   v(18)   v(7)    v(58)

*  set hcopydevtype=postscript

.end
```