```
clock CLKA 0 1 0 0
vector op msb mid lsb
vector x x3 x2 x1 x0
vector bus bus3 bus2 bus1 bus0
vector tout tout3 tout2 tout1 tout0
vector aluout out3 out2 out1 out0
vector y y3 y2 y1 y0
vector as as3 as2 as1 as0
vector in in3 in2 in1 in0
vector b b3 b2 b1 b0


ana clka op  x y  b tout b readbus readalu ldacc buffread enacc


V bus 0110

V op 000 000 000 001 001 001 001 001 010 010 010 011 011 011 100 100 100
101 101 101

V x 0010 0010 0010 0010 1101 1101 1101 1101

V clearacc      1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

V readbus       0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

V readalu       1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 0

V ldacc         0 1 0 1 0 1 0 1 0 1 0 1 0

V buffread      1 0 1 0 1 0 1 0 1 0 1 0 1

V enacc         1

R

| Operations Performed (in order): addx, and, addi, srl, or, not

|For simplicity, the accumulator reads only from the alu
```