```
clock Vdd 1

vector op msb mid lsb

ana op path carry asc and sr or not addsub

V op 000 001 010 011 100 101 110 111

R


| Meaning of Opcodes in Order Asserted:
  000   addx
  001   and
  010   addi
  011   srl
  100   or
  101   not
  110   add
```