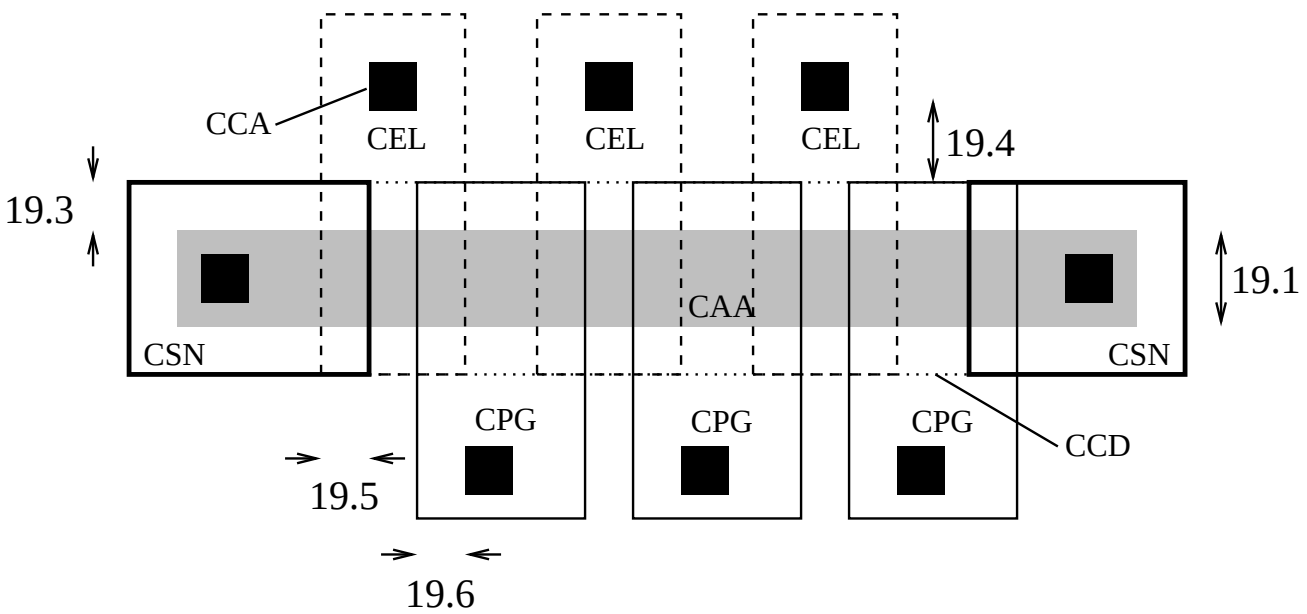
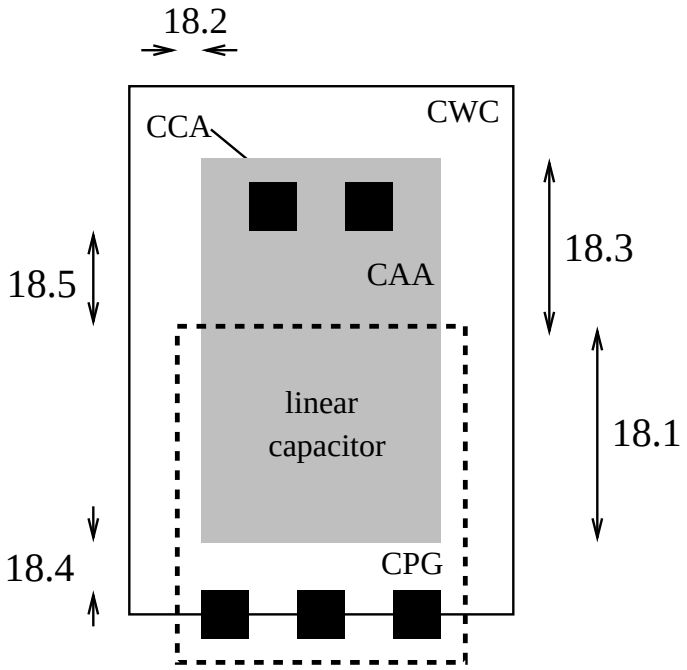
A.19 Buried Channel CCD - (CCD)

19.1	Minimum CCD channel width	4
19.2	Minimum CCD channel spacing	4
19.3	Minimum CCD implant overlap of **channel**	2
19.4	Minimum **contact** to CCD implant	3
19.5	Minimum **select** overlap of **electrode** or **poly**	2
19.6	Minimum **poly/electrode** overlap within **channel**	2



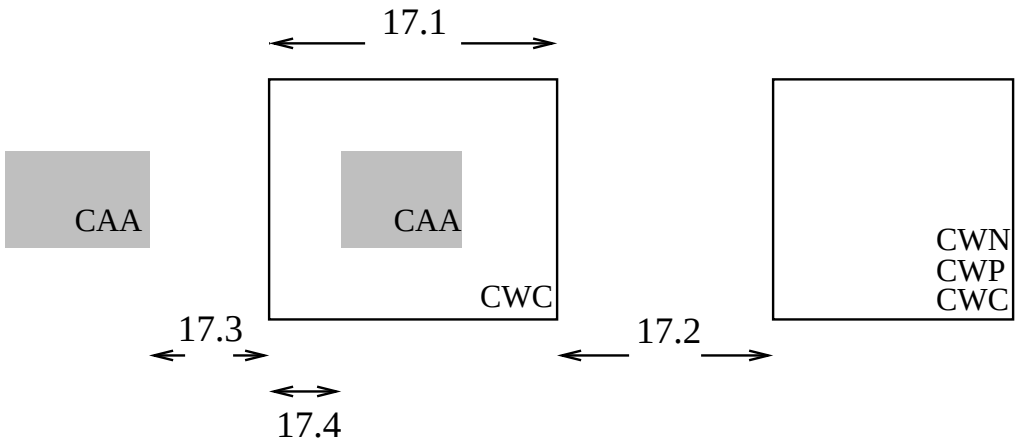
A.18 Linear capacitors

18.1	Minimum width	3
18.2	Minimum **poly** overhang of **active**	1
18.3	Minimum **active** overlap of **poly**	3
18.4	Minimum **poly contact** to **active**	2
18.5	Minimum **active contact** to **poly**	4



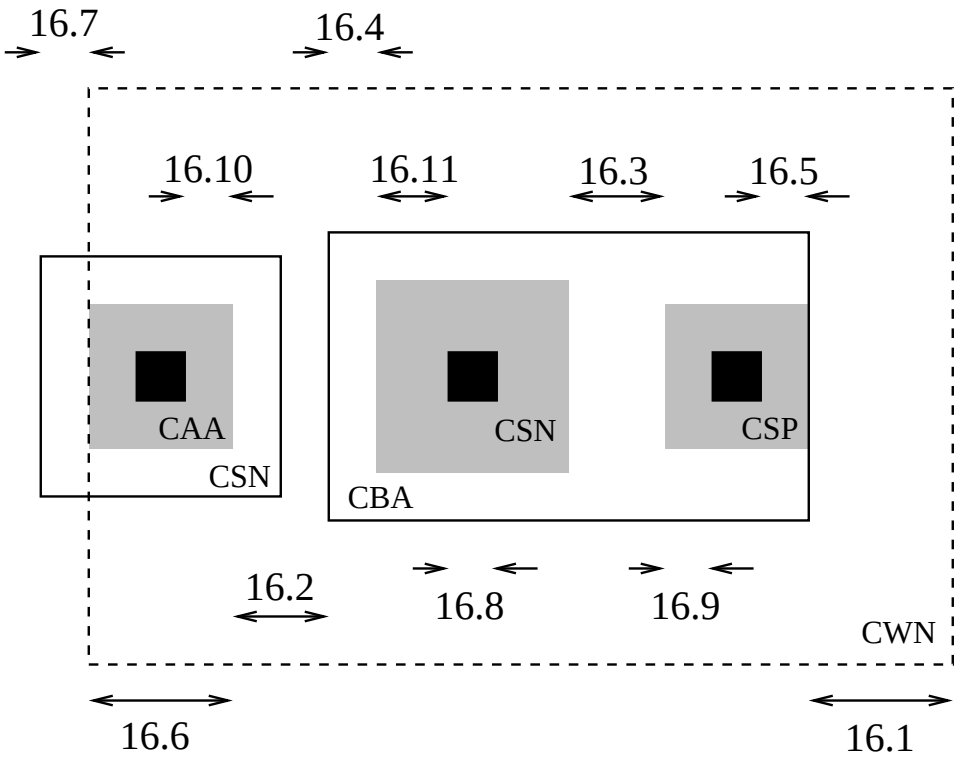
A.17 Capacitor well - (CWC)

17.1	Minimum width	10
17.2	Minimum spacing	9
17.3	Minimum spacing to external **active**	5
17.4	Minimum overlap of **active**	3



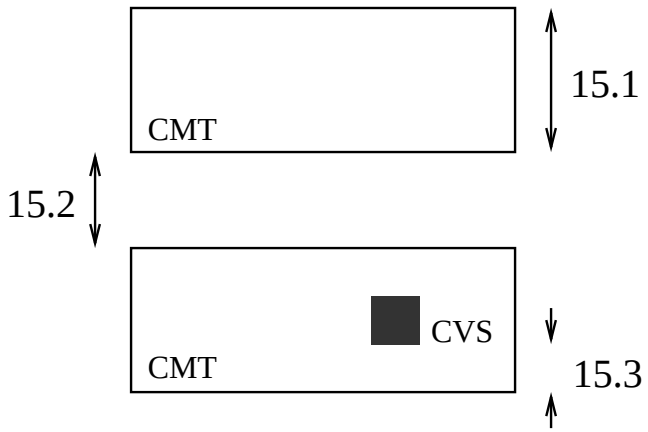
A.16 NPN Bipolar Transistor - (CBA)

16.1	Minimum **nwell** overlap of **pbase**	6
16.2	Minimum spacing between **pbase** and external **active**	4
16.3	Minimum spacing between opposite select within **pbase**	4
16.4	**Pbase** overlap of **N-select**	2
16.5	Minimum **base contact** to **pbase**	2
16.6	Minimum **active** width for collector	6
16.7	Minimum **select** overlap of **active** for collector	2
16.8	Contact of all **active**	2×2
16.9	P-select ovelap of base contact	2
16.10	Active overlap of collector contact	2
16.11	Select overlap of emitter contact	3



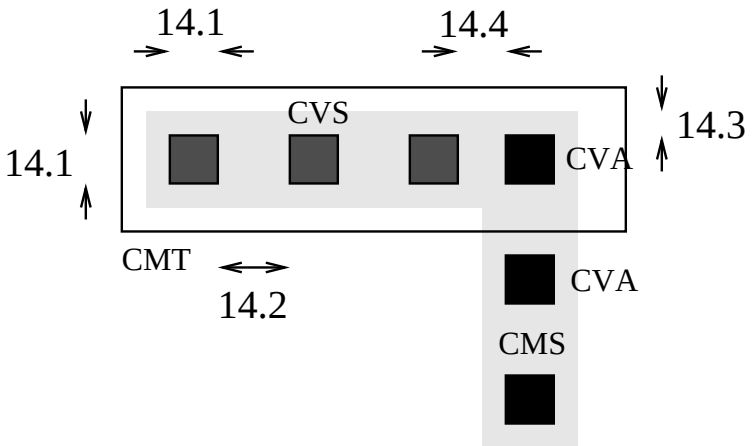
A.15 Metal3 - (CMT)

15.1	Minimum width	6
15.2	Minimum spacing to **metal3**	4
15.3	Minimum overlap of **via2**	2



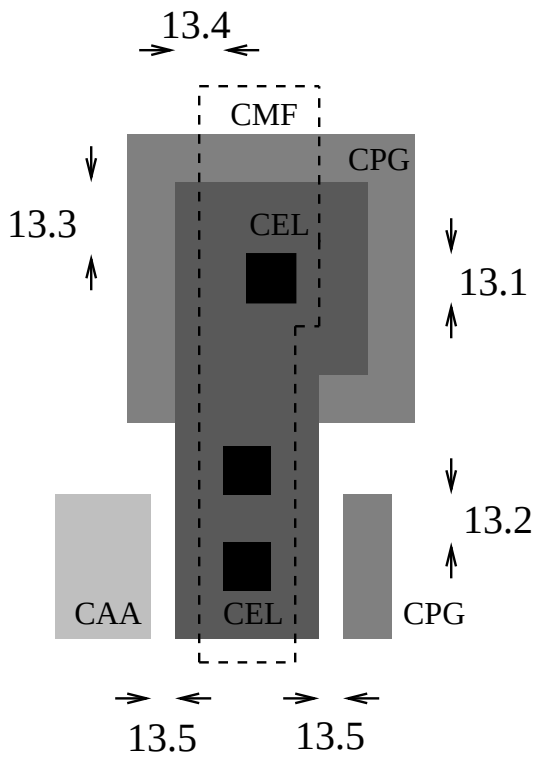
A.14 Via2 - (CVS)

14.1	Exact size	2×2
14.2	Minimu spacing	3
14.3	Minimum overlap by **metal2**	1
14.4	Minimum spacing to **via1**	2



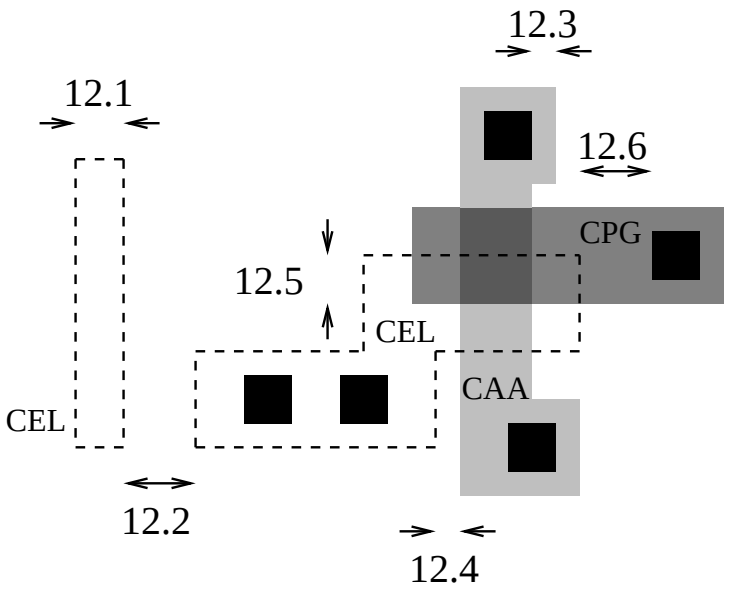
A.13 Electrode Contact - (CCE)

13.1	Exact contact size	2×2
13.2	Minimum spacing	2
13.3	Minimum **electrode** overlap (on capacitor)	3
13.4	Minimum **electrode** overlap (not on capacitor)	2
13.5	Minimum spacing to **poly** or **active**	3



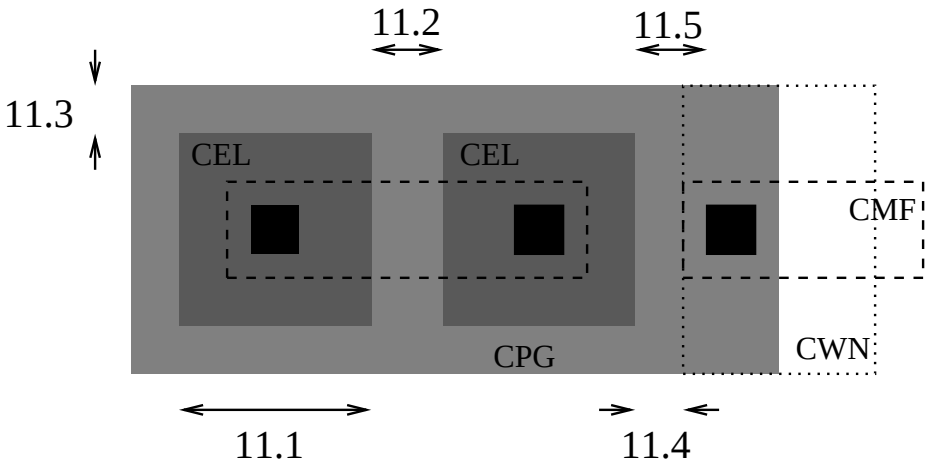
A.12 Electrode for Transistor - (CEL)

12.1	Minimum width	2
12.2	Minimum spacing	3
12.3	Minimum **electrode** gate overlap of **active**	2
12.4	Minimum spacing to **active**	1
12.5	Minimum spacing or overlap of **poly**	2
12.4	Minimum spacing to poly or active **contact**	3



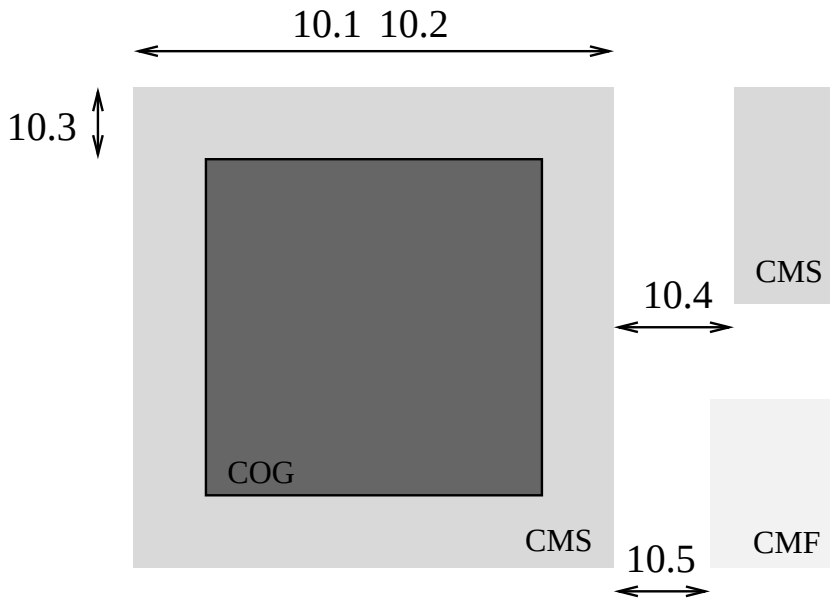
A.11 Electrode for Capacitor - (CEL)

11.1	Minimum width	3
11.2	Minimum spacing	3
11.3	Minimum **poly** overlap	2
11.4	Minimum spacing to **active** edge or **well** edge	2
11.5	Minimum spacing to **poly contact**	3



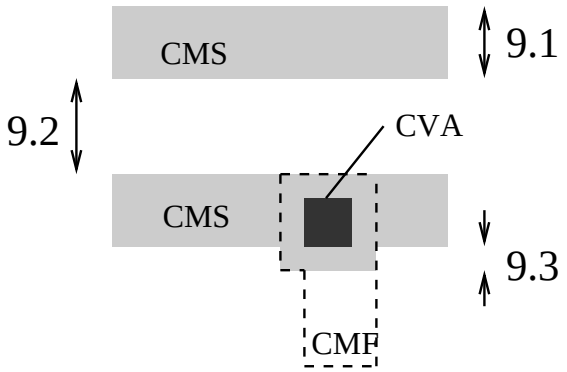
A.10 Overglass - (COG)

		microns
10.1	Bonding pad	100 × 100
10.2	Probe pad	75 × 75
10.3	Pad overlap of **glass**	6
10.4	Minimum pad spacing to unrelated **metal2**	30
10.5	Minimum pad spacing to unrelated **metal1, poly**, **electrode** or **active**	15



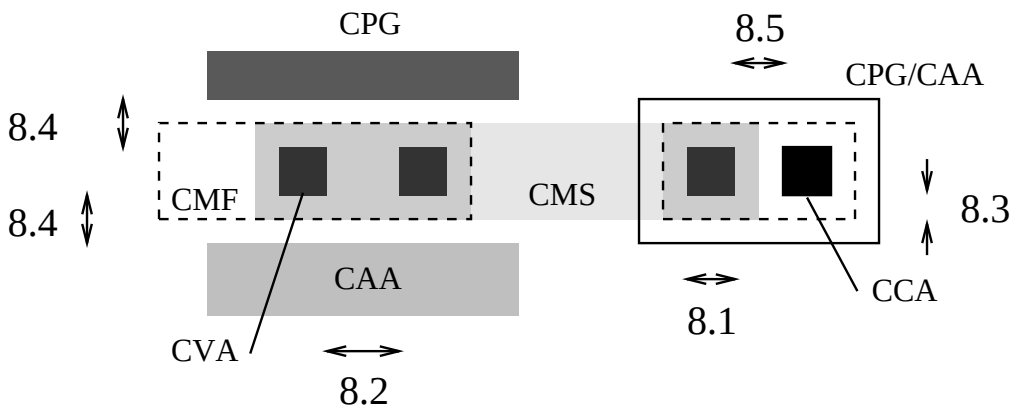
A.9 Metal2 - (CMS)

9.1	Minimum width	3
9.2	Minimum spacing	4
9.3	Minimum overlap of **via1**	1



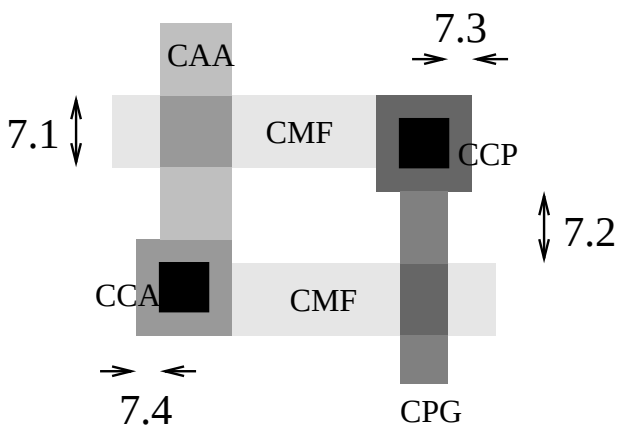
A.8 Via1 - (CVA)

8.1	Exact size	2×2
8.2	Minimum spacing 3	
8.3	Minimum overlap by **metal1**	1
8.4	Minimum spacing to **poly** or **active** edge	2
8.5	Minimum spacing to **contact**	2

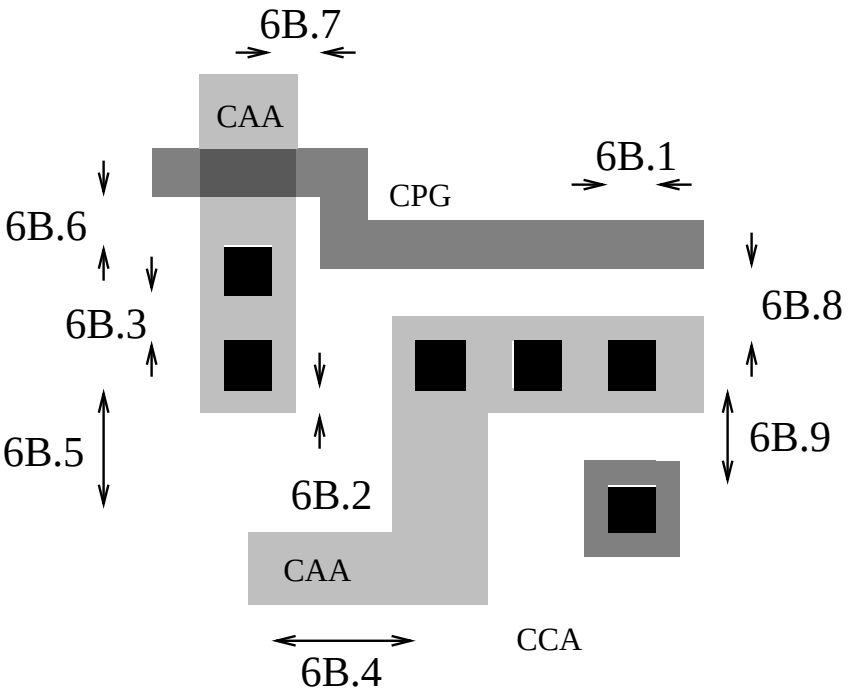


A.7 Metal1 - (CMF)

7.1	Minimum width	3
7.2	Minimum spacing	3
7.3	Minimum overlap by **poly**	1
7.4	Minimum overlap by **active**	1

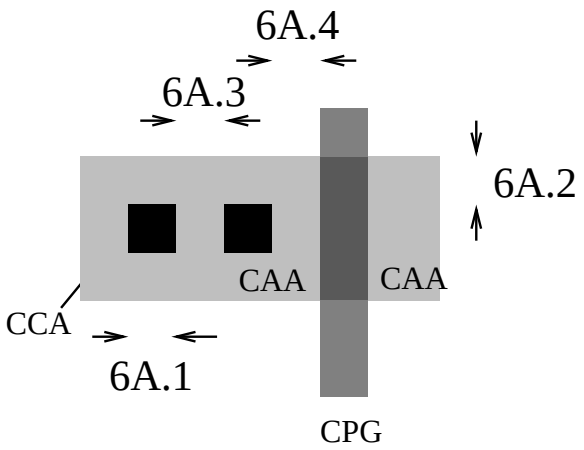


6B.1	Exact **contact** size	2×2
6B.2	Minimum **active** overlap	1
6B.3	Minimum spacing on same **active**	2
6B.4	Minimum spacing on different **active**	6
6B.5	Minimum spacing to diffusion **active**	5
6B.6	Minimum spacing to **channel**	2
6B.7	Minimum sapcing to field **poly** (one contact)	2
6B.8	Minimum sapcing to field **poly** (many contacts)	3
6B.9	Minimum spacing to **poly contact**	4

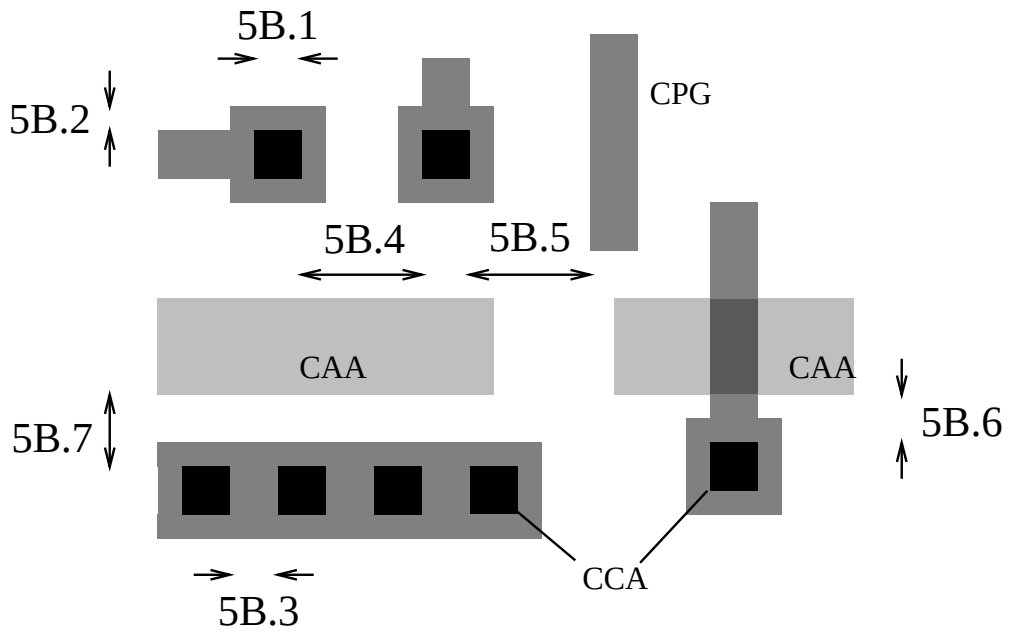


A.6 Contact to Active - (CCA)

6A.1 Exact **contact** size	2×2
6A.2 Minimum **active** overlap	2
6A.3 Minimum spacing	2
6A.4 Minimum spacing to **channel** of transistor	2

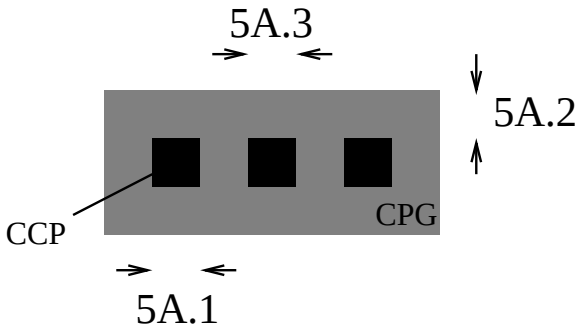


5B.1	Exact **contact** size	2×2
5B.2	Minimum **poly** overlap	1
5B.3	Minimum Spacing on same **poly**	2
5B.4	Minimum Spacing on different **poly**	5
5B.5	Minimum spacing to other **poly**	4
5B.6	Minimum spacing to **active** (one contact)	2
5B.7	Minimum spacing to **active** (many contacts)	3



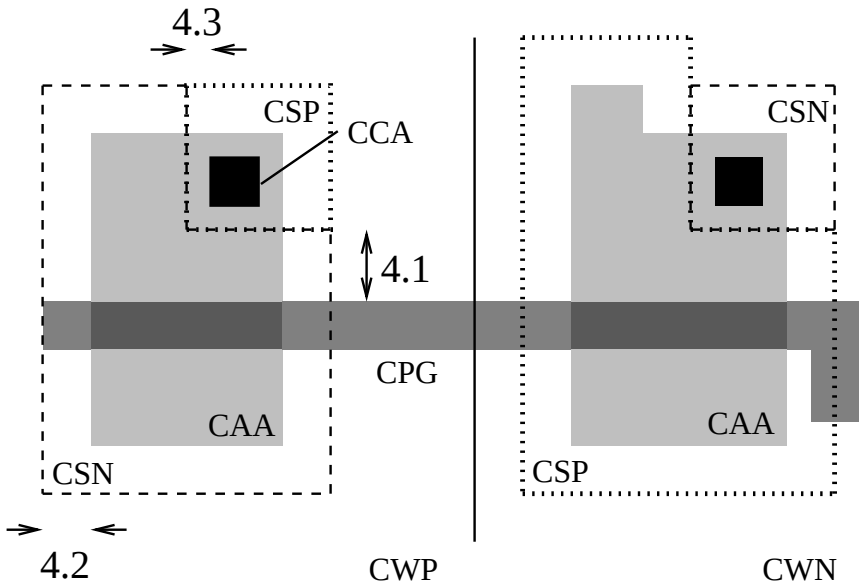
A.5 Contact to Poly - (CCP)

5A.1 Exact **contact** size	2×2
5A.2 Minimum **poly** overlap	2
5A.3 Minimum spacing	2



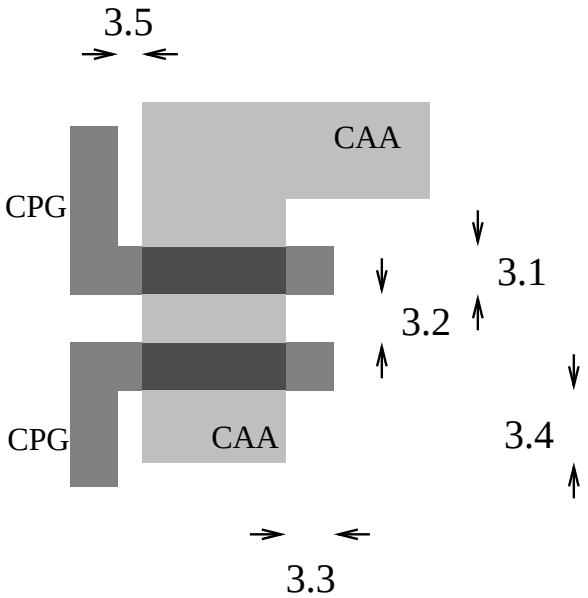
A.4 Select - (CSN, CSP)

4.1	Minimum select spacing to **channel** of transistor to ensure adequate source/drain width	3
4.2	Minimum select overlap of **active**	2
4.3	Minimum select overlap of **contact** to **well** or **substrate**	1
4.4	Minimum **select** width and spacing (Note: P-select and N-select may be coincident, but must *not* be overlap)	2



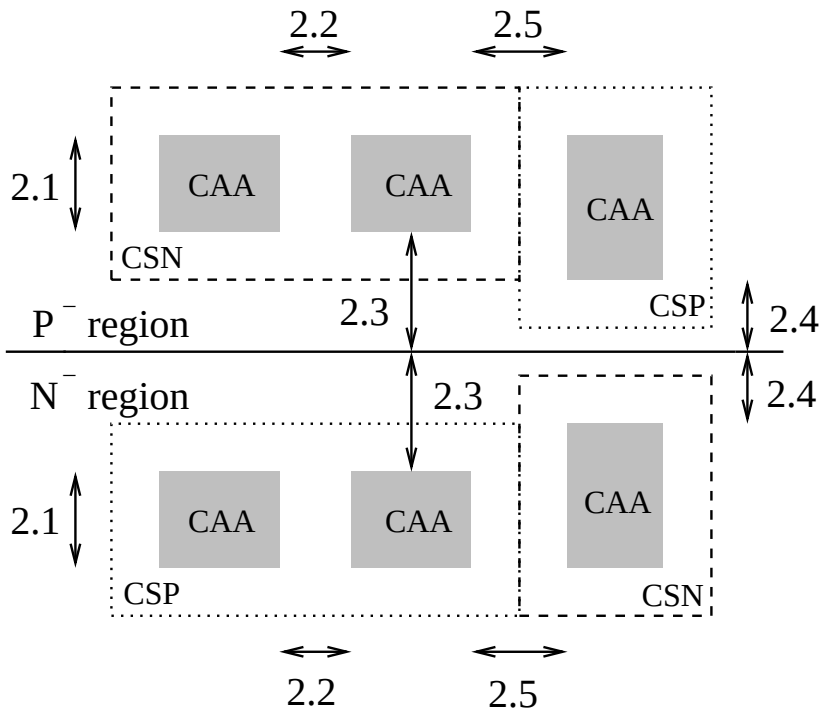
A.3 Poly - (CPG)

3.1	Minimum width	2
3.2	Minimum spacing	2
3.3	Minimum gate overlap of **active**	2
3.4	Minimum a**active** overlap of **ploy**	3
3.5	Minimum field **poly** to **active**	1



A.2 Active - (CAA)

2.1	Minimum width	3
2.2	Minimum spacing	3
2.3	Source/drain active to well edge	5
2.4	Substrate/well contact active to well edge	3
2.5	Minimum spacing between **active** of different implant	4

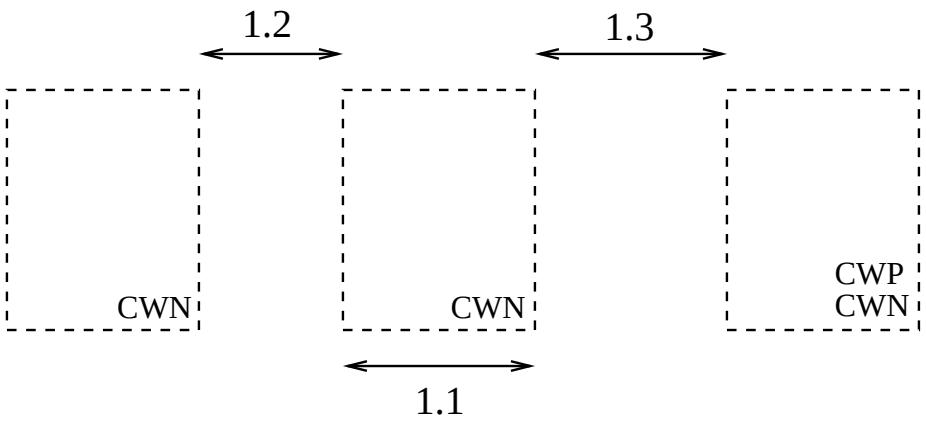


A MOSIS Scalable CMOS Design Rules

This appendix gives MOSIS' scalable CMOS design rules in CIF layers.

A.1 Well - (CWN, CWP)

1.1	Minimum width	10
1.2	Minimum spacing between wells of different potential	9
1.3	Minimum spacing between wells of same potential	0 or 6



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Jeffrey C. Gealpw, MIT
Brain Von Herzen, Synaptics, Inc.
Brian E. D. Kingsbury, UC Berkeley
Janet C. Marshall, NIST
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References

[1] J. C. Marshall, M. Parameswaran, M. E. Zaghloul, and M. Gaitan. High-level CAD melds micromachined devices with foundries. *IEEE Circuits and Devices*, 8(6):10–17, 1992.

[2] C. A. Mead and L. Conway. *Introduction to VLSI Systems.* Addison-Wesley, 1980.

[3] M. Parameswaran, H. P. Baltes, Lj. Ristic, A. C. Dhaded, and A. M. Robinson. A new approach for the fabrication of micromachined structures. *Sensors and Actuators*, 19:289–307, 1989.

[4] M. Parameswaran, A. M. Robinson, D. L. Blackburn and M. Gaitan, and J. Geist. Micromachined thermal radiation emitter from a commercial CMOS process. *IEEE Electron Device Letters*, 12(2):146–149, 1991.

[5] K. E. Petersen. Silicon as a mechanical material. *Proceedings of the [IEEE]*, 70(5):420–457, 1982.

[6] R. R. Troutman. *Latchup in CMOS Technology.* Kluwer Academic Publishers, 1986.

9 Extraction

The SCMOS technology extracts four types of transistor: **pfet, nfet, epfet** and **enet**. All of them must have at least two diffusion terminals. A diffusion terminal is a contiguous region along the perimeter of the transistor channel that connects to diffusion, as shown below:

At the present time capacitors (poly/poly2) are also extracted as a special type of fet. With modified ext2sim and sim2spice, the special fet will be converted to capacitance. Floating gates can not be extract at this time.

A transistor may have more than two diffusion terminals, in which case it is modeled as a collection of two-terminal transistors. If only one diffusion terminal is present, the the extractor flags this as an error and outputs a transistor with the source and drain shorted together.

At the present time bipolar transistors are extracted into 2 diodes in Magic version 6.0. We need to modify the programs : ext2sim and sim2spice in order to convert thse diodes into transistors. These modification have not been finish and will be supplied in later time through MOSIS. Magic 4.10 cannot extract bipolar transistors..

10 Installing the Technology File

Please follow the installation procedure in the README file of MOSIS's distribution tape. Most likely, you would just type **make** at your system prompt.

11 Acknowledgement

The author would like to thank the following persons for their contribution to this work:

- lambda=1.0[nwell] Generates CIF for the MOSIS SCN technology, using n-wells and 2.0-micron feature sizes. Both selects layers are presented.
- lambda=0.6[nwell] Generates CIF for the MOSIS SCN technology, using n-wells and 1.0-micron feature sizes. Both selects layers are presented.
- lambda=1.5[oldnwell]
- lambda=1.0[oldnwell]
- lambda=0.8[oldnwell]
- lambda=0.6[oldnwell] These styles are the same as the 4 styles above except they generate only N-select layer not N-select.
- lambda=1.0[gen] Generates CIF for the MOSIS SCE technology, which includes both p-wells and n-wells and has 2.0-micron minimum feature sizes.
- lambda=0.6[gen] Generates CIF for the MOSIS SCE technology, which includes both p-wells and n-wells and has 1.0-micron minimum feature sizes.
- lambda=0.5[gen] Generates CIF for the MOSIS SCN technology, using n-wells and 1.0-micron feature sizes. Both selects layers are presented.
- lambda=1.5(error) Generates only the error layers with lambda=1.5
- lambda=1.0(error) Generates only the error layers with lambda=1.0
- lambda=0.8(error) Generates only the error layers with lambda=0.8
- lambda=0.6(error) Generates only the error layers with lambda=0.6

The default style is **lambda=1.0[nwell]**. Other styles may be selected with the Magic command **:cif ostyle ....**

For reading CIF or GDS II (stream) file, there are twenty-two styles. Twenty of them correspond exactly to the styles listed above for output. The remaining two are **cbpm3u** and **oldcbpm3u**; they can be used to read in cells designed under the old MOSIS 3-micron rules. Designs converted using style cbpm3u or oldcbpm3u will probably have numerous design-rule violations. Whenever CIF is read, explicit wells are generated and left in the Magic files. You'll have to go in by hand and delete them if you don't want them, or modify the technology file locally so it doesn't generate them on read-in.

Be careful to select the correct style when reading CIF: if you use the wrong style you're likely to get many errors in the resulting Magic file, with very little warning from the CIF reader.

- CPG (GDS II layer number 46) Corresponds to the polysilicon and pcontact layers.
- CCP (GDS II layer number 47) Generated as one or more small squares in the center of each pcontact.
- CCA (GDS II layer number 48) Generated as one or more small squares in the center of each contact to diffusion.
- CMF (GDS II layer number 49) Corresponds to the metal1 Magic layer, plus all contacts.
- CVA (GDS II layer number 50) This layer is generated as one or more small squares in the center of each m2contact.
- CMS (GDS II layer number 51) Corresponds to the metal2 and m2c Magic layers.
- COG (GDS II layer number 52) Overglass holes: generated from the pad and overglass layers.
- CWG (GDS II layer number 53) Corresponds to Well in SCG technology.
- CWP (GDS II layer number 54) Corresponds to Select layer in SCG technology.
- CCE (GDS II layer number 55) Electrode (Poly 2) layer contact to first level metal.
- CEL (GDS II layer number 56) Electrode layer (Second poly layer).
- CCD (GDS II layer number 57) Buried CCD implant.
- CBA (GDS II layer number 58) P-base layer for the NPN transistors.
- CWC (GDS II layer number 59) Capacitor well implant.
- CX (GDS II layer number 60) Comment, No physical meaning.
- CVS (GDS II layer number 61) This layer is generated as one or more small squares in the center of each m3contact.
- CMT (GDS II layer number 62) Corresponds to the metal3 and m3c Magic layers.

If you're curious to see exactly where these layers get generated for a particular design, read about the **:cif see ...** command in the Magic tutorials or man page.

There are currently 20 output styles supported for CIF and GDS II. They are:

- lambda=1.0[pwell] Generates CIF for the MOSIS SCP technology, which uses p-wells and 2.0-micron feature sizes.
- lambda=0.6[pwell] Generates CIF for the MOSIS SCP technology, using p-wells and 1.0-micron feature sizes.

6 Hierarchical Constraints

The design-rule checker enforces several constraints on how subcells may overlap. The general rule is that overlaps may be used to connect portions of cells, but the overlaps must not change the structure of the circuit. Thus, for example, it is acceptable for poly in one cell to overlap pcontact in another cell, but it is not acceptable for poly in one cell to overlap ndiffusion in another, since that would form an ntransistor.

For contacts, there are additional restrictions. A contact in one cell may not overlap a contact in any other cell unless the two contacts have same type and they occupy exactly the same area. Partial overlaps are not permitted, nor are abutting contacts of the same type (contacts of different types may abut, as long as the abutment doesn't violate any other design rules). The contact restrictions are necessary to guarantee that the CIF via holes can be generated correctly in a hierarchical fashion.

7 Routing in SCMOS Technology

If you use Magic's automatic routing tools on an SCMOS design, the routing will be run in **metal1** and **metal2**. **Metal1** is the primary routing layer and will be used wherever possible. In order for Magic to route to terminals, they will have to be on layers that connect to either **metal1** or **metal2**. For example, terminals may be on the pcontact layer (since it connects to **metal1**) but not on the **polysilicon** layer. In this technology, the router will use an 8-unit grid.

8 Reading and Writing CIF and GDS

The SCMOS technology provides several styles of CIF and GDS II (calma) output, corresponding to different flavors of CMOS and different scale factors. All possible layers that can be generaetd from any of the output styles are:

- CWP (GDS II layer number 41) P-well. This layer is generated automatically by bloating the ndiff, nfet, ndc, psd, and psc layers, and OR-ing in the pwell layer.
- CWN (GDS II layer number 42) N-well. This layer is generated by bloating the pdiff, pfet, pdc, nsd, and nsc layers, and OR-ing in the nwell layer.
- CAA (GDS II layer number 43) This is the active mask. It is generated over the areas of Magic's four diffusion layers, plus transistors and diffusion contacts.
- CSP (GDS II layer number 44) P-plus implant mask. This layer is generated by bloating the pdiff, pfet, pdc, psd, and psc layers.
- CSN (GDS II layer number 45) N-plus implant mask. This layer is generated by bloating the ndiff, nfet, ndc, nsd, and nsc layers.

4.2 Buried CCD Layers

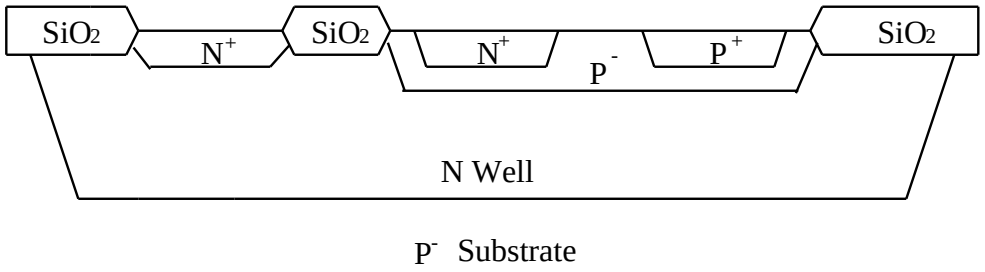
Three extra layers are used in Magic to accept designs for Buried CCD devices. The first layer is named **bccdiffusion** or **bd** for short. The second layer is named **nbccdusion** or **nbd** for short. The last layer is named **nbccdiffcontact** or **nbdc** for short. The nbd and nbdc layers are used to create input/output nodes. The overlapping rules of Nselect and BCCD implant are guarantee by the CIF generation. However the user has the responsibility to assure that the first and the last gates overlap the input/output nodes (nbd) by 2. here is no Magic rule checking on bd, nbd and nbdc, since they are created on a different plane.

5 Layers for Microelectro-Mechanical System

The standard CMOS process has been shown to be able to realize microelectro-mechanical system (MEMS) [1, 5]. Devices such as suspended corners, cantilevers, and pixels can be fabricated with post-processing anisotropic etching developed in [3, 4].

To support these designs, two new layers are used. The first layer is named to as **substrateopen, subopen** or **open**. This layer consists of glass opening and all necessary vias and contacts with the purpose to expose the silicon surface to the ambient after fabrication. When the chips are delivered, the post-processing etch can be performed. This etches the exposed silicon surface anisotropically to realizes the suspended structures. The second layer is refered to by the name of **pdiffusionstop, pdiffstop** or **pstop** for short. This layer is used to restrain the lateral etching at the surface of silicon. In general, a P-type (Boron) diffusion is used for the prupose.

For successful designs, the placement of these layers are crucial, as discussed below.



(CAA) and then biased by an appropriate amount to become the ACTIVE mask. Please remember that the PBASE (CBA), therefore, is a composite layer.

The base layer in Magic used to build NPN bipolar transistors is named **pbase** or **pb**. Pbase contact to metal1 is named **pbasecontact, pbcontact** or **pbc**. The emitter layer is named **emitter, emit** or **em**. Its contact to metal1 is **emittercontact, emitcontact** or **emc**. The collector layer is named **collector, col, co** or **cl**. Its contact layer to metal1 is called **collectorcontact, colcontact, colc, coc** or **clc**. Pbc and emc must be at least 7 units away from each other. This is because Magic bloats emc by 2 to get the N^+ select layer, and it bloats pbc by 1 to obtain the P^+ select layer. Moreover the N^+ select and P^+ select must be at least 7 unit away. The total distance, thus, is 4+2+1=7. Pbc must be overlapped by pbase by 1 unit. Clc must be 5 units away from pbase. Again this is because Magic bloats clc by 1 to get the active layer and collector active bloated must be 4 away from pbase. Well (Nwell) do not have to be painted explicitly. However, we strongly recommend you paint your own well for NPN bipolar transistors.

At the present time we have no way to extract NPN bipolar transistor automatically.

by at least 1 λ. Eelctrode must be at least 1 λ away from diffusion, except where it is forming a transistor. Transistors must be at least 3 λ away from each other.

With two layers of polysilicon, you may overlap them with diffusion to get floating gate devices and buried channeled CCD's. You may also use the two polysilicon to make capacitors. Rules on buried CCD and capacitors will be discussed in the following sections. In making floating gate devices, Magic accepts the names **doubleptransistor, pfloating-gate, pfloatg, pffet**, or **pfg** for P-type floating gate devices. It accepts the names **doublentransistor, nfloating-gate, nfloatg, nffet**, or **nfg** for N-type floating gate devices. Floating gate devices must be at least 2 λ in length and 3 λ wide.

Since Magic has no way of knowing the overlapping two polysilicon layers are used for floating gates, it will flag rule violations. It basically treat the overlap of two polysilicon as capacitors and insists that poly must overlap electrode by 2 λ. In general, if you are doing floating gate devices you should ignore these design rule violations.

4 Layers for Low-Noise Analog Process

4.1 NPN Transistors

An extra P^- base diffusion layer is allowed on selected MOSIS runs. This layers allows the design of (1) in well isolated NPN bipolar transistor; (2) higher voltage P-channel MOSFETs; (3) in well P and N-channel junction FETs; (4) in well higher threshold nMOS devices; (5) in well isolated photoreceptors; (6) in well metal semiconductor Schottky diodes (assuming nwell process).

There are two different styles in designing the NPN bipolar transistors — SCEA and SCGA. Magic accepts the SCEA style of designs. In SCEA style, the drawn PBASE (CBA) layer (eg. P^- in NWELL) is bloated by 2 lambda per side to give the PBASE IMPLANT mask by MOSIS. Moreover, the PBASE (CBA) layer is orred with the drawn ACTIVE layer

3.3 Polysilicon/Electrode Capacitors

Over-lapping polysilicon with electrode will give you precision capacitors for analog designs. Since regular electrode layers must be 2 λ away from polysilicon a special magic layer is created for capacitor. It accepts the names **capacitor, poly cap, pcap** or just **cap**. In making a capacitor, the electrode layer must be overlapped by 2 λ of poly. The electrode layers must be 2 λ away from wells and polycontacts. When making a electrode contact on a capacitor the electrode must overlap the composite contact layer, **capcaontact** by 2 λ. This capcontact layer can also be called **ccontact** or **capc** or **cc**. Magic will try to extract capacitor as a two terminal fet. (At MOSIS we have made some modification to **ext2sim** and **ext2spice** which allows the automatic extraction of capacitors. You may obtain these by sending an ATTN message to MOSIS.) It is recommended that you make the capacitor layer larger enough to compensate fabrication variations.

3.4 Polysilicon/Electrode Transistors

Electrode layer can also be used to create transistors by over-lapping electrode over pdiffusion or ndiffusion. Magic accepts the names **epfet** and **eptransistors** or **enfet** and **entransistor** respectively. Transistors of each type can be generated by painting polysilicon and diffusion on top of each other, or by painting the transistor layer explicitly. The design rules are the same for both types of transistor: transistors must be at least 2 λ long and 3 λ wide. Electrode used as gate must overhung transistor by at least 2 λ. Diffusion (ndiff or pdiff) must overhung transistor by at least 3 λ. They must be separated from nearby electrodes/econtacts

Electrode (or Second Poly) is drawn in waffle patten with yellow color, and can be referred to in Magic as either **poly2** or **electrode** or **el** or **p2**. It has a minimum width of 2 λ and a minimum spacing of 3 λ.

3.2 Electrode Contact

Electrodes must be at least 2 λ away from any diffusion contact. Econtacts, with the 1 λ overlap of electrode, will be at least 3 λ away from and diffusion contacts, as a result. See Section 2.10 for more rules on substrate contacts.

Contacts between metal1 and electrode (or poly2) go by the names **electrodecontact, econtact, ec, poly2contact** and **p2c**. As with all contacts, you only draw the outer boundary of the overlapping area of electrode and metal1; Magic fills in the contact cut(s) at mask generation time. Econtact areas must be at least 4 λ wide and must be overlapped by 1 λ with the layer electrode. This guarantees the total overlap of electrode over the real cut to be at least 2 λ. Therefore there is no spacing rule governs the econtact layers. Econtacts must be at least 3 λ away from polycontacts even if they are connected electrically by metal1. There is another type of electrode contact to metal1 layer, **capcontact**. This layer has different design rules. It is used in making electrode contacts for poly/electrode capacitors. Its properties will be describe in more detail in section 3.9.

CIF layer names described in Section 5. There may be a few cases where you'd like to guarantee that certain areas are covered with wells, e.g. pads. For these cases you may paint the explicit layers **nwell** and **pwell**. Nwell appears on the screen as diagonal green stripes, and pwell appears as diagonal brown stripes. The explicit well layers that you paint will supplement the automatically-generated wells. Pwell must be at least five units from pdiffusion, ptransistor, or pdcontact, and three units from nncontact. Nwell must be at least five units from ndiffusion, ntransistor, or ndcontact, and three units from ppcontact. Nwell and pwell may abut but not overlap (if you paint one well on top of the other, the new one replaces the old one). All nwell and pwell areas that you paint must be at least 10 units wide and are separated from other wells of the same type by at least nine units.

Guard rings may be created using the nndiffusion and ppdiffusion layers. Nncontacts and ppcontacts should be used to strap the rings to Vdd and GND, respectively. Nndiffusion must be at least 3 λ from pwell, 6 λ from ppdifffusion or ppcontact, and 8 λ from ndiffusion or ndcontact (these are the same rules as for nncontact). Similar rules apply to ppdiffusion. Guard rings are probably the only things that nndiffusion and ppdiffusion will be used for.

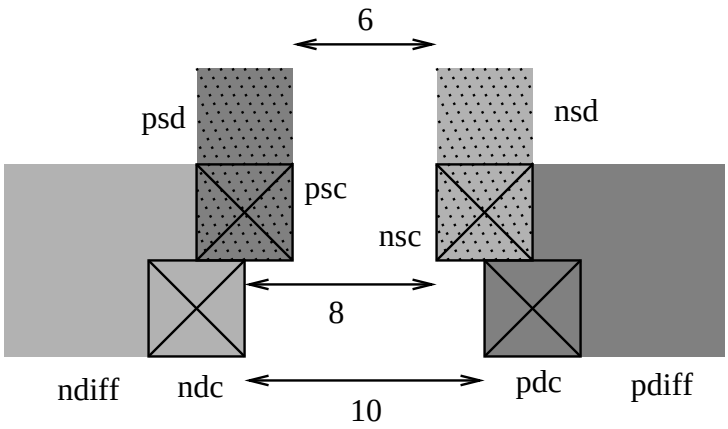
2.13 Overglass and Pads

Normally, everything in the layout is covered by overglass in order to protect the circuitry. If you do not wish to have overglass in certain areas of the layout, there are two Magic layers you can use for this. The Magic layer **pad** should be used for drawing pads. It generates a hole in the overglass covering and also automatically includes metal1, metal2, and via. Pad is displayed as metal2 over metal1, with additional diagonal stripes. The rules for pads are in absolute microns, not lambda units: the pad layer must always be at least 100 microns on a side. Since this rule is in absolute units, it is not checked by the Magic design-rule checker. Pads will generally need to be modified in order to fabricate at different scale factors or for different flavors of CMOS.

An additional layer **glass** is provided to allow designers to make unusual glass cuts anywhere on the chip for probing or other purposes. This layer is drawn in dark diagonal stripes. Probe areas should generally be at least 75 microns wide, but Magic does not check this rule.

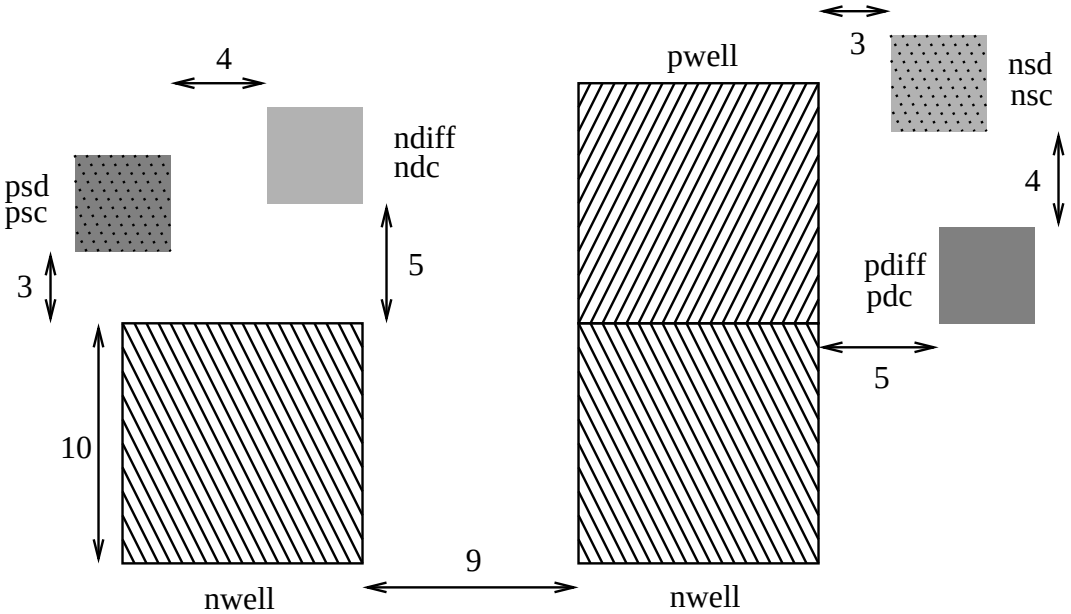
3 Layers for Two Polysilicon Process

3.1 Electrode



be 8 units from ndiffusion, ppcontact need only be 8 λ from pdiffusion, and nncontact and ppcontact need only be 6 λ apart.

2.12 Wells and Rings



For the most part, you should not need to draw explicit wells. However it is recommended that you use painting explicit well as a mean to plan for your layout topology. When writing out CIF or GDS II files, Magic generates them automatically. Nwell is generated around pdiffusion, ptransistor, pdcontact, and nncontact. Pwell is generated around ndiffusion, ntransistor, ndcontact, and ppcontact. Magic merges nearby well areas into single large wells when possible. For example, two ndiffusion or pdiffusion areas will share a single well if they are within 10 units of each other. If you're curious about exactly what Magic will use as the well areas, you can use the Magic command **:cif see ...** along with the

2.10 Substrate Contacts

There are several additional rules besides those in Section 2.6 that apply to substrate contacts. Substrate contacts are used to maintain proper substrate voltages and prevent latchup [6]. Nncontact is used to supply a Vdd voltage level to the n-wells (or n-substrate) around p-transistors, and ppcontact is used to supply a GND voltage level to the p-wells (or p-substrate) around n-transistors. Nncontact must be separated from p-transistors by at least 3 units to ensure that the n+ implant doesn't affect the transistor. Nncontact may be placed next to pdcontact in order to tie a transistor terminal to Vdd at the same time. Because of diode formation, nncontact will not connect to adjoining pdiffusion unless there are contacts to metal1 to strap them together. Similar rules apply to ppcontact.

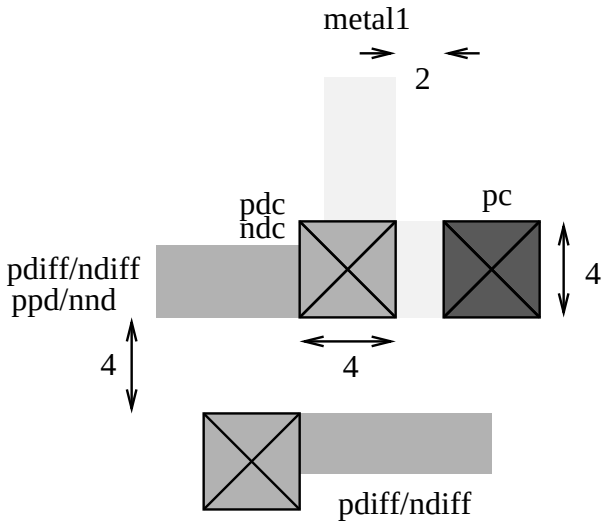
There is a special technology file written by prof. Fred Rosenberger of Washington University at Saint Louis which will check if you have placed enough substrate contacts in a well. This technology file and accompany program is distributed by MOSIS User Group (MUG). Please contact prof. Don Bouldin at University of Tennesse to obtain a copy of the program and technology file. It is recommended that you place plenty of well and substrate contacts in your layout, however. If you place too few, you risk latch-up in your circuit, so a good rule of thumb is to place one nncontact for each ptransistor that has its source tied to Vdd, and one pwcontact for each ntransistor that has its drain tied to GND. To avoid having wells floating (especially auto-generated wells), it is recommended that you put a well (substrate) contacts for every cluster of transistors.

2.11 Spacings between P and N

Ndiffusion, ntransistor, ndcontact, and ppcontact must be kept far away from pdiffusion, ptransistor, pdcontact, and nncontact, in order to leave room for wells. Ndiffusion and pdiffusion must be 10 λ apart. Substrate contacts can be 2 λ closer to material of the opposite type (the wells needn't surround them by as many units), so nncontact need only

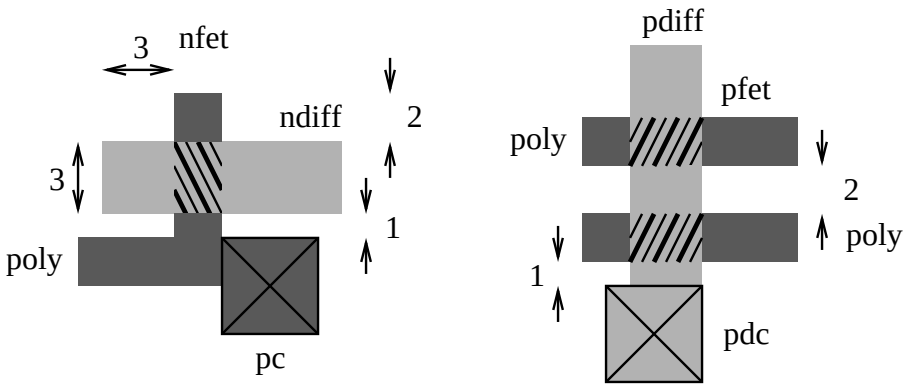
transistor area. The names **nfet**, and **ntransistor** may be used. Transistors of each type can be generated by painting polysilicon and diffusion on top of each other, or by painting the transistor layer explicitly. The design rules are the same for both types of transistor: transistors must be at least 2 λ long and 3 λ wide. Polysilicon used as gate must overhung transistor by at least 2 λ. Diffusion (ndiff or pdiff) must overhung transistor by at least 3 λ. They must be separated from nearby poly contacts by at least 1 λ. Polysilicon must be at least 1 λ away from diffusion, except where it is forming a transistor. Transistors must be at least 2 λ away from each other.

between metal1 and psubstratepdiff are called **psubstratepcontact** or **ppcontact** or **psc** or **ppc** or **pohmic** All diffusion contacts must be at least 4 λ wide, and must be separated from unrelated diffusion by 4 λ, one unit more than the normal diffusion-diffusion separation. It is recommended that contacts to poly or diffusion be sized by multiple of 4 unit. This is again to warrant the cuts to be on the lambda grid.

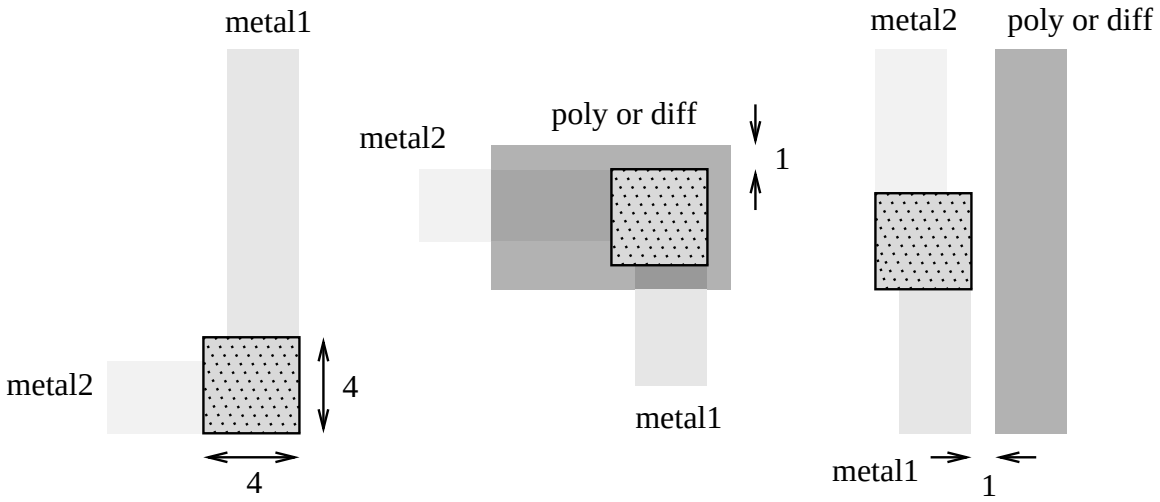


Both poly, electrode and diffusion contacts appear on the screen as an overlap between the two constituent layers, with a cross over the contact area. All contacts must be rectangular in shape. Pdc may abut nsc and and ndc may abut psc; all other contact abutments are illegal. Pcontact must be at least 2 λ from any diffusion contact, even if the two contacts are electrically connected as on the top/right of the figure above.

2.9 MOS Transistors

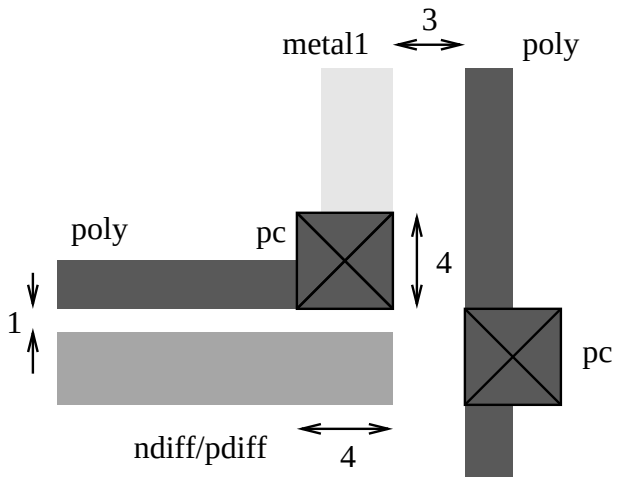


P-type transistors are drawn as an area of poly over-lapping pdiffusion, with brown stripes in the transistor area. Magic accepts the names **pfet** or **ptransistor** for this layer. N-type transistors are drawn as an area of poly overlapping ndiffusion, with green stripes in the



2.8 Polysilicon and Diffusion Contacts

Contacts between metal1 and polysilicon go by the names **polycontact, pcontact, polycut**, and **pc**. As with all contacts, you only draw the outer boundary of the overlapping area of poly and metal1; Magic fills in the contact cut(s) at mask generation time. Pcontact areas must be at least 4 λ wide and must be separated from unrelated polysilicon and pcontact by at least 3 λ. This is one unit more than the normal poly-poly separation, and is required because MOSIS bloats the polysilicon around pcontacts. Polycontacts must be 1 λ away from diffusions.

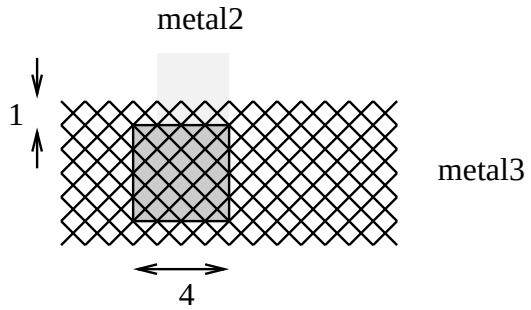


In digital design there are four kinds of contacts between metal1 and diffusion, one for each of the kinds of diffusion. There are other diffusion contacts used only to build analog (NPN) devices. These layers will be detailed in section 4. Contacts between metal1 and ndiffusion are called **ndcontact, ndiffcut** or **ndc**. Contacts betwen metal1 and pdiffusion are called **pdcontact, pdiffcut** or **pdc**. Contacts between metal1 and nsubstratendiff are called **nsubstratencontact** or **nncontact** or **nsc** or **nnc** or **nohmic**. Lastly, contacts

2.6 Metal3 Contacts

Via between metal2 and metal3 is called **m3contact, m3cut, m3c, via2**, or **v2** and is drawn with crossed waffle pattens mixed with purple and cyan colors. In Magic, contacts aren't drawn as two areas of overlapping material with a via hole in the middle. Instead, you just draw a single large area of a special composite layer, for example, m3contact in the case of metal3 contacts. This corresponds to the area where the two wiring layers overlap (metal2 and metal3 in the case of metal3 contacts). Magic will automatically output metal2, metal3 when it generates CIF or Calma output and will also generate the small via hole in the center of the contact area. For large contact areas Magic will automatically generate many small via holes in CIF or Calma output. All contacts must be rectangular: two contacts of the same type may not abut.

The minimum width of m3contact is 4 λ and it must be enclosed by metal3 by at least 1 λ. It is recommended that metal3 contacts be sized in the following quantized values: 4, 9, 14, 19, 24 ... (or 1+1+2+5k where k=0, 1, 2, ...). This is to assure that metal2 contacts are always on the lambda grid.



2.7 Metal2 Contacts

All other contacts involve the metal1 layer. Contacts from metal1 to metal2 are called **m2contact, m2cut, m2c, via**, or **v**. They appear on the screen as an area of metal1 overlapping an area of metal2, with a black waffle pattern over the contact area. Metal2 contacts must be at least 4 λ wide. No enclosure of either metal1 or metal2 is required. M2contact of quantized sizes: 4, 9, 14, 19, 24 ... (or 1+1+2+5k where k=0, 1, 2, ...) is also recommended for the same reason as m3c.

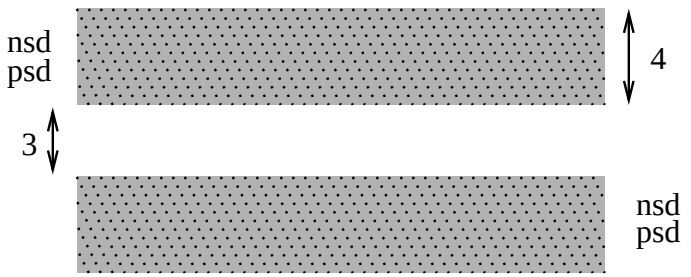
There is an additional special rule for metal2 contacts: there must not be any electrode, polysilicon or diffusion edges underneath the area of the contact or within 1 λ of the contact. This rule is present because it is hard to fabricate a metal2 contact over the sharp rise of a poly or diffusion edge. It is acceptable for poly or diffusion to lie under a m2contact area, as long as it completely covers the area of the m2contact with an additional 1 λ surround.

2.5 Diffusion

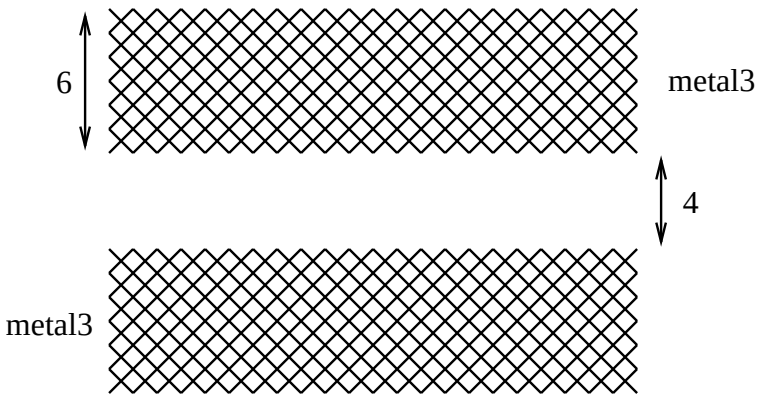
In the SCMOS technology, it is unnecessary (however it is recommended) for you to specify wells and implant selection layers explicitly. Instead, there are four different layers that correspond to the two kinds of diffusion in two types of well. Based on these four layers, Magic automatically generates the masks for active, wells, and implant selects.

The most common kinds of diffusion are P-diffusion in an N-well (N-substrate) and N-diffusion in a P-well (P-substratete); they are used for creating P-type and N-type transistors, respectively. P-diffusion in an N-well is drawn with a filled light brown color; Magic accepts the names **pdiffusion, pdiff**, or **brown** for this layer. N-diffusion in a P-well is drawn in filled green, and can be referred to as **ndiffusion, ndiff**, or **green**.

The other two kinds of diffusion are used for generating well (substrate) contacts and guard rings; they consist of a strongly implanted diffusion area in a well of the same type. P-diffusion in a P-well is drawn with a light brown color and it has stippled holes in it. It goes by the names **psubstratepdiff, ppdiff, pohmic, ppd** or **psd**. N-diffusion in an N-well is drawn in a light green color with stippled holes in it, and goes by the names **nsubstratendiff, nndiff, nohmic, nnd** or **nsd**.

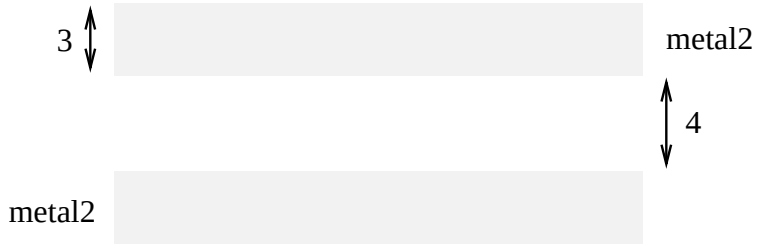


The basic design rules for the first two kinds of diffusion are the same: they must be at least 3 λ wide and have a spacing (to the same kind of diffusion) of at least 3 λ. The second kinds of diffusion used as substrate (well) contacts must be at least 4 λ wide and have a spacing (to the same kind of diffusion) of at least 3 λ. Spacing rules between diffusions of different types are discussed later in Section 2.11.



2.2 Second-level Metal

The next level of metal is drawn in a filled purple color, and has the names **metal2**, **m2** or **purple**. It must always be at least 3 λ wide, and metal2 areas must be separated from each other by at least 4 λ.



2.3 First-level Metal

The lowest level of metal is drawn in a filled blue color and has the names **metal1**, **m1** or **blue**. It has a minimum width of 3 λ and a minimum spacing of 3 λ.

2.4 Polysilicon

Polysilicon is drawn in filled red, and can be referred to in Magic as either **polysilicon**, **red**, **poly** or **p**. It has a minimum width of 2 λ and a minimum spacing of 2 λ.

- 8 layers to support two polysilicon process
- 9 layers to support low-noise analog process
- 2 layers for the implementaion of *linear capacitor*
- 2 layers for micromachined device fabrication [1, 5]

In general, the interconnect layers (metal3, metal2, metal1, electrode, poly, diffusions) will come out as you draw them. You draw contacts in terms of the total overlap area between the layers being connected, not in terms of the via holes. All contacts are to first-level metal except vias between second and third metal layers. No buried or stacked contacts (mushroom contacts) are allowed.

In order for SCMOS designs to be fabricated with either N-well or P-well technology, both P-well and N-well contacts must be placed, and where wells and guard rings are specified explicitly (e.g. in pads) both flavors must be specified. When the circuit is fabricated, one of the flavors of wells, guard rings, and substrate contacts will be ignored. Implants will be generated automatically by Magic from bloated or shrunk versions of the various contacts and diffusions. However, wells can either be painted explicitly or left for Magic to generate. The final wells will be the combination of painted wells and automatically generated wells from bloating/shrinking of the diffusions and contacts.

The painting tables have been set up in the SCMOS technology to make it easy for you to turn N-flavored things into P-flavor, and vice versa. If you paint **nwell** over an area, any N-diffusion in the area will be turned into P-diffusion, N-type FET into P-type FET, N-diffusion contact into P-diffusion contact, P-substrate diffusion into N-substrate diffusion, and P-substrate contact into N-substrate contact. Similarly, if you paint **pwell** over an area, any P-diffusion in the area will be turned into N-diffusion, P-type FET into N-type FET, P-diffusion contact into N-diffusion conatct, N-substrate diffusion into P-substrate diffusion, and N-substrate contact into P-substrate contact. Thus, if you'd like to make a symmetrical copy of something, except for the opposite well, you can copy it, paint the opposite well over it, then erase the well to leave just the basic layers.

2 Layers for Standard CMOS process

Again, layers you draw in Magic are abstract layers or *logs*, and do not correspond exactly to the mask patterns be used to fabricate your circuit. As a result, following rules may have different numbers when compared with MOSIS scalable CMOS Rules which is specified for CIF layers (see Appendix A).

2.1 Third-level Metal

The top level of metal is named **metal3**, **m3** or **cyan**. It is drawn in cross patten with a cyan color. It must always be at least 6 λ wide, and separated from each other by at least 4 λ.

Magic Technology Manual for MOSIS' Scalable CMOS

(Preliminary)

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1 Introduction

This document describes the Magic (version 6) technology corresponding to the MOSIS Scalable CMOS (SCMOS) design rules. It includes information about the layers, design rules, routing, CIF generation, and circuit extraction. The Magic name for this technology is **scmos**; if it isn't the default technology at your site, you may have to use the switch **-T scmos** when running Magic from the shell. The most important characteristic of the SCMOS technology is that it is *scalable* and *flavorless*: layouts designed using the SCMOS rules may be fabricated in either N-well or P-well technology at a variety of feature sizes.

Circuit layouts in Magic follows Mead and Conway's λ-based design style: geometry rules are followed by a dimensionless unit λ [2]. By changing the assigned value of λ, design can be easily scaled down as fabrication technology advances. MOSIS currently supports CMOS fabrication at $\lambda = 0.5\mu m$, $\lambda = 0.6\mu m$ and $\lambda = 1.0\mu m$, i.e. 1.0 μm, 1.2 μm and 2.0 μm of feature size respectively. Other smaller scale factors will become available in the future.

Layers you draw in Magic are *abstract* or *composite* layers, and do not correspond exactly to the mask patterns be used to fabricate your circuit. In fact, Magic layers must be translated into CIF (or GDS II) layers before submitting to MOSIS. There are total 45 layers defined on 7 planes in SCMOS technology. These layer can be further characterized into the following five categories:

- 24 layers to support standard three-level metal, single polysilicon CMOS process