TABLE OF CONTENTS

RELEASE NOTES

Spice3e is the fifth major release of Spice3. This release incorporates new features not available in Spice 3c or 3d, as well as several performance improvements. All of the features described here are believed to be fully functional. The development of SPICE and its algorithms is ongoing at Berkeley, and therefore not all of the intended capabilities of the program have been implemented in full yet.

New features and bug fixes incorporated in Spice3e (the current release of Spice3):

Lossy Transmission Lines
Proper calculation of sheet resistance in the MOS models.
A new command ("where") to aid in debugging troublesome circuits.
Smith-chart plots working (see the "plot" command summary for remaining limitations).
Arbitrary sources in subcircuits handled correctly.
Arbitrary source reciprocal calculations and DC biasing is now done correctly.
Minor bug-fixes to the Pole-Zero analysis
Miscellaneous bug fixes in the front end.

New features and bug fixes incorporated in Spice3d2 (the *previous* release of Spice3):

Distortion analysis
Noise analysis
Improved Pole-Zero analysis
A new BSIM MOS model (BSIM2, level 5)
A new analytic MOS model (level 6)
Miscellaneous bug fixes in the front end.

Some common problems remaining in Spice3e (note that this list is not complete):

Models defined within subcircuits are not handled correctly. Models must be defined outside of ".subckt" and ".ends" lines or the model is not found.

Batch run data is not compacted resulting in excessively large raw output files, especially transient simulation of lossy transmission lines. Running simulations interactively is not affected.

Sufficient detail is sometimes not preserved in transient analysis. Providing a small value for the "TMAX" parameter (the fourth argument) in the transient run command will solve this problem.

Convergence problems can sometimes be worked around by relaxing the transient "TMAX" parameter.

Ascii (printer) plots do not print decibel plots vs log of the frequency by default, as in spice2. You must explicity request the x-axis to be log; either "plot vdb(2) xlog" or "plot vdb(2) vs log10(frequency)" will do.

Multiple analyses and plots in spice2 emulation mode sometimes get confused. Either run interactively, run one analysis at a time, or generate raw data files instead of ascii-plots.

Operating point summary information is not available in a table, as in spice2.

The bulk node of the bipolar transistor (BJT) is modelled incorrectly. Do not use the bulk node; use a semiconductor capacitor to model bulk effects.

Charge storage in MOS devices based on the Meyer model is incorrectly calculated.

The BSIM MOS model implementations reveal compiler limitations. On some systems, a "core dump" when simulating any BSIM device may be from a compiler bug. Other systems may not even be able to compile the code.

Transient simulation of strictly resistive circuits (typical for first runs or tests) allow a time step that is too large (e.g. a sinusoidal source driving a resistor). There is no integration error to restrict the time step. Use the "TMAX" parameter or include reactive elements.

Deep nesting of subcircuits may exceed internal static buffers.

There are many other small bugs, particularly in the front end.

Bug reporting:

Please send bug reports or suggested enhancements to Spice3 via electronic mail to:

spice@Berkeley.EDU (Internet)
ucbvax!spice (UUCP-net)

or by physical mail to:

Spice Bug Report
EECS/ERL Industrial Support Office
479 Cory Hall
U.C. Berkeley
Berkeley, Ca. 94720

Include the version of Spice used, the system type and operating system version, the smallest input file demonstrating the problem, and the resulting (incorrect) output.