Rice University
Elec 422: VLSI Design I
Midterm Examination

Fall 2000

November 21, 2000

Due: 4pm Friday, December 1, 2000

*Name:*_____

Points	15	15	15	15	15	10	15	Max = 100
Problem	1	2	3	4	5	6	7	Total

Take home exam with Three hours total elapsed time.
You may stop to ask the instructor or lab assistant a question and then resume.
This exam is closed book and closed notes.
Please attach additional pages as needed to complete these problems.
Please state your assumptions clearly.
Please label all signals on all diagrams clearly.

Please sign the honor system pledge below.

Pledge:

1 Logic Design (15 points)

Fully draw a transistor level diagram to implement the following function. Use static complementary CMOS logic only. Assume that only the original signals are available. All complements need to be generated in your circuit. Use compound gates where possible. You do not need to minimize the logic or indicate transistor ratio sizes. Please connect the output wires from one gate to the inputs of the next gate, all in the same diagram. Exclusive-OR is shown as $\oplus$.

$$mid1 = \overline{(a \cdot b) + c + (d \cdot e)}$$

$$mid2 = \overline{f \oplus g}$$

$$result = \overline{mid1 \cdot mid2 \cdot h}$$

2 Stick Diagram - CMOS Two Level Metal (15 points)

Draw a CMOS stick diagram for the circuit implemented in Problem 1 in a standard static complementary CMOS logic family. Use our typical two-layer metal MOSIS SCMOS process.

Follow these I/O constraints exactly:

1. Please make Vdd and GND run horizontally across the circuit in metal1.
2. Please make the inputs, a, b, c, d, e come from the left in metal1
3. Please make the inputs, f, g, h come from the right in metal 1
4. Please make the output "result" exit to the right in metal 1

Please make sure that your design preserves the relative position of the signals along the cell boundary and that the signals enter and leave the cell on the specified layer. (Note: Please use an entire page for the stick diagram.)

3 Design Rules (15 points)

Use the MOSIS SCMOS rules as described in the Elec422 Manual. The circuit will be presented in color and in black and white on the following pages. There will be a color "xv" xview screendump plot with grid, and a color "pplot" plot of the same circuit.

There may be several occurances of the same error in different parts of the layout. Please treat each as a separate error. The $magic$ design rule checker finds over 15 errors in this piece of layout. Please locate at least 15 errors and label each error area with a unique number label (1 through 15) on whichever of the plots you find most convenient and describe the design rule error in words below indicating what the minimum width or separation should have been:

error (1):

error (2):

error (3):

error (4):

error (5):

error (6):

error (7):

error (8):

error (9):

error (10):

error (11):

error (12):

error (13):

error (14):

error (15):

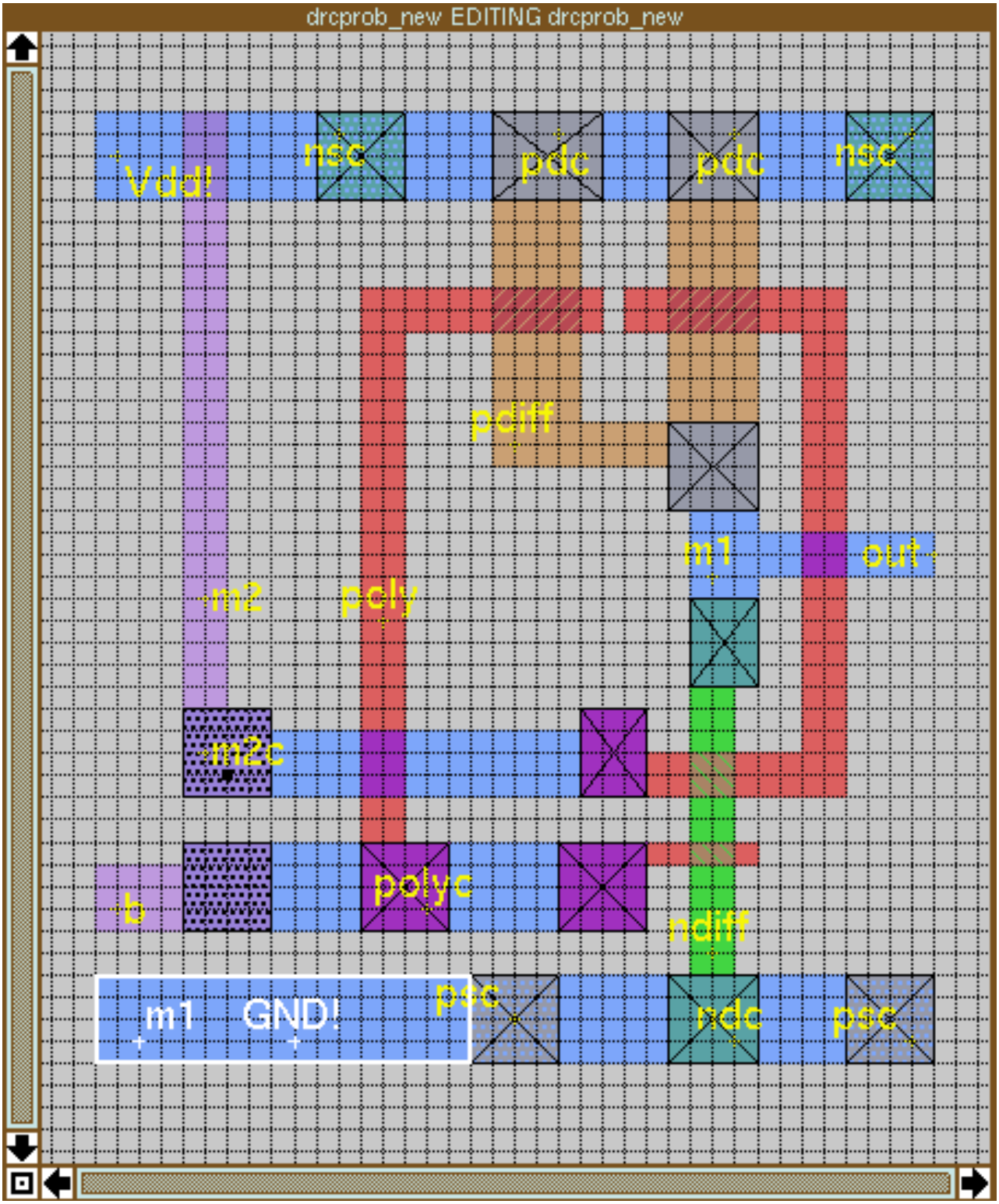

Figure 1: “xv” xview plot of circuit.

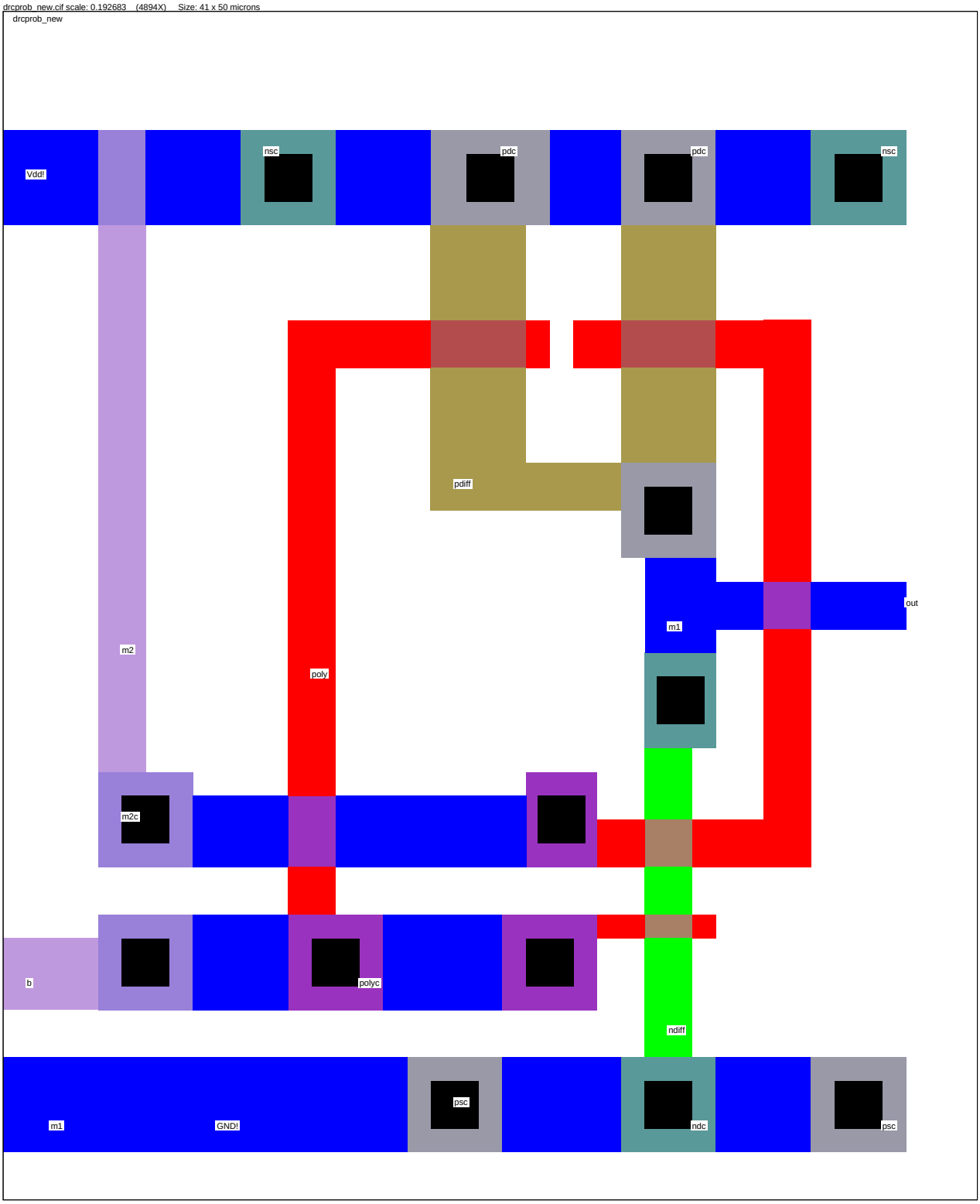

Figure 2: Color Pplot plot of circuit.

4 System Timing (15 points)

Label the following circuit according to the timing discipline discussed by K. Karplus and presented in class. Use labels such as Q_A, V_A, $V_A S_B$, and so on. Consider Input and Output nodes to only be signals at the external physical boundary of the circuit. You should label the Inputs, $a, b, e, h, i, j, k, o, p$, with the weakest allowable signal. Based on the timing rules for combinational logic and storage elements, propagate these signals through the interior nodes of the circuit. By doing this, the Outputs should be labeled with the strongest produced signal. The TGATE + INVERTER groups can be considered as dynamic latches, therefore this circuit would be connected to both CLKA and CLKB. Start with signals based on CLKA on the left hand side of the circuit. It is possible that in the circuit as designed below there could be a node or nodes which violate the timing discipline. If this is the case, please try to preserve as much of the circuit as possible and indicate the node or nodes that are in violation. Also, suggest a possible solution to the timing discipline violation.

node a:	node b:	node c:
node d:	node e:	node f:
node g:	node h:	node i:
node j:	node k:	node l:
node m:	node n:	node o:
node p:	node q:	

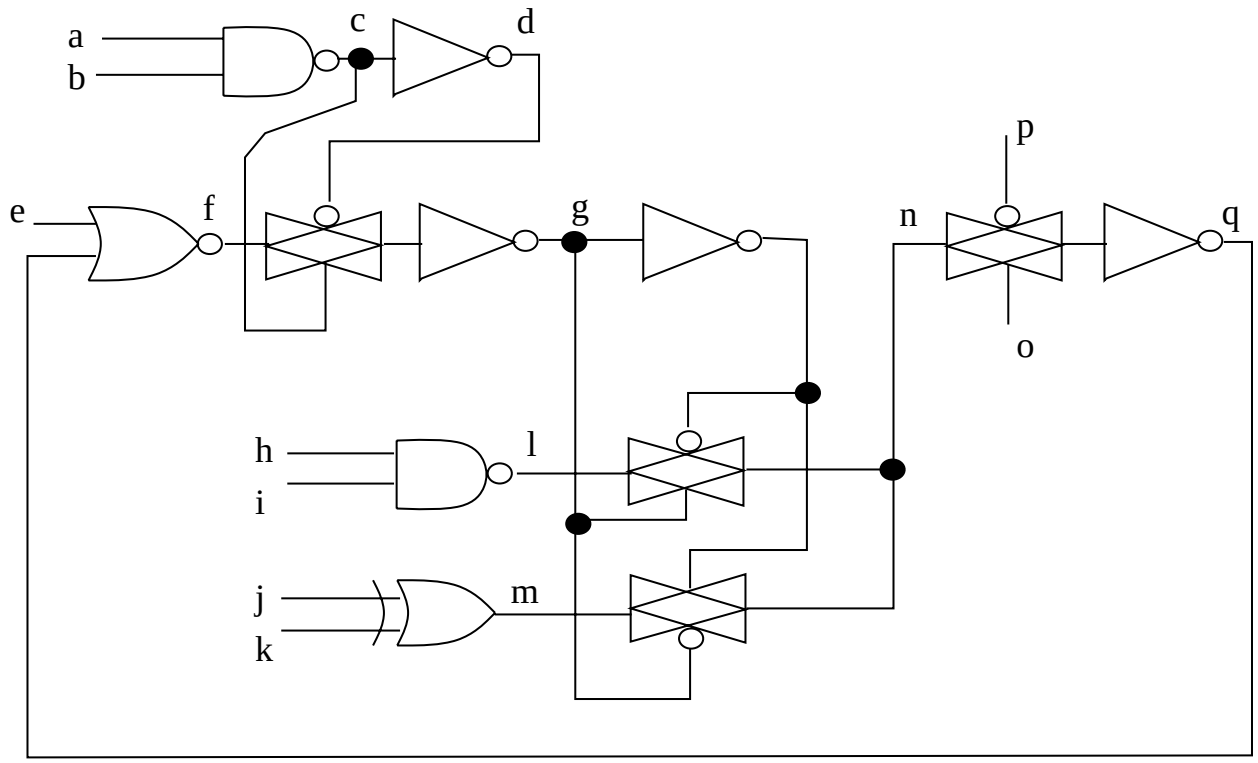

Figure 3: Circuit for timing problem.

5 Logic Families - Domino(15 points)

Dynamic Domino Logic: Draw a transistor level diagram only to implement the following logic function in Dynamic Domino CMOS logic with n-channel pulldown logic blocks:

$$mid1 = (a + b) \cdot c \cdot d$$

$$mid2 = mid1 + e + f$$

$$result = g \cdot mid2$$

By hand, "simulate" the behavior of this circuit. An "irsim" style test vector file is given below. For each of the watched nodes, plot the behavior of the circuit versus time for the following set of inputs:

```
| IRSIM test vector file for dynamic Domino circuit
|

clock Vdd 1

ana precharge a b c d mid1 e f mid2 g result


V precharge  0 1 0 1 0 1 0 1 0
V a          0 1 0 1 0 0 0 1 0
V b          0 0 0 0 0 1 0 0 0
V c          0 1 0 1 0 0 0 0 0
V d          0 0 0 1 0 1 0 1 0
V e          0 1 0 0 0 0 0 1 0
V f          0 1 0 1 0 0 0 1 0
V g          0 1 0 1 0 0 0 1 0
R
```

6 Processing Technology (10 points)

Consider a typical CMOS process. Briefly answer the following questions. Two or three sentences are sufficient.

1. Draw a simple diagram and briefly describe the apparatus used for ion implantation.

2. Draw a simple diagram and briefly describe the apparatus used in the Czochralski process for crystal growth.

3. Draw a simple cross-section diagram showing the structure of a metal2 to metal1 contact or via. Assume that this structure is in an empty portion of the chip. Label each of the conducting and insulating layers from the surface of the silicon and on up.

7 Approximate RC Timing Analysis (15 points)

Perform an approximate RC timing analysis of three inverters connected in a ring oscillator circuit as shown in the figure below.

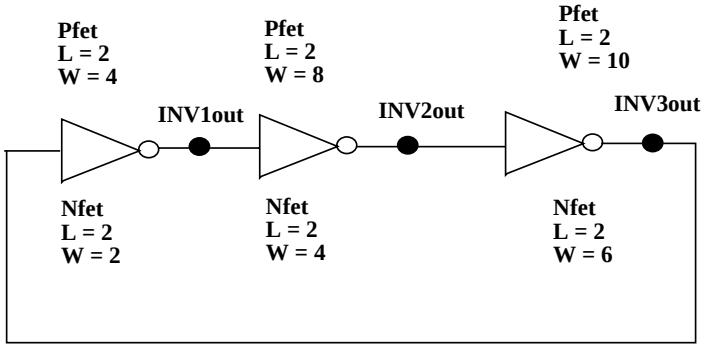

Figure 4: Ring oscillator circuit.

You may ignore the interconnect wire lengths. The various contacts to be considered in the analysis are the ndiff (ndc), pdiff (pdc), and poly contacts (polyc) as typical within an inverter. You may ignore the resistance of the contacts. Assume that the lengths (L) and widths (W) of the transistors in lambda λ units vary from inverter to inverter and are as marked in the figure. Assume that the circuit is in steady state and is oscillating in this problem.

Compute the following quantities, with R in $K\Omega$, C in fF, and T (time) in nanoseconds, ns:

1. $R_{INV1rise}, R_{INV1fall}, C_{INV1out}, T_{INV1rise}, T_{INV1fall}$
2. $R_{INV2rise}, R_{INV2fall}, C_{INV2out}, T_{INV2rise}, T_{INV2fall}$
3. $R_{INV3rise}, R_{INV3fall}, C_{INV3out}, T_{INV3rise}, T_{INV3fall}$
4. Total time for propagation when INV1 rises and INV2 falls and INV3 rises,
5. Total time for propagation when INV1 falls and INV2 rises and INV3 falls,
6. Use the propagation times calculated above to compute the approximate period and frequency of oscillation of this circuit.

Use the following approximate values for the parameters for approximate RC analysis:

nfet passing 0 = $14K\Omega = 1R/\Box$, nfet passing 1 = $56K\Omega = 4R/\Box$

pfet passing 0 = $112K\Omega = 8R/\Box$, pfet passing 1 = $28K\Omega = 2R/\Box$

$C_g = 12fF$

Contacts: 4×4 ndiff = $2.0C_g$, 4×4 pdiff = $1.5C_g$, 4×4 poly = $0.25C_g$.

pdiff lumped with pchannel = $0.5C_g/\lambda$ of transistor width.

ndiff lumped with nchannel = $0.5C_g/\lambda$ of transistor width.

gate of nfet or pfet = $0.5C_g/\lambda$ of length where min width = 2λ.