A 21.8−27.5GHz PLL in 32nm SOI Using G_m Linearization to Achieve −130dBc/Hz Phase Noise at 10MHz Offset from a 22GHz Carrier

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***Abstract*—This paper describes a new approach to low phase noise LC VCO design based on transconductance linearization of the active devices. A prototype 25GHz VCO based on this approach is integrated in a dual loop PLL and achieves superior performance compared to the state of the art. The design is implemented in the 32nm SOI deep sub-micron CMOS technology and achieves a phase noise of −130dBc/Hz at 10MHz offset from a 22GHz carrier. Additionally, the paper introduces a new layout approach for switched capacitor arrays that enables a wide tuning range of 23%. More than 500 measurements across PVT variations validate the proposed PLL design: phase noise variation across 46 dies for 3 different frequencies is $\sigma <$ 0.6dB, across supply variation over 0.7−1.5V is 2dB and across 80°C temperature variation is 2dB. At the 25GHz center frequency, the VCO FOM_T is 188dBc/Hz.**

***Index Terms*—60GHz, phase noise, PLL, transconducance linearization, tuning range, VCO**

I. Introduction

Phase noise in CMOS LC VCOs is fundamentally limited by the oscillation amplitude, and the inherent device noise. In this work, we introduce a new approach based on *transconductance linearization* of the active devices that increases the signal swing while reducing the active device noise contribution in LC VCOs. Consequently, this provides a significant improvement in the VCO phase noise performance. We implement this approach using a signal feedback technique similar to that presented in [1]. Additionally, for the capacitor array, we utilize a new layout approach based on interconnect inductance mitigation. Using these novel approaches, we are able to globally optimize the VCO for phase noise, power, tuning range and PVT robustness. Consequently, the implemented PLL incorporating the resulting linear transconductance VCO (LiT VCO) achieves both an excellent measured phase noise of −130dBc/Hz at 22GHz (10MHz offset), and, in contrast to the 6.7% tuning range of the VCO-only result reported in [1], a large frequency tuning range (FTR) of 23% (21.8−27.5GHz). This range covers, with margin, operation over 22.8−26.4GHz, supporting 60GHz superheterodyne radios using a frequency doubler [2].

II. Transconductance Linearization

The oscillation amplitude in an LC VCO is limited by the non-linearity of the large signal device transconductance (G_m)[1]. The G_m vs. gate ac swing ($V_{g,sw}$) for a FET based cross-coupled VCO is shown in Curve I in Fig. 1. As shown, the G_m drops with increasing oscillation amplitude ($= V_{g,sw}$). The equilibrium amplitude, A_{XC}, is reached when $G_m.R_t = 1$. The main source of non-linearity is the transistor entering the triode region.

In contrast, if the VCO is designed to avoid the triode region, G_m is linearized. To achieve this in the LiT VCO, the LC tank is placed between the gates of the FET devices as shown in Fig. 2. The half circuit model for the VCO is shown in Fig. 3. The capacitive divider ensures that the drain swing is a fraction of the swing across the LC tank ($V_{g,sw}$), eliminating FET triode-operation. From Fig. 3,

$$V_d = \frac{V_t}{k}, \quad \text{where } k \approx \frac{C_c + C_d}{C_c} \tag{1}$$

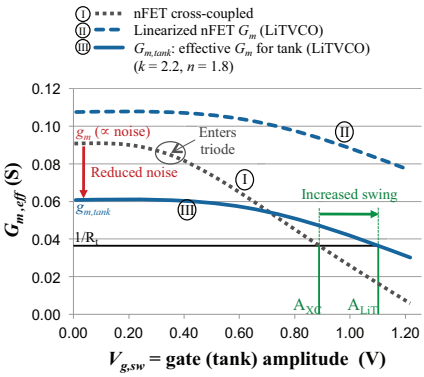


Fig. 1: Transconductance linearization in LiT VCO

Moreover, the capacitive dc isolation allows the FET gate ($V_{g,bias}$) to be biased lower than its drain (V_{DD}), further eliminating triode operation. Consequently, FET non-linearity is reduced, resulting in a more linear G_m as shown in Curve II in Fig. 1 for $k = 2.2$.

Also note that due to the capacitive division, only a part of the FET ac current flows into the tank as shown in Fig. 1. From Fig. 3, where I_d is the FET drain current, and I_t is the fraction of I_d flowing into the tank, at the resonant frequency,

$$I_t = \frac{I_d}{n}, \quad \text{where} \quad n = \frac{Z_{C_d} + Z_{C_c} + R_t}{Z_{C_d}} = \frac{C_c + C_d + R_t.sC_d.C_c}{C_c} \tag{2}$$

[1]Here, G_m is defined as $G_m = \frac{I_\omega}{V_\omega}$, where I_ω and V_ω are the ac drain current and ac gate voltage at the frequency of oscillation, ω.

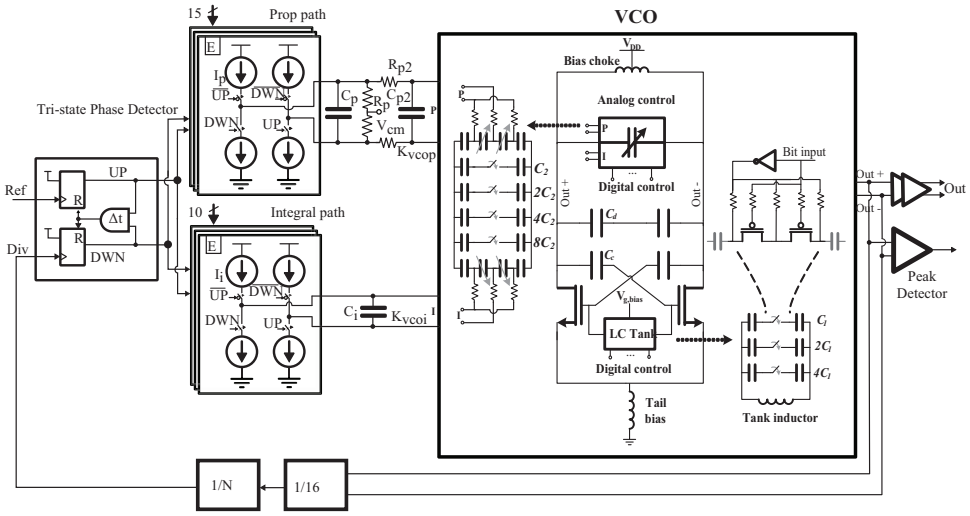


Fig. 2: Block diagram of the PLL showing the detailed VCO schematic including frequency tuning schemes

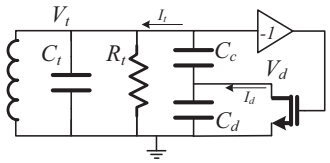


Fig. 3: An equivalent half circuit model of the LiT VCO showing the capacitive feedback technique employed (biasing details not shown)

This reduces the effective G_m (to $G_{m,tank}$) as plotted in Curve III in Fig. 1 for $k = 2.2$ and $n = 1.8$. The resulting oscillation amplitude, A_{LiT}, using curve III for the LiT VCO, is larger than A_{XC}, and results in improved phase noise performance in the LiT VCO.

As shown in Fig. 4, the larger oscillation amplitude can be viewed as a voltage limit extension in the LiT VCO. This enables a power vs. phase noise trade-off beyond the voltage limit imposed in a cross-coupled VCO.

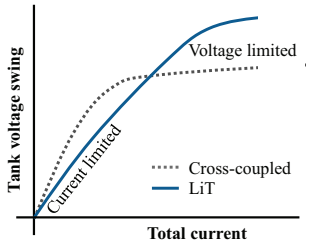


Fig. 4: Voltage limited regime extension in LiT VCO

Additionally, phase noise contribution from the FET is reduced: active device noise power at the oscillation zero crossings (when the oscillator's phase noise sensitivity is at its highest) is proportional to $g_m (= G_m(V_{g,sw} = 0))$. Note that for the LiT VCO, the effective transconductance across the tank ($g_{m,tank}$) is lower than the device g_m by n (i.e. $g_{m,tank} = g_m/n$). Therefore, at the zero crossings, the noise contribution of the active devices is reduced by the same amount as shown in Fig. 1. Additionally, by eliminating triode operation, the LiT VCO reduces degradation of the loaded tank Q. Consequently, the LiT VCO enables a larger tank amplitude and yet injects less noise into the tank as compared to the cross-coupled VCO leading to significant improvements in phase noise.

The foregoing theory of LiT VCO operation enables design optimization by utilizing additional power to enable a larger tank amplitude, lower noise injection and improved loaded tank Q as compared to traditional cross-coupled VCOs. Based on G_m curves as shown in Fig. 1, any cross-coupled VCO optimized using [3] can be converted into a LiT VCO design. The target amplitude of oscillation, A_{LiT}, can be maximized to the tolerable limits imposed by the technology. G_m curves can then be constructed for the active device for different combinations of k and n and a global optimum for power, phase noise, tuning range and robustness can be determined[2].

III. Implementation

The LiT VCO PLL shown in Fig. 2 has been implemented in IBM's 32nm SOI CMOS process. The PLL includes two differential control paths: an integral path comprising a charge pump and capacitor, and a proportional path comprising a charge pump and resistor. The LiT VCO design is optimized at $k = 2.2$ and $n = 1.8$ (Fig. 1). C_c, C_d and C_t are selected so as to obtain this k and n combination while adding minimum capacitive load on the tank.

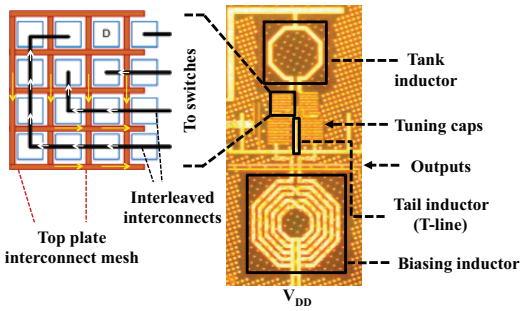
a) Tuning range: For the targeted 60GHz application, a large frequency tuning range (FTR) is a critical requirement [2]. We utilize switched capacitors on the drain and tank simultaneously (Fig. 2) to manipulate the feedback ratio and extend G_m linearization (and low phase noise performance) over a large FTR. At these high frequencies, a large FTR (in conjunction with a low K_{VCO}) also involves implementing

[2]For example, increasing k linearizes the G_m at the expense of power. Similarly, increasing n lowers the active device noise at the expense of power and start-up margin. Also, k and n are related through equations 1 and 2.

a large switched capacitor array in the tank. For optimal phase noise, a small inductor is utilized [3]. Consequently, the capacitor array and the inductor occupy comparable areas (Fig. 5) and the interconnect inductance significantly impacts VCO performance.

To avoid this problem in the LiT VCO, the interconnect parasitics are minimized. As shown in Fig. 5, the unit capacitors are arranged in a square, reducing the perimeter to area ratio of the structure. The top plates of the MIM-capacitors are connected using a mesh to reduce parasitics by parallelization. The bottom-plate interconnects are interleaved into the top plate mesh and carry an opposing current so that the resulting mutual inductance subtracts from the self-inductance of the interconnections. Consequently, compared to the 100pH tank inductor, the interconnects connecting the 70x80μm^2 capacitor array contribute only 12pH of inductance. By limiting the inductive parasitics, parasitic oscillation modes are eliminated, and a large tuning range of 23% is obtained.

Discrete frequency tuning is achieved using a 3-bit coarse and a 4-bit fine switched capacitor array (Fig. 2). Varactors are used for continuous tuning and provide around 100MHz analog tuning range achieving the desired low K_{VCO}.



Tank inductor inductance	100pH
Tank inductor area	80 x 80 = 6400μm^2
Cap array interconnect inductance	12pH
Capacitor array area	70 x 80 = 5600μm^2
Biasing inductor	6nH (300μm dia.)
T-line tail inductor	70pH

Fig. 5: Die photo of the LiT VCO showing the capacitor array design details for minimizing interconnect inductance, and other implementation details

b) Biasing: As shown in Fig. 2, an inductor is used to resonate out, at $2f_0$, the parasitic capacitance at the tail node. The resulting source degeneration at $2f_0$ reduces the G_m cell noise contribution when one transistor is in cut-off. The tail inductor is implemented using a transmission line to retain the symmetry in the LiT VCO layout (see Fig. 5). A DAC digitally controls the VCO gate bias for performance optimization. This bias control also eliminates the tail current source which can be a significant source of noise. Also, only a fraction of the noise from the biasing choke (6nH) (Fig. 4) flows into the tank reducing the total noise from the biasing circuitry in the LiT VCO as compared to the cross-coupled topology.

IV. Measurement Results

Measurement results from the PLL are plotted in Figs. 6−9. Fig. 6 shows the phase noise vs. frequency offset from a 22.6GHz carrier with −4.4dBm output power (single-ended). The differential output power is greater than 0dBm over the entire FTR.

Fig. 7 shows the measured phase noise @10MHz offset over the FTR for 3 dies at different radii on the wafer. The phase noise of the LiT VCO-based PLL varies from −130dBc/Hz at 22GHz to −126dBc/Hz at 27GHz. This performance is notably superior to other PLL's for 60GHz applications (Table I).

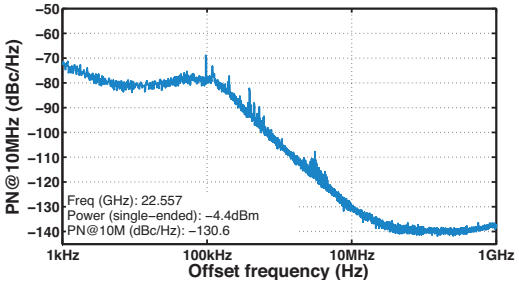


Fig. 6: Phase noise vs. frequency offset from a 22GHz carrier

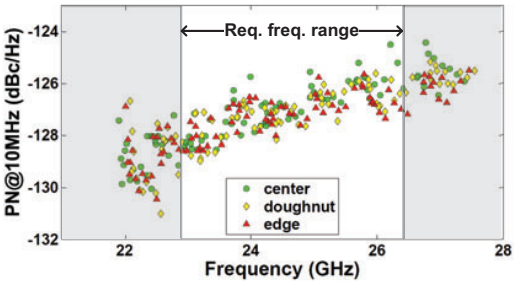


Fig. 7: Phase noise over the tuning range for different die locations on a wafer

The measured tuning range of 21.8−27.5 GHz covers the required range (22.8−26.4 GHz) and is shown in Fig. 8 over all 3-bit coarse tuning combinations. The resulting 23% FTR makes this a robust solution that is manufacturable in volume.

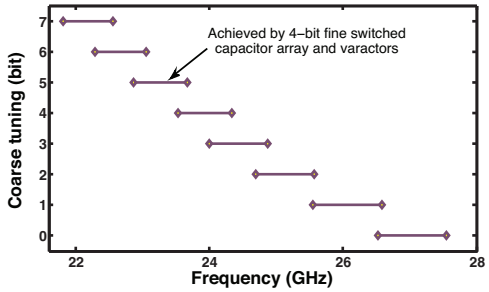


Fig. 8: Coarse frequency tuning showing frequency overlap

Die to die phase noise variation for 46 dies on a wafer is shown in Fig. 9(a). Measurements using 3 capacitor settings on each die are denoted by 3 different markers. All other settings are kept identical. The measured phase noise variation is $\sigma < 0.6$dB across all dies. The PLL's performance robustness across temperature at a fixed capacitor setting is shown in Fig. 9(b). The measured phase noise at 10MHz offset degrades

TABLE I: Table for comparison with other PLLs

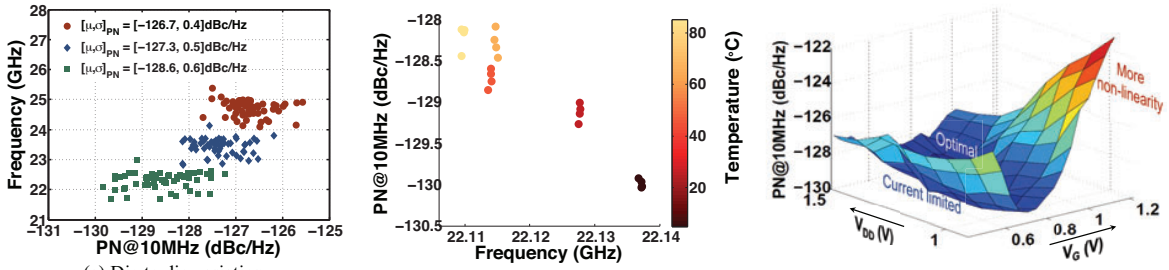
Ref	Floyd, JSSC 08 [2]	Osorio, et al. ISSCC 11 [4]	Richard, et al. ISSCC 10 [5]	Murphy, et al. JSSC 11 [6]	Scheir, et al. ISSCC 09 [7]	Pellerano, et al. ISSCC 08 [8]	This work
FTR (GHz) (f_{osc}) (GHz)	16.0-18.8 (17.4)	21.7-27.9 (24.8)	17.5-20.9 (19.2)	42.1-53.1 (47.6)	57.0-66.0 (61.5)	39.1-41.6 (40.4)	**21.8-27.5 (24.7)**
PN @10MHz from f_{osc} (dBc/Hz)*	-123.9	-121.0	-126.0 (@21GHz)	-117.5	-95.0	-112.0	**-127.3**
Technology (nm)	130 BiCMOS	45 CMOS	65 CMOS	65 CMOS	45 CMOS	90 CMOS	**32 SOI**
PLL power (mW)	144	40	80	72	78	64	**36‡**
PN @ 10MHz from 24.7GHz (dBc/Hz)†	-120.9	-121.0	-124.6	-123.2	-102.9	-116.3	**-127.3**
VCO tuning range (%)	16.5	25	17.7	23.1	14.6	6.2	**22.9**
VCO FOM_T (dBc/Hz)§	182.8	185.9	___	186.7	___	___	**188.6**

* Calculated assuming 20dB/decade degradation with offset frequency

† Calculated assuming 20dB/decade degradation with oscillation frequency

‡ Includes the consumption of the micro-controller and sensors for digital calibration and optimization; the VCO consumes 24mW

§ $FOM_T = L(\Delta\omega) - 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega} \cdot \frac{FTR}{10}\right) + 10 \cdot \log\left(\frac{P_{diss}}{1mW}\right)$ where P_{diss} is the VCO power dissipation



(a) Die to die variation (b) Temperature variation (c) Bias variation

Fig. 9: Robustness of the LiT VCO design to PVT variations

by 2dB from −130dBc/Hz at 5°C to −128dBc/Hz at 85°C. The center-band frequency drops by 30MHz.

The effect of varying V_{DD} and $V_{g,bias}$ on the phase noise is shown in Fig. 9(c). For low $V_{g,bias}$, the VCO is in the current limited regime. Phase noise initially improves with increasing $V_{g,bias}$ until the FET becomes non-linear due to triode operation (particularly for lower V_{DD}), after which the phase noise degrades. This demonstrates the effect of triode operation on LiT VCO phase noise. Finally, the PLL's measured phase noise varies by only 2dB across 800mV supply variation (from 0.7 to 1.5 V).

V. Conclusions

In this paper, a low phase noise VCO integrated in a dual loop PLL for 60GHz applications was presented. A novel G_m linearization technique was used to achieve a larger oscillation amplitude that, along with lower active device noise, resulted in significantly improved phase noise performance. Additionally, a new capacitor array layout approach was used to reduce interconnect inductance, enabling a large 23% FTR.

Table I compares the LiT VCO PLL performance at its center frequency (24.7GHz) with other PLLs designed for 60GHz applications. The LiT VCO PLL demonstrates the lowest phase noise of −127.3dBc/Hz at 10MHz from 24.7GHz, a large FTR of 23%, the lowest power consumption of 36mW and the best FOM_T of 188.6dBc/Hz compared to the other designs. Finally, measured results show the design is robust to process, temperature and supply variations and maintains excellent performance across all variations.

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