A 2.5Gb/s 0.38mm^2 Optical Receiver with Integrated Photodiodes in 0.18µm CMOS SOI

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Abstract — In this work, we report an optical receiver with integrated photodiodes operating at 850nm wavelength. The receiver achieves a data-rate of 2.5Gb/s without using any equalizer. To minimize the area, no inductors are used in the design. The entire receiver occupies an area of 0.38mm^2. This represents the smallest optical receiver operating at the Gb/s regime. The chip is fabricated in 0.18µm CMOS SOI process technology.

Index Terms — Optical Receiver, Integrated Photodiode, CMOS, Silicon Process.

I. Introduction

CMOS optical receivers with integrated photodiodes have recently attracted great interests [1-3]. In contrast with conventional optical receivers, where photodetectors and peripheral circuits are implemented separately and connected by bondwires, fully integrated receivers have both photodetectors and circuits fabricated on the same chip. This results in a higher performance due to the absence of parasitic inductance and capacitance caused by bondwires. In addition to parasitic elements of the bondwires, their length has to be precisely controlled to maintain an acceptable impedance matching in high frequencies. This limitation can significantly reduce the bandwidth, increase the cost, and limit the yield in high-volume production.

Although integrated optical receivers have been reported in the past [1-3], they have several limitations. In the prior art, bulk CMOS processes were utilized. In a bulk process, the slow diffusion current generated deep in the substrate limits the bandwidth of the photodiodes to MHz frequencies. In order to operate these bulk receivers at Gb/s rates, complicated equalizers are required. Equalizers increase the complexity of the design, area of the chip, and cost of fabrication. In addition to equalizers, in order to boost the amplifier bandwidth, the technique of inductive peaking has been widely used. In modern CMOS process technology, the area of a single inductor ranges from 0.01 to 0.1 mm^2. This large area per inductor increases the chip size and results in a higher fabrication cost.

In this work, we present a fully integrated CMOS optical receiver operating at 2.5Gb/s fabricated in a 0.18µm CMOS SOI process technology. The photodiode has a bandwidth of more than 9GHz, eliminating the need for equalizers. Furthermore, by carefully constructing feedback and negative capacitance circuits, an inductor-less architecture is realized. As a result, the entire receiver occupies a small area of 0.38mm^2. To the best knowledge of the authors, this is the smallest realization of a fully integrated optical receiver operating at the Gb/s regime.

The paper is organized as follows. Section II describes the design of the photodiode. Section III introduces the details of the receiver circuitry. Section IV reports the measurement results. Section V concludes the paper.

II. CMOS Photodiodes

In this work, in order to block the slow diffusion current generated deep in the substrate from the active channel, we utilize a CMOS SOI process. It has been reported that [4] photodiodes implemented in CMOS SOI processes are immune to the slow substrate current, as the active silicon region is separated from the substrate by a buried oxide layer.

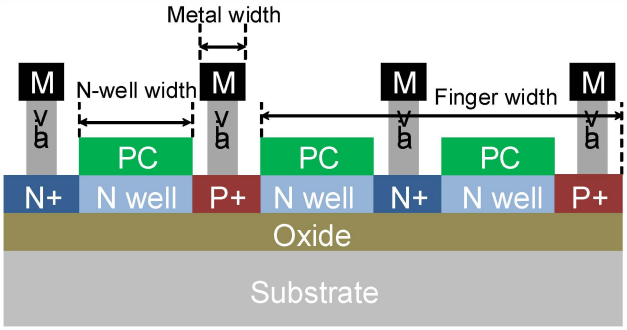

Figure 1: Cross section of the photodiodes used in this work. Here "M" refers to the first metal layer, while "PC" refers to the polysilicon layer.

The photodiodes used in this work are P+/N-well diodes with a cross section shown in Figure 1. The buried oxide layer has a thickness of 1µm. The thickness of the active silicon above the buried oxide layer is approximately 150nm. The polysilicon layer, shown in Figure 1, is used by the foundry for self-alignment purposes and does not impact the operation of photodiodes. In order to improve the responsivity, the metal filling above the photodiodes was blocked, and dummy metal structures are carefully added around the diodes to meet the metal density requirements.

In order to push the speed and responsivity of the photodiodes, their layout should be carefully designed [4, 5]. We have optimized the photodiode structure such that the N-well and finger widths are 0.36µm and 5.4µm, respectively. This photodiode occupies an area of approximately 40µm by 40µm. This area is chosen as a compromise between

responsivity and bandwidth. The measured responsivity of the photodiode is 15mA/W at a reverse bias of 9V. The intrinsic 3dB bandwidth is higher than 9GHz.

III. RECEIVER

The architecture of the receiver is presented in Figure 2. Two identical photodiodes are connected to differential inputs of a transimpedance amplifier (TIA) to maintain the symmetry and minimize the input offset. One of the photodiodes is exposed to the optical beam while the other one is blocked by a metal layer. A fully-differential TIA converts the input optical current to a differential voltage. An offset cancellation amplifier (A_{oc}) follows the TIA to cancel the DC offset between two differential branches. A four-stage limiting amplifier (LA) further amplifies the signal and an output buffer delivers the signal to a 50Ω load.

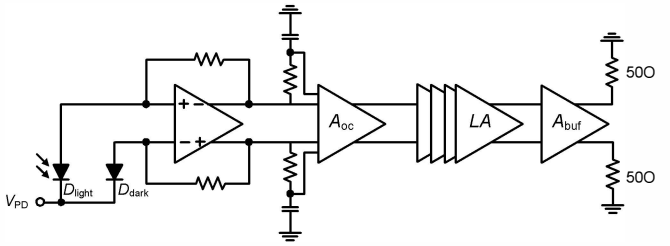

Figure 2: Receiver architecture

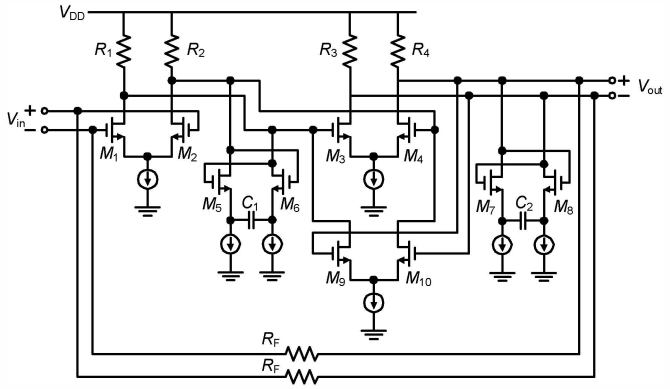

Figure 3: Schematic of the TIA.

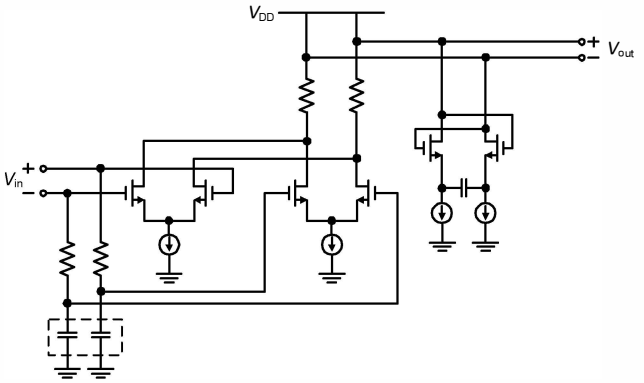

Figure 4: Schematic of the offset-cancellation amplifier.

The schematic of the TIA is presented in Figure 3. The transimpedance gain of the TIA is designed to be 62dBΩ. The TIA core consists of a two-stage differential amplifier. In order to increase the bandwidth, both active feedback and differential negative capacitance structure are used. The active feedback improves the gain-bandwidth-product of the amplifier by a factor of approximately f_T/f_{3dB}, where f_T is the cutoff frequency of the transistor and f_{3dB} is the bandwidth of the gain cell [6].

Next, the effects of the negative capacitance structure are discussed. In the cell that includes M_5, M_6, and C_1, the differential impedance looking into the drain of M_5 and M_6 is:

$$-\frac{2}{g_m}+j\frac{1}{\omega C_1} \qquad (1)$$

In equation (1), it is assumed that the parasitic capacitance of the transistors and the channel-length modulation are negligible. In this equation, g_m is the transconductance of M_5 and M_6. This impedance can be considered as a series combination of a negative resistance ($-2/g_m$) and a negative capacitance ($-C_1$). In this design, g_m is maximized such that ($-2/g_m$) is much smaller than the imaginary part, and hence can be neglected. Assuming the original load capacitance is C_L, the addition of the negative capacitance will reduce the load capacitance to (C_L-C_1) and boost the bandwidth of the TIA core amplifier by a factor of $C_L/(C_L-C_1)$.

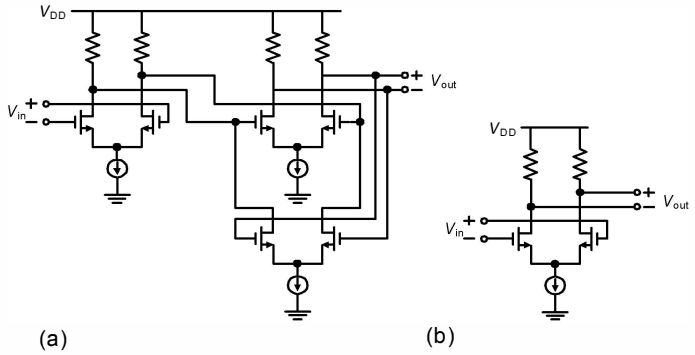

Figure 5: Schematic of the (a) gain cell of the limiting amplifier, and (b) output buffer.

In Figure 4 we present the schematic of the offset-cancellation amplifier, which consists of two differential amplifiers with common-source topology. The capacitor and the resistor at the input behave as a low-pass filter. The capacitors (shown in the dashed box) have a value of 1μF and are implemented off-chip. The on-chip resistors have a value of 1kΩ, setting the cutoff frequency of the low-pass filter to 160Hz. Under this configuration, the DC and low-frequency part of the input signal will be cancelled. It is important to set the cutoff frequency of the filter low enough to minimize the impact on the bit error rate. At the output of the offset-cancellation amplifier, a negative capacitance cell is used to increase the bandwidth.

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In Figure 5(a) the gain cell of the Limiting Amplifier (LA) is shown. The LA consists of four gain cells with a total gain close to 30dB. The design for the gain cell is shown in Figure 5(a). Each gain cell consists of two-stage differential amplifier with common-source topology. To push the bandwidth, an active feedback circuit is used. Finally, the schematic of the output buffer stage is shown in Figure 5(b). This amplifier uses a common-source topology.

IV. Measurement Results

The chip micrograph is presented in Figure 6. The entire receiver occupies an area of 440µm by 860µm (including the pads). The chip is fabricated in IBM 7RFSOI 0.18µm process technology. The receiver uses a supply voltage of 2.5V. The photodiodes are biased at -9V to maximize the bandwidth and responsivity. The total power consumption of the receiver is 165mW.

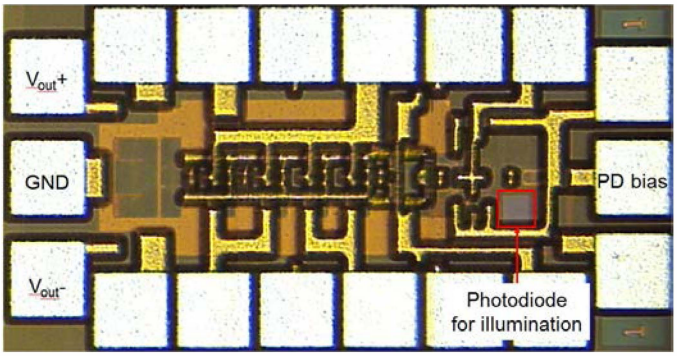

Figure 6: Micrograph of the chip.

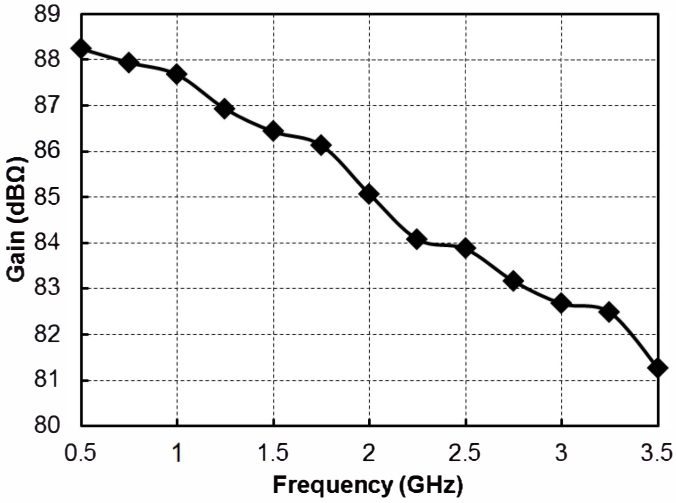

Figure 7: Measured conversion gain.

The measured conversion gain of the receiver versus frequency is plotted in Figure 7. A directly-modulated 850nm 14Gb/s Vertical Cavity Surface Emitting Laser (VCSEL) ULM850-14-TT-N0101U with 50Ω input impedance is used as the optical source. The laser beam is coupled to a multimode fiber and directed to the photodiode from the top of the chip. An Agilent network analyzer, N5230C, is used to measure the transmission coefficient, S_{21}, as a function of frequency, where port 1 modulates the VCSEL and port 2 monitors the output of the receiver. The measured S_{21} is then converted into the conversion gain. As shown in Figure 7, the conversion gain of the entire receiver is 88dBΩ with a 3dB bandwidth of 2GHz.

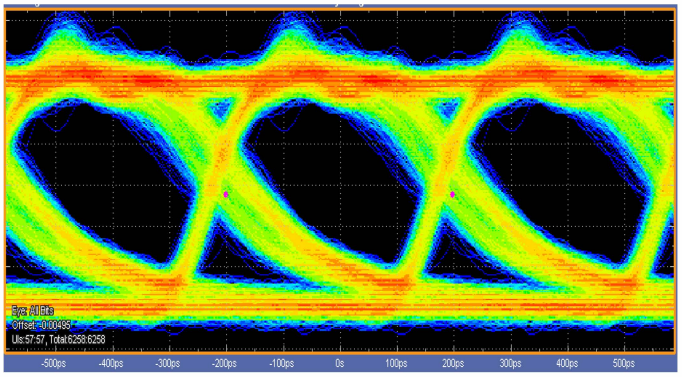

Figure 8: Measured eye diagram at 2.5Gb/s.

Spec	[1]	[2]	[3]	This work
Speed (Gb/s)	1.8	2.5	4.5	2.5
Area (mm^2)	4.5	0.53	1.77	0.38
Process	0.18µm	0.18µm	0.13µm	0.18µm

Table 1: Comparison with the prior art.

The eye diagram of the receiver is measured using a Tektronix oscilloscope DSA70804B. A Tektronix arbitrary waveform generator AWG7122C is used to generate a 2^7-1 PRBS test pattern. In Figure 8, the measured eye diagram at a bit rate of 2.5Gb/s is reported. The laser power is kept constant at -1dBm. The bit error rate is also measured using an Agilent bit error rate tester N4903B. At a bit rate of 2.5Gb/s and an input laser power of -1dBm, a bit error rate of lower than 10^{-10} is measured. The performance comparison between the proposed receiver and the prior art is shown in Table 1. It is observed that due to the lack of inductor and equalizer, the reported receiver occupies the smallest area.

V. Conclusion

In this work, we report a fully integrated optical receiver that achieves a data rate of 2.5Gb/s. The receiver operates at wavelength of 850nm. The custom on-chip photodiodes achieve an intrinsic 3dB bandwidth of higher than 9GHz, eliminating the need for equalizers. Moreover, the reported receiver adopts an inductor-less design by carefully incorporating the active feedback and negative capacitance circuits. Therefore, the entire chip only occupies an area of $0.38mm^2$, representing the smallest optical receiver operating at the Gb/s regime.

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