

A 30GHz Impulse Radiator with On-Chip Antennas for High-Resolution 3D Imaging

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Abstract — This paper reports a 30-GHz impulse radiator utilizing an injection-locked asymmetric cross-coupled voltage-control-oscillator (VCO) with on-chip bow-tie antennas. The impulse radiator converts a digital trigger signal to a radiated impulse with a variable pulse-width down to 60psec with peak EIRP of 15.2dBm without using any lens. Coherent spatial pulse combining is demonstrated by using two widely spaced radiators. A timing jitter of the 216fsec for the combined signal is measured. The impulse radiator has the capability of producing 3D images with depth resolution of 33 μ m at 25cm of target distance in the air. The chip is implemented in a 0.13 μ m SiGe BiCMOS process technology. The total die area is 2.85mm² with maximum power consumption of 106mW.

Index Terms — 3D impulse imaging, BiCMOS, Coherent spatial pulse combining, impulse radiator, VCO.

I. INTRODUCTION

During the last decade, impulse radiators have been proposed for medical imaging, spectroscopy, and gesture recognition [1]. Higher resolution, higher signal-to-noise ratio (SNR), and fast image acquisition are the main objectives in the roadmap of silicon-based integrated imaging radars. However, there exists a trade-off in designing impulse-based imaging radars: a shorter impulse provides higher resolution but lower SNR. Coherent spatial combining provides a solution to the problem. In coherent spatial combining, the phase (starting time) of the radiated impulses has to be locked to the reference signal with low timing jitter. In [1], timing coherency is achieved by a co-locked PLL and delay-locked loop, but the architecture dramatically increases the complexity, power consumption, and die area of the system. In [2], the authors did not provide a solution to locking the phase of the radiated pulses. In the prior work [2]-[3], off-chip antennas, bulky auxiliary lenses or reflectors, and mechanical scanners are required to capture images.

In this paper, we propose a novel impulse radiator with injection-locked asymmetric cross-coupled VCO operating at 30GHz. The proposed impulse radiator has the capability to lock the phase of the radiated pulses with improved accuracy and smaller die area compared with the prior work [1]-[3]. In this work, 3D images are captured by a coherent impulse radiator array with depth resolution of 33 μ m at 25cm of target distance.

The remaining part of this paper is organized as follows: Section II describes the circuit topology for the proposed

impulse radiator. Section III provides the measurement results. Section IV demonstrates the 3D images captured by the proposed impulse radiator. Finally, Section V concludes the paper.

II. SYSTEM ARCHITECTURE

Impulses can be generated by modulating voltage-controlled oscillators (VCO). Conventional cross-coupled VCOs employ a symmetric topology. However, due to the symmetric topology of the VCO core, when modulated by a digital trigger signal, the starting phase of the impulse is random because the differential component of the noise at the VCO core sets the starting phase of the oscillation. Unlike symmetrical VCOs, the starting phase of the impulse generated from the proposed asymmetric VCO is set by deterministic differential DC component at the VCO core. Therefore the phase of the radiated impulse is locked to the arrival time of the trigger signal. By changing the trigger signal, this topology enables a pulse-width-tunable and pulse-position-tunable impulse radiator.

As shown in Fig. 1, the proposed impulse radiator consists of four blocks: a digital buffer, an asymmetric cross-coupled VCO, a power amplifier (PA), and broadband bow-tie antennas. A trigger signal is fed to the input of a CMOS buffer. The input impedance of the buffer is designed to be 50 Ω to minimize the reflection and ringing of the trigger signal. The buffer sharpens the trigger signal and turns on the current source (transistor M_1 in Fig. 1) of the asymmetric cross-coupled VCO. Turning on the current source causes VCO to oscillate. To minimize the timing jitter induced by the VCO, the emitter lengths of bipolar transistors M_2 and M_3 (Fig. 1) are chosen to be 15.6 μ m and 5.2 μ m. Two neutralization capacitors C_1 and C_2 are used to increase the voltage swing of VCO and consequently reduce jitter. At the core of oscillator, two varactors are used to tune the oscillation frequency. An impedance matching network, consisting of a differential transmission line TL_1 , C_3 and C_4 , enables maximum power delivery from VCO to the following PA and also provides required inductance for oscillation. To minimize the loading effect of the following PA, the capacitance of C_3 and C_4 are kept below 200fF respectively. The load-pull approach is used to maximize the output power of PA and PAE. Preceding the on-chip bowtie antennas, a revised single-stub shunt-matching

network (TL2, TL3, C5 and C6) is inserted at the collector nodes of power transistors (M4 and M5). The capacitors C5 and C6 enable the matching solution with shorter transmission lines. Therefore this network mitigates the insertion loss of matching and consequently improves the gain of the amplifier and PAE.

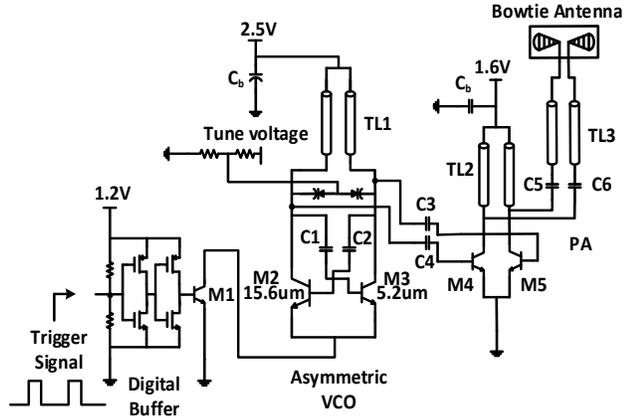


Fig. 1. The proposed impulse radiator with an asymmetric cross-coupled VCO and on-chip bow-tie antennas.

The on-chip bow-tie antennas are designed for broadband operation. Both the antenna geometry and thickness of the silicon substrate are carefully chosen to suppress the substrate modes, thereby increasing the radiation efficiency. A moment-based electromagnetic simulator, HyperLynx 3D, is used to simulate the bow-tie antennas. The peak radiation efficiency of the antennas is 19.1% at 30GHz. In order to maximize the radiated power, the chip radiates from the back-side (substrate side). Unlike prior art [4], no silicon-lens is used in this design.

III. MEASUREMENT RESULTS

In order to capture radiated impulses without adding distortions, a broadband custom receiving antenna is designed to provide flat gain and constant group delay. The receiving antenna is connected to a sampling oscilloscope (Agilent DCA-X 86100D). The chip is fed by a tunable trigger signal generated by a Tektronix Arbitrary Waveform Generator (AWG) 7122C.

By tuning the duty-cycle of the digital trigger signal, the width of the radiated impulses can be varied. The chip is capable of radiating short impulses with minimum width of 60ps and maximum peak EIRP of 15.2dBm (Fig. 2(a)). Fig. 2(b) shows the measured radiation pattern at 30GHz, which has a directivity of 6dBi.

To verify the coherency of radiated impulses, coherent spatial pulse combining is demonstrated. Two widely-spaced radiators are used to combine their radiated impulses in the far-field without using any focusing lens.

The AWG generates two synchronized digital trigger signals; it can shift them with respect to each other with a resolution of 1ps. As shown in Fig. 3, the amplitude of the combined impulse is very close to the algebraic sum of two individual impulses. The measured RMS jitter of the combined impulse is better than 216fsec when the injected trigger signal has an RMS jitter of 150fsec.

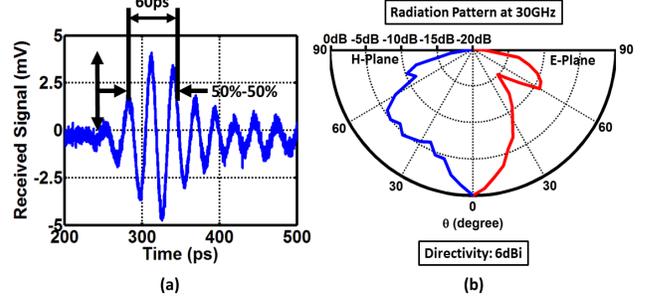


Fig. 2. (a) The measured waveform of 60ps radiated impulse. (b) The measured radiation pattern at 30GHz.

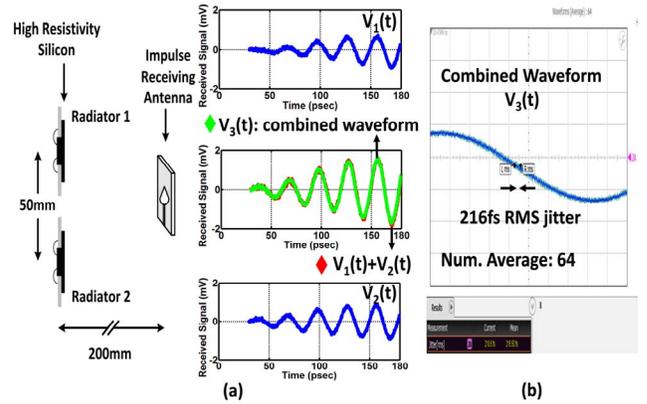


Fig. 3. (a) The measured coherent spatial pulse combining of two widely-spaced radiators and the measurement setup. (b) The measured jitter of combined impulse.

IV. 3D IMAGING BY USING A COHERENT IMPULSE RADIATOR ARRAY

A coherent impulse radiator array with N -elements, can improve the total peak radiated power by a factor of N^2 , thereby increasing SNR dramatically. In this work, 3D images are captured using an effective 9-by-9 impulse radiator array. A single radiator is moved to 81 locations and the reflected impulses from the objects are captured at each location. With grid spacing of 5mm, an effective aperture size of 4cm \times 4cm is achieved.

The objects used for 3D imaging include one small cylindrical aluminum foil (radius=1cm), two spaced cylindrical aluminum foils, and one large aluminum foil ring. The chip emits 60ps impulses with repetition period of 3ns. The target distance is 25cm ($Z=25$ cm). By postprocessing the received impulses from 81 locations, 3D images are generated. As shown in Fig. 4, at $Z=20$ cm,

TABLE I
COMPARISON WITH STATE-OF-THE-ART MICROWAVE 3D IMAGING RADIATORS

	This Work	[1]	[2]	[3]
Radiator Type	Pulsed	Pulsed	Pulsed	Phase
Frequency	30GHz	94GHz	94GHz	144GHz
RMS Jitter	<216fsec	1.2ps	N/A	N/A
Coherent Spatial Combining	Yes	N/A	N/A	N/A
3D Imaging Performed	Yes	No	Yes	Yes
Lens/Reflector	No	No	14cm-diameter Lens	Dish Reflectors
Pulse Duration	60ps (tunable)	36ps	3.5ns	N/A
Depth Resolution	33μm	0.39mm	0.1cm	0.76cm
Chip Area	2.85mm²	6.16mm ²	7.56mm ²	4.38mm ²
Power Consumption	106mW*	580mW	960mW	457mW
Technology	130nm SiGe BiCMOS	130nm SiGe BiCMOS	65nm CMOS	65nm CMOS

* The power consumption with maximum peak EIRP

no object is detected. At $Z=25\text{cm}$, which is the exact Z -coordinate of the objects, the produced images show the shape of the objects. The 216fsec RMS jitter of the radiated impulses corresponds to a depth-resolution of $33\mu\text{m}$ in the air. Unlike prior art [2]-[3], these high-resolution images are produced without using any lenses or reflectors. To the best of the authors' knowledge, this work presents the highest resolution ever achieved for a silicon-based lens-free integrated imaging system. Table I compares this work with the prior art.

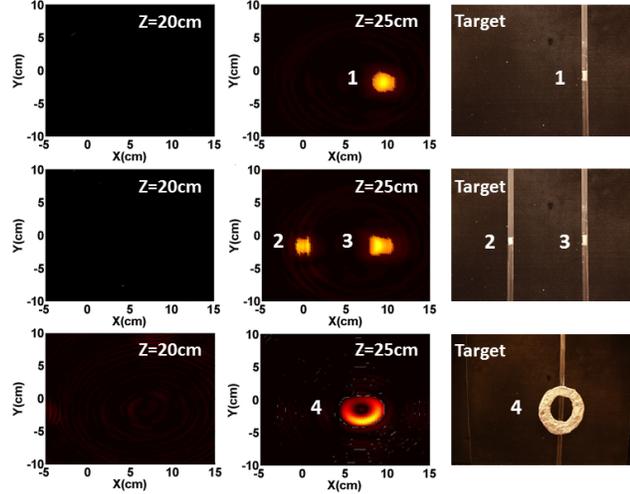


Fig. 4. Captured 3D images of three scenarios.

V. CONCLUSION

In this paper, an integrated impulse radiator is reported. The radiator comprises a digital buffer, an injection-locked asymmetric cross-coupled VCO, an integrated PA, and on-chip bow-tie antennas. It radiates impulses with a variable pulse-width down to 60psec with peak EIRP of 15.2dBm. The measured timing jitter of the radiated impulses is 216fsec when a reference signal with jitter of

150fsec is used. A 3D imaging system is built based on the impulse radiator and it generates high-resolution 3D images with depth resolution of $33\mu\text{m}$ at 25cm of target distance in the air. The reported radiator is fabricated in a 130nm SiGe BiCMOS process technology, with a size of $1.89\text{mm}\times 1.51\text{mm}$, as shown in Fig. 5.

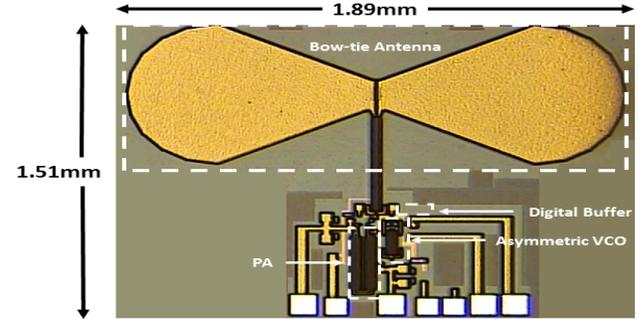


Fig. 5. Micrograph of the chip.

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