A Fully-Integrated Digitally-Programmable 4×4 Picosecond Digital-to-Impulse Radiating Array in 65nm Bulk CMOS

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Abstract — In this paper, a fully-integrated 4×4 digital-to-impulse radiating array with a programmable delay at each element is reported. Coherent spatial combining from 16 elements is successfully demonstrated. The combined signal from 16 elements achieves a jitter of 230fsec, a pulse width of 14psec, and an EIRP of 17dBm. Each array element is equipped with an 8-bit digitally-programmable delay that provides a step resolution of 200fsec and a dynamic range of 20psec. The chip is implemented in a 65nm bulk CMOS process.

Index Terms — Direct Digital-to-Impulse (D2I) Transmitter, Picosecond Pulse Radiation, On-Chip Antenna, Coherent Spatial Combining, Programmable Delay Generator, Slot Bow-Tie Antenna, Bulk CMOS, Silicon.

I. Introduction

In the last few years, there has been a growing interest for generation and radiation of ultra-short impulses in silicon. These impulses can be used in 3D imaging radars, spectroscopy, high-speed wireless communication, and precision time/frequency transfer. They should be very short in time and provide a large peak power. Their pulse width limits the depth resolution, and their peak power determines the transmission range. Impulse generation methods can be divided into two main categories. In the first category, a continuous-wave signal is generated on-chip and a switch is used to modulate the amplitude of the continuous-wave and convert it to a train of short impulses. The shortest radiated impulse reported with this method is 26psec, which was based on a noisy envelope of the radiated signal [1]. The second category is based on the technique of direct digital-to-impulse (D2I) radiation, which was introduced in [2-3], for the first time. In this technique, no on-chip oscillator was used. Instead, a fast trigger signal is generated and used to release the DC energy stored in a broadband on-chip antenna.

In [2], radiation of 9-psec impulses using an on-chip differential inverted-cone antenna was reported. In [3], 8-psec impulses were radiated using an on-chip slot bow-tie antenna. The work in [2-3] was based on a single element, and no on-chip delay control was implemented. Furthermore, the impulse radiators reported in [2-3] were fabricated in a 130nm SiGe BiCMOS process.

In this work, for the first time, a 4×4 digital-to-impulse radiating array is reported in CMOS. The array has the ability to control the delay at each individual element. Each element includes a broadband on-chip impulse antenna, a fast trigger generation block, and a programmable delay. The on-chip impulse antennas are based on a slot bow-tie topology. Each antenna radiates impulses with a minimum duration of 14psec and a repetition rate of up to 10GHz. The radiated impulses are locked to an external digital trigger, with timing jitter of better than 230fsec. This low level of timing jitter and the ability to program the delay at each element enable a near-ideal spatial combining with beam steering capability.

Each individual element of this array is equipped with an integrated programmable delay that shifts the timing of the digital trigger by fine steps of 200fsec and a dynamic range of 20psec. A 128-bit serial digital input sets the timing of the impulses radiated by all elements. The radiated impulses from the entire array are successfully measured and reported.

It is demonstrated that the radiated impulses from 16 elements can be coherently combined in space. Furthermore, it is shown that timing control at each element is necessary to precisely align the radiated impulses at a desired direction in space.

This paper is organized as follows. Section II introduces the circuit architecture; section III reports the measurement results, and section IV concludes the paper.

II. Circuit Architecture

The architecture of the 4×4 array is shown in Fig. 1 and the block diagram of a single element is presented in Fig. 2. A

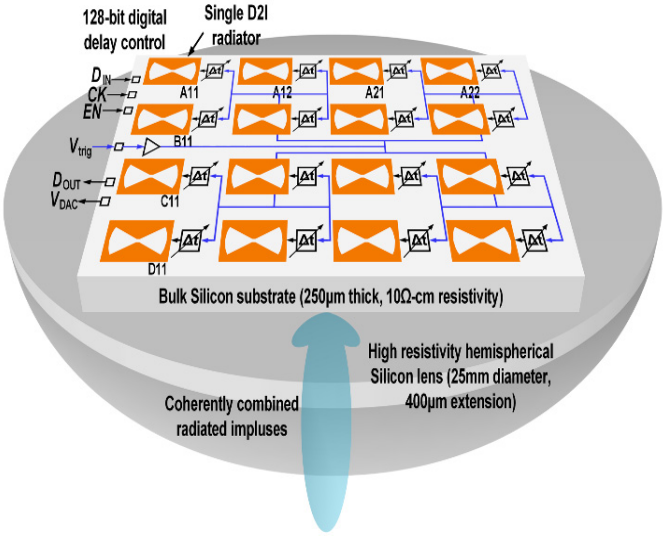

Fig. 1. Architecture of the 4×4 digital-to-impulse radiating array

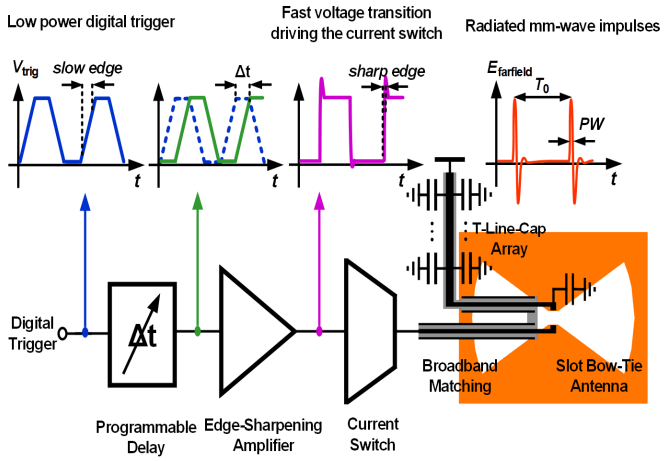

Fig. 2. Block diagram of a single array element

digital trigger with a rise time of 150-psec is fed to the input and distributed to all 16 elements using an equidistance H-tree distribution. At each element, a series of digital buffers reduces the rise/fall time of the trigger signal to less than 30psec and sends it to a programmable delay element. After adjusting the delay, the trigger signal is sent to an edge-sharpening power amplifier to further reduce the rise/fall time and increase its amplitude. Then it is fed to a cascode switch. The switch is connected to an on-chip antenna through impulse matching circuitry. When the switch is turned On, the impulse antenna and the pulse matching circuitry are energized by storing a DC current. When the switch is turned Off, the energy stored in the antenna is released and converted to impulse radiation. A broadband slot bow-tie antenna is designed to radiate ultra-short impulses.

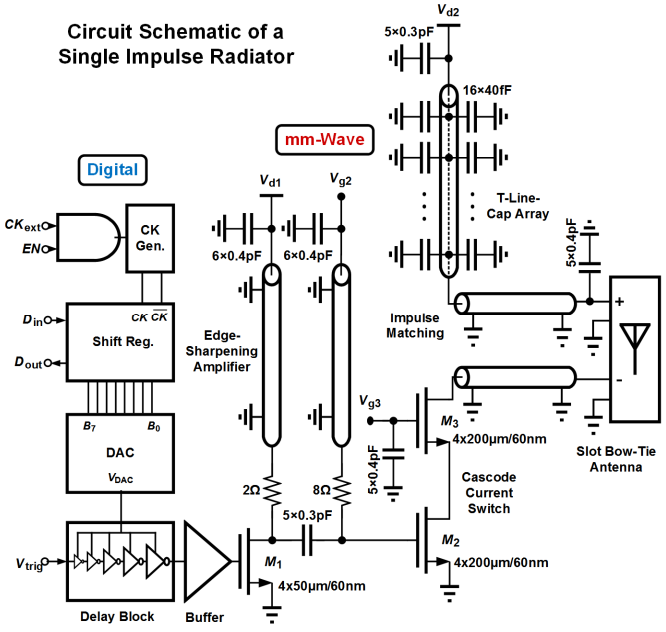

Fig. 3. Circuit schematic of a single impulse radiating element

In the proposed topology, each individual radiator can operate in two modes. In the first mode, a positive impulse is radiated that is locked to the rising edge of the digital trigger. In the second mode, a negative impulse is radiated and locked to the falling edge of the digital trigger. As shown in Fig. 3, the voltage at node V_{g2} activates one or both of these modes. The control voltage V_{d1} modulates the peak amplitude of the radiated impulse. A distributed network of bypass capacitors is used at the biasing nodes to ensure fast delivery of charges at the time of switching. The slot bow-tie antennas are fabricated using a copper metal layer. The edges of the antennas are curved to achieve larger bandwidth and smaller peak resistance. The antenna is coupled to a silicon lens that has a diameter of 25mm and an extension length of 0.4mm. The lens has a resistivity of 10KΩcm. The silicon lens increases the radiation efficiency by minimizing the substrate modes and reducing the ringing effects.

The delay of the trigger signal at each element is controlled using 8-bit serial data. Fig. 3 also shows the schematic of the programmable delay generator used at each element. Digital delay control is achieved by adjusting the supply voltage of a series of NOT stages through an on-chip DAC.

III. Measurement Results

One of the major challenges in measurement of ultra-short impulses is the receiver. As described in [2-3], the receiving antenna should have a flat gain and a linear phase (constant

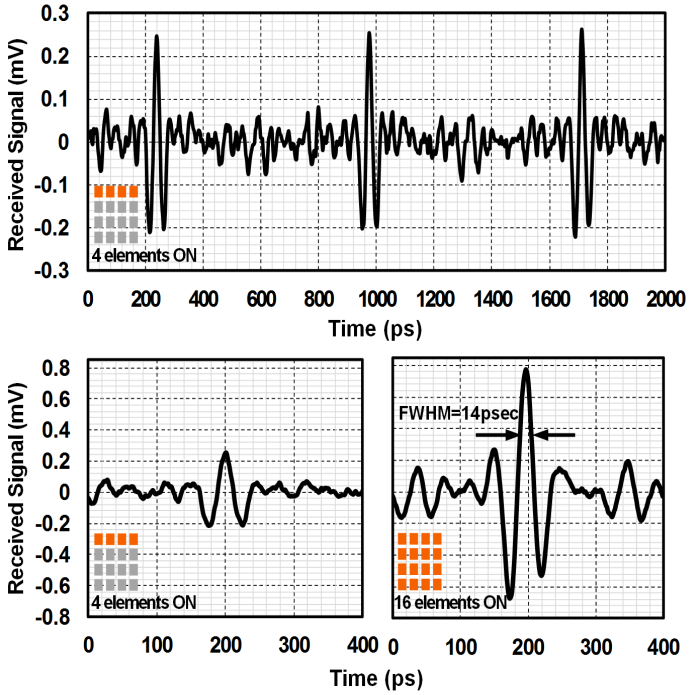

Fig. 4. Measured time-domain waveforms by the sampling oscilloscope (raw data) from 4 and 16 elements. Due to the variation in the amplitude of radiation from different elements, in these plots, the combined amplitude of 16 elements is not equal to four times the amplitude of 4 elements.

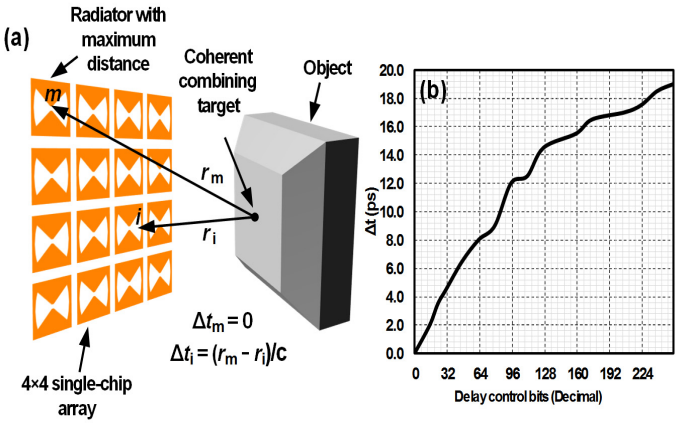

Fig. 5. (a) An illustration of the coherent combining of the radiated impulses (b) Measured delay at each element versus the digital input

group delay) in a wide range of frequencies. In this work, a custom PCB-based impulse receiving antenna was fabricated and used at the receiver. This antenna was directly connected to a wideband sampling oscilloscope (Agilent DCA86100 with sampling head 86118A). In contrast with [2], no mm-wave lens is used to focus the power onto the PCB antenna. Using a center frequency of 40GHz and the Friis equation, a peak EIRP of 17dBm for the combined signal from 16 elements is calculated. Fig. 4 shows the time-domain waveforms of the radiated signals from 4 and 16 elements. In this measurement, in order to

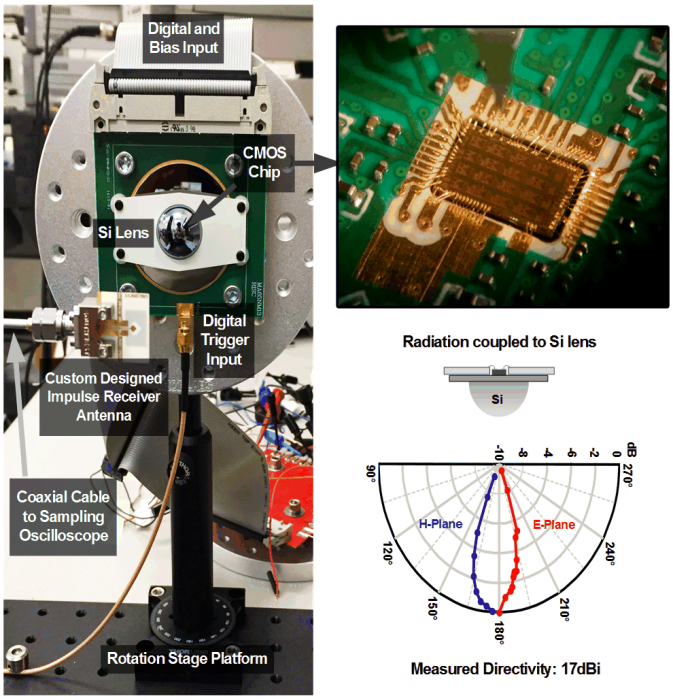

Fig. 6. Measurement setup (left) and radiation pattern of the digital-to-impulse array (right)

coherently combine the signal from 16 elements, individual delays are tuned to maximize the amplitude.

The measured dynamic range of the delay generators at each element was 20psec. Fig. 5. (b) reports the measured delay versus the digital input in one of the elements and illustrates the effect of the delay in coherent combining of the impulses at a desired location in 3D space. Considering the size of the chip, the farthest distance between two elements is 2.4mm (8psec in air). Therefore, the dynamic range of 20psec is sufficient to enable beam steering in all angles.

Fig. 6 shows the H-plane and E-plane radiation patterns of the combined signal from 16 elements. The peak power of the received signal is used to measure the radiation pattern. It is confirmed that the pulse width is conserved in different angles. The measured directivity of the array is 17dBi. A photo of the measurement setup is also shown in Fig. 6.

To assess the quality of the coherent combining, the jitter of the combined signal from all 16 elements was measured and reported in Fig. 7. The measured RMS jitter with averaging of 64 and 128 was 230fsec and 150fsec, respectively. Averaging was used to reduce the noise of the sampling head in the oscilloscope.

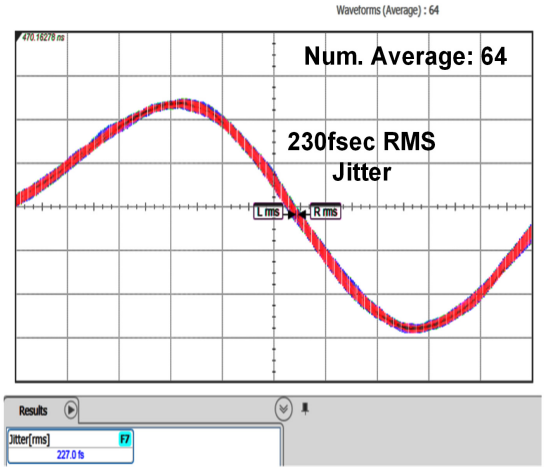

Fig. 7. Jitter of the received combined signal from 16 elements

Table I summarizes the performance of the digital-to-impulse radiating array and Fig. 8 shows a die photo of the chip. The chip was fabricated in IBM 65nm bulk CMOS process technology.

IV. Conclusion

To the best knowledge of the authors, this is the first digital-to-impulse radiating array. All 16 elements of the array are equipped with a programmable delay generator. Coherent spatial combining from 16 elements is successfully demonstrated. The combined signal from 16 elements achieves

TABLE I
PERFORMANCE SUMMARY OF THE CHIP AND COMPARISON WITH PRIOR ART

	This work	[1] JSSC 2013	[2] RFIC 2014	[3] IMS 2014	[4] JSSC 2014
Shortest radiated pulse	**14ps**	26ps	9ps	8ps	100ps
Peak EIRP	**17dBm**	13dBm	10dBm	13dBm	18.8dBm
Phase synchronization with an external reference	**Yes**	No	Yes	Yes	No
Number of array elements	**16**	1	1	1	4
Array architecture	**D2I array** **(broadband)**	N/A	N/A	N/A	Phased-array (LO-path phase shifting, narrowband)
Delay resolution (per element)	**200fs**	N/A	150fs	N/A	5° at 40GHz LO (350fs)
Delay range (per element)	**20ps**	N/A	400ps (off-chip delay line)	N/A	90° at 40GHz LO (6.25ps)
Pulse generation method	**Direct Digital-to-Impulse (D2I)**	Oscillator-based	D2I	D2I	Oscillator-based
TX/RX	**Only TX**	TX/RX	Only TX	Only TX	TX/RX
Power consumption	**650mW**	739mW	260mW	220mW	1.2W
Technology	**65nm CMOS**	0.13µm SiGe	0.13µm SiGe	0.13µm SiGe	65nm CMOS
Die area	**6.6mm²**	1.2mm²	0.88mm²	0.47mm²	20mm²

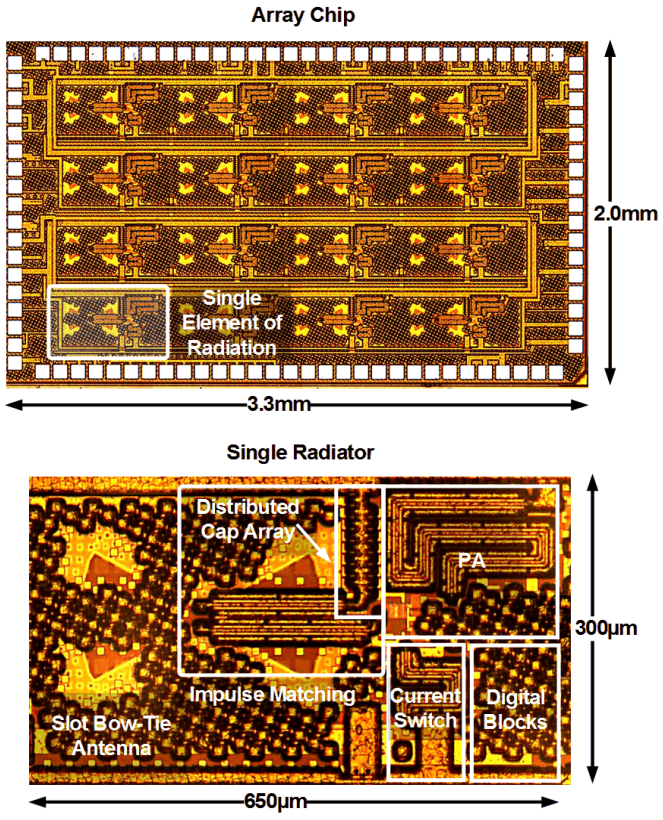

Fig. 8. A die photo of the 4×4 impulse radiating array (top) and a zoomed image of a single element (bottom). Fill blocks are placed at the corners of the slot bow-tie antenna where the sensitivity to parasitic capacitance is maximum.

a jitter of 230fsec, a pulse width of 14psec, and an EIRP of 17dBm. Each delay generator provides a delay resolution of 200fsec and a dynamic range of 20psec.

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