A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas

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Abstract—In this paper, we present the receiver and the on-chip antenna sections of a fully integrated 77-GHz four-element phased-array transceiver with on-chip antennas in silicon. The receiver section of the chip includes the complete down-conversion path comprising low-noise amplifier (LNA), frequency synthesizer, phase rotators, combining amplifiers, and on-chip dipole antennas. The signal combining is performed using a novel distributed active combining amplifier at an IF of 26 GHz. In the LO path, the output of the 52-GHz VCO is routed to different elements and can be phase shifted locally by the phase rotators. A silicon lens on the backside is used to reduce the loss due to the surface-wave power of the silicon substrate. Our measurements show a single-element LNA gain of 23 dB and a noise figure of 6.0 dB. Each of the four receive paths has a gain of 37 dB and a noise figure of 8.0 dB. Each on-chip antenna has a gain of +2 dBi.

Index Terms—BiCMOS, dielectric lens, integrated circuits, on-chip dipole antennas, phased-array, silicon germanium, surface wave.

I. INTRODUCTION

SILICON technology has entered the realm of millimeter-wave frequencies by the sheer force of transistor scaling, unmatched levels of integration, low cost, and high yield. This has opened the door to a plethora of new applications, formerly accessible only to III-V semiconductors. There are several frequency bands in the millimeter-wave (mm-wave) range which have been approved by Federal Communications Commission (FCC) for wireless communications and automotive radar. These include the 24.05–24.25 GHz[1] and 57–64 GHz bands for high speed wireless communications, and the 22–29 GHz and 76–77-GHz bands for automotive radar. Although the current industrial efforts at 77-GHz range are focused on automotive radar, a mm-wave wireless system can also be used for other applications, such as short-range surveillance, microwave imaging, and ultra-high-speed data transmission. Recently, several silicon-based systems have been reported that operate at these frequencies [2]–[5].

[1]Although technically speaking the millimeter frequency range starts at 30 GHz, the behavior and general considerations for 24-GHz systems are close enough to 30 GHz to be considered in that category for the purposes of our discussions.

Automobile radar operating in the 77-GHz frequency band is one such application as the 76–77-GHz band has been allocated for this purpose in many countries around the world [6]. Also, the Electronic Communications Committee (ECC) within the European Conference of Postal and Telecommunications Administrations has allocated the 77–81 GHz window for the automotive UWB short-range radar [7]. Compared to the radar bands at lower frequencies, such as the 22–29 GHz band, operating at 77-GHz band is more compatible with other applications in the nearby frequency spectrum. Meanwhile, the effective wavelength at 77 GHz on silicon is on the order of a millimeter which makes possible on-chip antennas that can significantly improve system reliability and repeatability, while lowering the cost by eliminating the last mm-wave electrical interfaces to the chip.

The objective of this work is to demonstrate a general purpose low-cost fully integrated phased-array receiver operating at 77 GHz using an on-chip antenna array. Besides implementing antennas on highly conductive silicon substrate, other design challenges of the system include a low-noise front-end, efficient and accurate phase shifting and signal combining, as well as high-speed frequency generation and distribution.

Historically, III-V compound semiconductors rather than silicon-based processes have been used to implement the mm-wave systems due to their high carrier mobility, high breakdown voltages, and lower passive loss. The low breakdown voltage of silicon transistors combined with poor metal conductivity make power generation at mm-wave frequencies challenging. In a standard silicon process the substrate is lossy due to its low substrate resistivity, which often is less than $10 \ \Omega \cdot \mathrm{cm}$. This is substantially smaller than that of GaAs substrates $(10^7 - 10^9 \ \Omega \cdot \mathrm{cm})$. Additionally, the high dielectric constant of silicon $(\epsilon_r \sim 11.7)$ results in the silicon substrate absorbing most of the power in unshielded structures such as inductors, coplanar transmission lines and dipole antennas rather than allowing the energy to propagate in a desired manner or to radiate into free space. In the absence of appropriate preventive measures, the combination of high dielectric constant and low resistivity substrate can dissipate most of the power as heat in the substrate and thus lowers the overall system efficiency. The combined effect of the high dielectric constant and low resistivity of the substrate also has profound effects on the on-chip antenna design as discussed in the next section.

In this paper, we present a fully integrated four-element phased-array receiver with on-chip antennas at 77 GHz implemented in a 130-nm IBM SiGe BiCMOS process. In Section II, we discuss the integration of the on-chip antennas in silicon. Section III shows the system architecture and the details of the

circuit design are presented in Section IV. Finally, we report the experimental results in Section V.

II. ANTENNA DESIGN

An antenna converts electrical power in the circuit domain to electromagnetic wave radiations in a propagation medium and *vice versa*. The radiated energy appears as loss if looked at from a pure circuit domain perspective and is thus modeled as a resistance.[2] In addition to this so-called "radiation resistance" which is essential to the antenna operation, a second resistive part is required to model the physical energy loss in the non-ideal metals and the dielectrics. For an antenna excited with a current source, loss and radiated power can be calculated as

$$P_{\text{rad}} = R_{\text{rad}} I^2 / 2$$
$$P_{\text{loss}} = R_{\text{loss}} I^2 / 2 \tag{1}$$

where P_{rad} is the radiated power, P_{loss} is the lost power, R_{rad} is the radiation resistance, R_{loss} is the loss resistance, and I is the antenna current. Obviously, high loss resistance wastes power and lowers the overall efficiency. In fact, radiation efficiency is directly related to the ratio of loss and radiation resistances. By knowing these two values, radiation efficiency can be calculated as

$$\eta_{\text{rad}} = \frac{R_{\text{rad}}}{R_{\text{rad}} + R_{\text{loss}}}. \tag{2}$$

In this section, we focus on important antenna parameters such as gain and efficiency and compare several antenna configurations suitable for silicon on-chip implementation based on these parameters.

A. Radiating From Topside Without Ground Shield

The most obvious choice for on-chip antennas is to implement them as metal lines on top of the substrate and radiate upward into the air. In this subsection, we show why this may not be an effective solution by looking at a dipole antenna placed at the boundary of semi-infinite regions of air and dielectric (Fig. 1). Although this over-simplified configuration does not correspond to the practical setting, it guides us to better understand the effects of silicon high dielectric constant on antenna radiation pattern and efficiency. For a dipole antenna seeing the vacuum (or air) on one side and a dielectric on the other side, the ratio of the power coupled into air to the total radiated power is approximated[3] by [9], [10]

$$\frac{P_{\text{air}}}{P_{\text{total}}} = \frac{1}{\varepsilon^{3/2}} \tag{3}$$

where P_{air} is the radiated power into air, P_{total} is the total radiated power and ϵ is the dielectric constant. From this formula for silicon dielectric $(\epsilon \sim 11.7)$ a very small portion of the power radiates into the air (about 3%) and the rest of it couples into silicon. This demonstrates that without any mechanism to reroute the power coupled into silicon substrate, it is not possible to implement a high efficiency antenna on-silicon this way.

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[2]Often a reactive part is also used to account for the resulting phase difference between antenna's voltage and current.
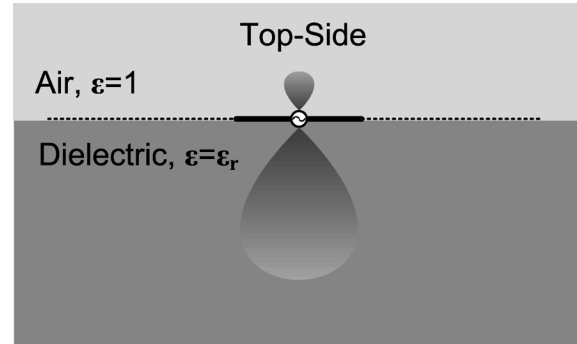
[3]Within a factor of 2.

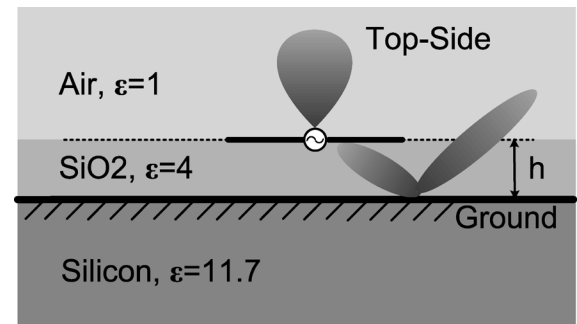Fig. 1.   Radiating from top side without ground shield.

Fig. 2.   Radiating from top side with on-chip ground shield.

B. Radiating From Topside With On-Chip Ground Shield

Another possible option is to incorporate an on-chip ground shield and trying to reflect the radiated energy upward, thus preventing it from coupling into silicon, as shown in Fig. 2. In this case, the on-chip antenna and the ground shield have to be placed inside the SiO_2 due to process limitations. For such a configuration, the distance of the antenna and the ground shield affects the antenna-ground coupling and determines the radiation resistance [18], [19]. Unfortunately, the distance between the bottom of the top metal layer and the top of the lowest metal layer rarely exceeds 15 μm in today's process technologies. This small antenna-ground spacing causes a strong coupling between the antenna and the ground layer which lowers the all-important radiation resistance. Fig. 3 shows the results of the electromagnetic simulations of a copper dipole antenna placed over a metal ground plane with a SiO_2 dielectric of thickness, h, sandwiched in between. The dipole dimensions are 4 μm $\times$ 20 μm $\times$ 1150 μm and a moment-based EM simulator, IE3D [26], is used to perform the simulations. The dipole-length is equal to a length of a resonant dipole at 77 GHz which is placed in the boundary of semi-infinite regions of air and SiO_2. Based on this simulation, for a spacing of 15 μm between the antenna and the ground layer, the radiation resistance is very small (less than 0.1 Ω) hence the total resistance is dominated by the ohmic loss of the copper resulting in a radiation efficiency of less than 5%. An option to increase the efficiency of the antenna seems to be the implementation of an off-chip ground shield to increase the distance between the antenna and its ground layer. We will discuss this case in the next subsection.
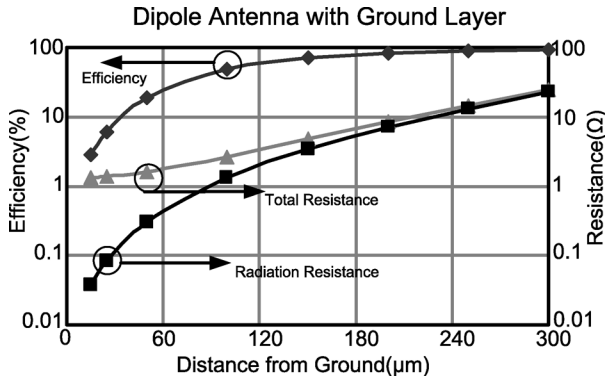
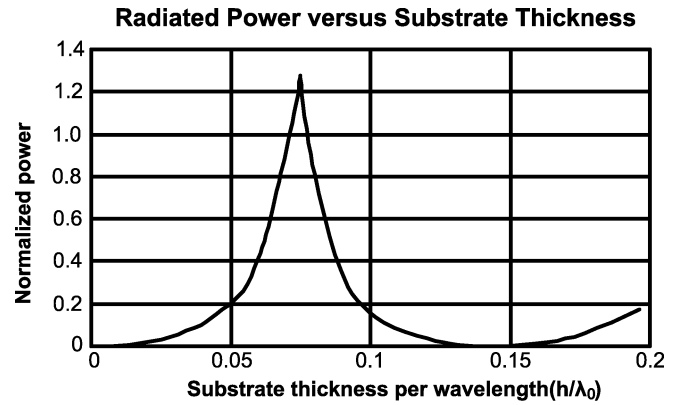Fig. 3. Dipole radiation resistance and efficiency.

Fig. 4. Radiating from top side with off-chip ground shield.

Fig. 5. Normalized radiated power for a grounded dipole [9].
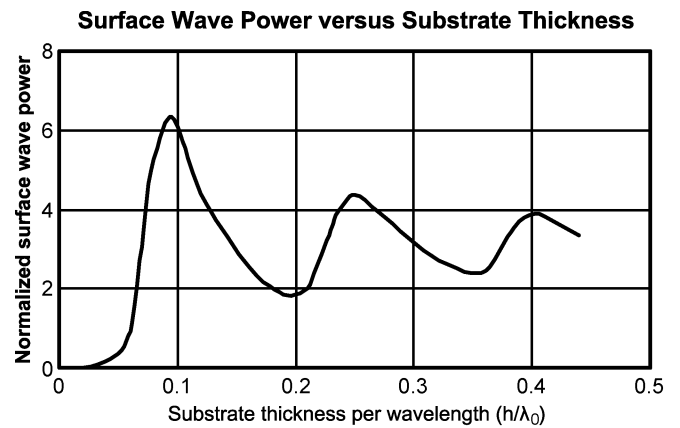
Fig. 6. Surface wave power for a grounded dipole [9].

Fig. 7. Radiating from planar back-side.

C. Radiating From Topside With Off-Chip Ground Shield

As shown in Fig. 4, an off-chip ground shield can be placed underneath the silicon substrate. In this case, the silicon substrate thickness is much larger than the SiO_2 layer and effectively we are dealing with a high dielectric constant substrate ($\epsilon = 11.7$). Unfortunately, because of the high dielectric constant of silicon and the large substrate thickness (100 μm or more), most of the power gets absorbed into surface-wave power [9]–[11]. If we assume the thickness of SiO_2 is negligible compared to that of silicon, then the surface-wave power can be numerically calculated. Based on these results, normalized radiated power and surface-wave power are plotted in Fig. 5 and Fig. 6, respectively. These quantities are normalized to the dipole's free space radiated power given by [9]

$$P_0 = \omega^2 \mu_0^{3/2} \varepsilon_0^{1/2} I^2 d^2 / 12\pi \qquad (4)$$

where I is the current, ω is the angular frequency, and d is the effective length of the dipole. As is shown in Fig. 5, at 77 GHz the maximum radiated power, which is around $1.3P_0$, occurs at the silicon substrate thickness of 290 μm ($h = 0.075\lambda_0$). However, at this substrate thickness, the power in all the surface wave modes is more than $3.5P_0$ (Fig. 6), which indicates that even in the case of lossless silicon substrate, the power wasted in the surface wave modes is 2.7 times greater than the useful radiated power. It is important to realize that for a lossy and finite-dimensional substrate, the surface-wave power is either dissipated due to the substrate conductivity or radiated from the edge of the chip and that often results in an undesirable radiation pattern.
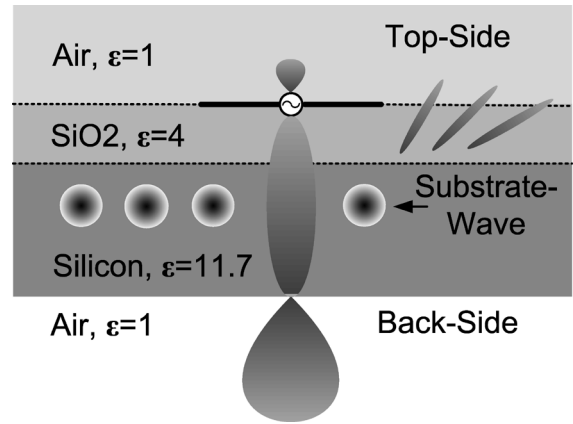
D. Radiating From the Planar Backside

Following the prior discussion, we attempt to determine what happens if we remove any ground shield and radiate from the backside of the chip (see Fig. 7). In this case, based on numerical calculations [9], [11], the normalized radiated and surface-wave powers are plotted in Fig. 8 and Fig. 9, respectively. At 77 GHz, the total radiated power, the sum of the power radiated from the air side and the substrate side, peaks at the silicon substrate thickness of 580 μm ($h = 0.15\lambda_0$) and approaches P_0. At this substrate thickness, the total surface-wave power is
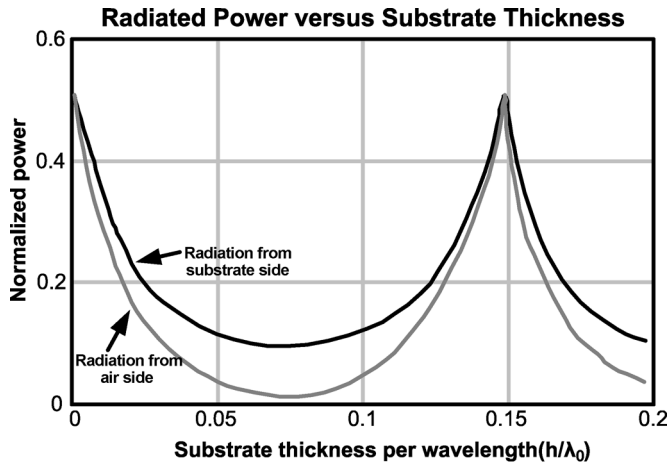
Radiated Power versus Substrate Thickness

Fig. 8.   Normalized radiated power for an ungrounded dipole [9].

Surface Wave Power versus Substrate Thickness
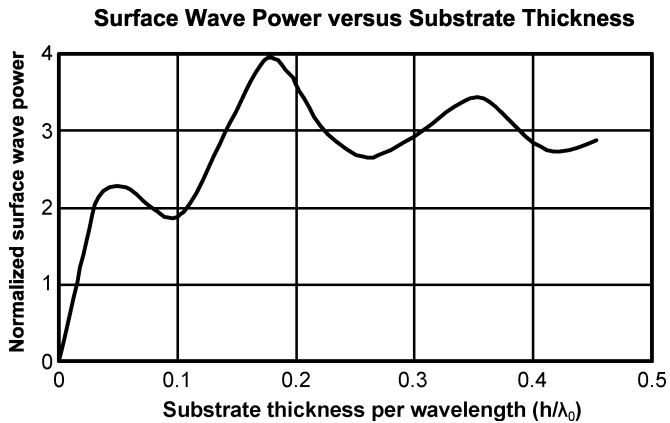

Fig. 9.   Surface wave power for an ungrounded dipole [9].

around $3.4P_0$, which is 3.4 times greater than the power radiated from the air side and the substrate side combined.

E. Radiating From the Back-Side Using a Dielectric Lens

Fortunately, the amount of the total power absorbed into surface-waves depends on the geometry of the substrate. A hemispherical silicon lens with a matching layer can convert the surface-wave power to a useful radiated power [9]–[15]. This configuration is illustrated in Fig. 10. A quarter wave-length matching layer can be used to match the silicon impedance ($Z_{si} = 110 \ \Omega$) to air impedance ($Z_{air} = 377 \ \Omega$) [16]. In our design, we have used the silicon lens without the matching layer due to the fabrication limitations. In this design, antennas are fabricated by using bottom metal layers to minimize the distance to the substrate. A parallel combination of three bottom metal layers maintains high antenna metal conductivity. To further reduce the substrate loss, the silicon chip is thinned down to 100 μm. This minimizes the path length through which the radiated wave travels inside the lossy doped substrate. Due to layout limitations in our design, the antennas are placed at the edge of the chip and a slab of undoped silicon is abutted to the substrate to maintain a uniform dielectric constant substrate underneath the antenna (Fig. 11). For mechanical stability, a 500-μm-thick undoped silicon wafer is placed underneath the chip and the silicon lens is mounted on the backside seen in
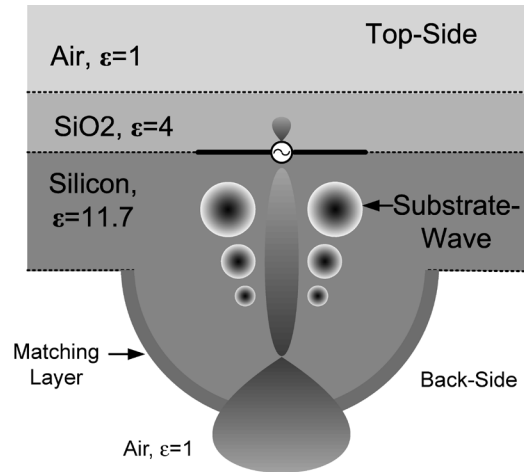

Fig. 10.   Radiating from back side using a silicon lens.

Fig. 11. All of the low-frequency connections are brought to the chip by board metal traces and wire-bond connections. As this setup is highly compatible with flip-chip technology, all of these low-frequency signals can be carried by flip-chip connections as well.

III. SYSTEM ARCHITECTURE

In this section, we describe the block diagram of the 77-GHz four-element phased-array receiver which is part of a complete 77-GHz four-element transceiver. The transmitter and local oscillator (LO) generation circuits are presented in [21] and [23].

Fig. 12 shows the architecture of the receiver chip, which adopts a two-step downconversion scheme with an RF frequency of 76–81 GHz and an IF in the 25–27 GHz. This frequency plan enables us to generate the first and second LO signals with a single frequency synthesizer. It is also noteworthy that the IF is located in the 22–29 GHz radar band, hence a dual-mode radar chip can be potentially developed by bypassing the RF front-end. Each receiver front-end consists of an on-chip dipole antenna, a low-noise amplifier (LNA), an RF mixer, and a dual-mode IF amplifier. The gain of the IF amplifier can be varied by 15 dB using a single digital control bit. The four-path IF signals are combined using a symmetric active combining amplifier, which will be discussed in Section IV. The combined signal is further downconverted to baseband using quadrature paths.

A differential voltage-controlled oscillator (VCO) generates the first LO signals at 52 GHz, which are symmetrically distributed to each RF mixer using differential transmission lines (t-lines). A network of LO buffers is used for LO signal distribution to compensate for the t-line loss and to ensure hard switching of the mixers. The continuous analog phase shifting is performed locally at each RF mixer by an analog phase rotator, which realizes continuous beam steering while accurately compensating for the phase and amplitude deviations. The quadrature second LO is obtained by dividing the first LO frequency by 2 [21], [23]. A frequency divider chain is used to further divide the second LO frequency down to 50 MHz to be locked to an external reference frequency.

At mm-wave frequencies, t-lines are a better choice than inductors for matching purposes. At these frequencies, the required reactance for matching circuits is small. These matching
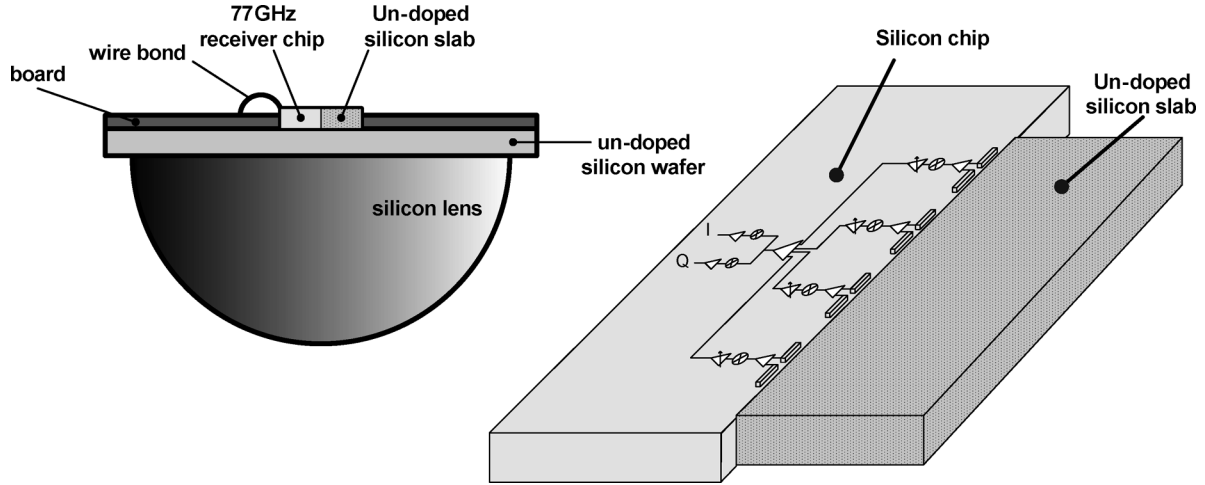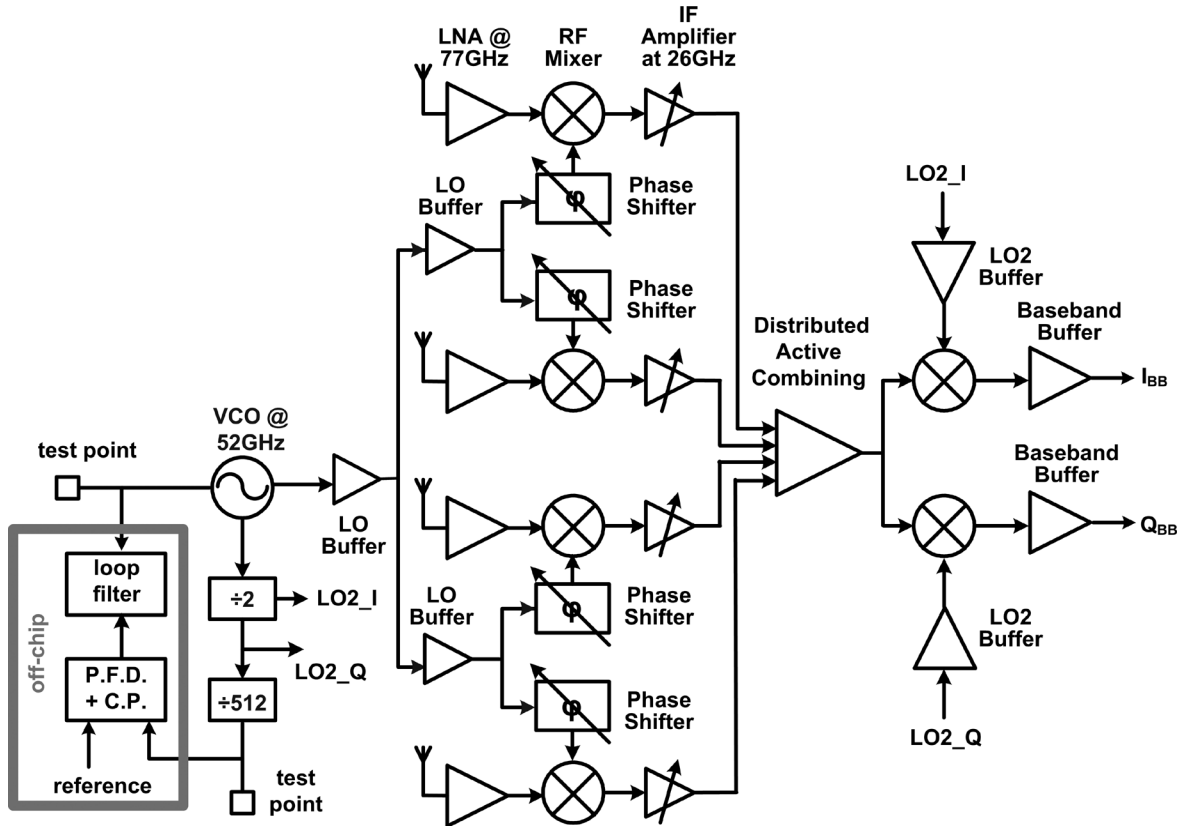
Fig. 11. Board setup configuration.

Fig. 12. System architecture.

circuits can be implemented by using shielded transmission lines. Other advantages of these shielded transmission lines are accurate modeling, well-defined return path, high isolation, and reduced coupling to the adjacent circuits [8].

IV. CIRCUIT DESCRIPTION

A. 77-GHz LNA With an On-Chip Balun

The two-stage differential cascode LNA driven by a differential dipole antenna uses shunt and series t-lines for impedance matching [Fig. 13(a)]. The differential input impedance of the LNA and its differential output impedance are designed to be 50 Ω and 100 Ω, respectively, at 77 GHz. In order to characterize LNA performance independently, a single-ended-to-differential converter, a balun, following a $\lambda/4$ t-line is placed at the front of the stand-alone LNA test structure, as shown in Fig. 13(b). This combined structure converts the differential 50 Ω input impedance of the LNA to single-ended 50-Ω impedance which can be easily driven by a single-ended 50-Ω waveguide probe.

B. 77-to-26-GHz RF Mixer

A double-balanced current-commuting mixer is employed to downconvert the 77-GHz RF signal to a 25.5-GHz IF, as illustrated in Fig. 14 [27]. AC-coupling capacitors are placed at the
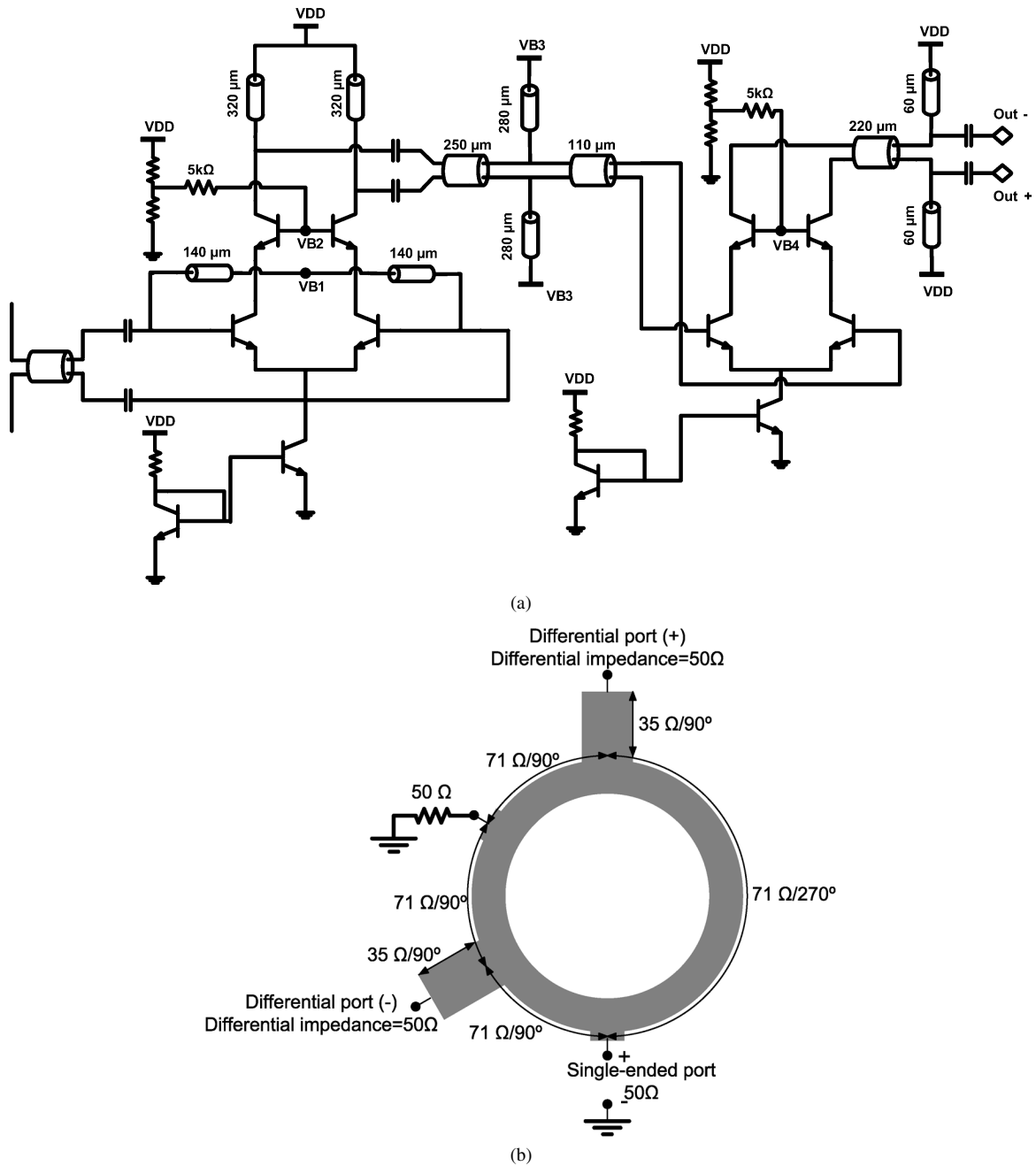
Fig. 13.   (a) 77-GHz LNA schematic. (b) Schematic of balun.

RF ports. The RF and LO ports of the mixer are all matched to a differential impedance of 100 Ω, using t-line stub tuning [22].

The bandwidth of this mixer is primarily determined by the quality factor Q of the resonant load at 26 GHz. The 3-dB bandwidth (BW) of the load impedance is related to Q as

$$\text{BW} = \frac{\omega_o}{Q} \tag{5}$$

where ω_o is the resonant frequency. The load impedance of a parallel LC at resonance is given by [22, p. 307]

$$Z_L \approx \omega_o L Q. \tag{6}$$

Therefore, the choice of Q is a trade-off between bandwidth and gain. To achieve the desired bandwidth, a Q of 3.5 is the maximum, according to which we choose 0.4-nH inductance and 250-Ω de-Q resistance to form the load with the capacitance of the transistor parasitic and input impedance of the subsequent stage.

Simulation results indicate the RF mixer achieves 5-dB voltage conversion gain, a 10-GHz bandwidth, and an 11-dB noise figure. They also show an input return loss of 20 dB at the RF port and 11 dB at the LO port. To save chip area, resistive emitter degeneration instead of inductive degeneration is used to enhance the linearity. The common node of the degeneration resistors is connected to the ground instead of a tail current source for better linearity.
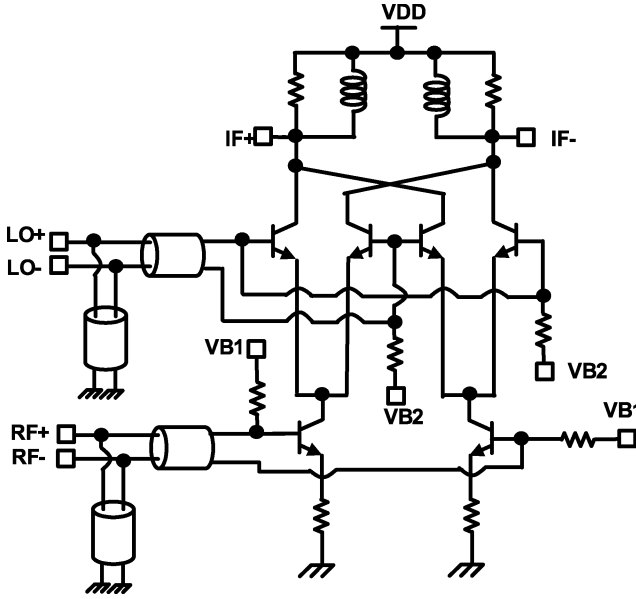
Fig. 14. 77-GHz RF mixer.

Fig. 15. 26-GHz two-gain mode amplifier.

C. 26-GHz Two-Mode Amplifier

A differential resistively degenerated cascode is used as the 26-GHz amplifier, as shown in Fig. 15. A differential current-bleeding branch consisting of Q_2 and Q_3 is added. The DC bias voltage at the base of Q_2 and Q_3 can be toggled between two values by digital switches, corresponding to a high-gain and a low-gain mode of the amplifier. In high-gain mode, Q_2 and Q_3 are off. In low-gain mode, the gain normalized to its high gain value is approximately given by

$$\frac{A_{v,\text{low}}}{A_{v,\text{high}}} = \left(1 + \frac{A_2}{A_4}\exp\left(\frac{V_{b,\text{low}} - V_{\text{dd}}}{V_T}\right)\right)^{-1} \quad (7)$$

where A_2 and A_4 are the emitter area of Q_2 and Q_4, respectively, and $V_{b,\text{low}}$ is the base voltage of Q_2 and Q_4 in the low-gain mode. In this design, V_{B,Q_2} at low-gain mode is set to V_{dd}, and A_2/A_4 is fixed at 11/3. Equation (7) predicts 13.5-dB gain variation between the two modes. The simulation result shows 15-dB gain variation.

D. A 26-GHz Signal Combining Amplifier

The four-path 26-GHz signals are combined through a distributed active combining amplifier, as shown in Fig. 16 [27]. Emitter resistive degeneration is implemented at the input transconductors to improve the linearity and accordingly the dynamic range of the system. The current outputs of the transconductors are routed to the combining node via a symmetric two-stage binary structure. A pair of cascode transistors is inserted at each combining junction to isolate the input and output ports, thereby improving the overall stability of the amplifier. The total length of each routing transmission line, T1, is 340 μm and that of T2 is roughly 2.55 mm. Both T1 and T2 use a differential t-line structure with ground and side metal shields to minimize the substrate loss and cross coupling. Matched transmission line terminations are obtained by choosing the appropriate bias current so that the conductance g_m of the cascode transistors is matched to the real t-line conductance.
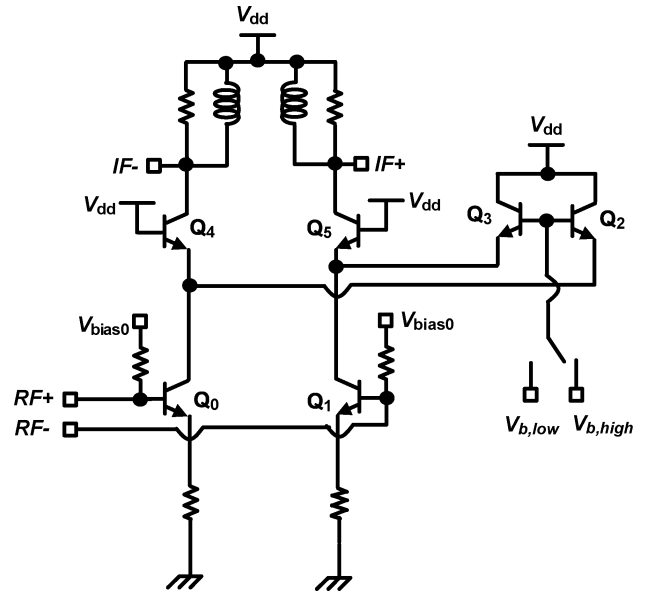
For the operating frequency of ω_0, the imaginary part of the emitter-base admittance, $j\omega_0 c_\pi$, is much smaller than g_m if the transistor transition frequency ω_T is much higher than ω_0. Therefore, a matched termination can be achieved even without additional passive tuning. In this work, we dedicated 1-mA DC bias current to each branch. T_1 is designed to exhibit 64-Ω odd-mode impedance, while T_2 has an odd impedance of 32 Ω. Simulations show that the return loss is better than 10 dB at the terminations of the transmission lines at both levels. The differential output of the amplifier is loaded with an *LC* tank with parallel resistors to improve the bandwidth.

E. 26-GHz Quadrature Mixer

A pair of double-balanced mixers driven by quadrature LO signals are used to perform frequency translation from 26 GHz to baseband, one of which is shown in Fig. 17. The 26-GHz signals are coupled into the mixer transconductance stage through 0.9-pF MIM capacitors. The input differential pair is degenerated with 30-Ω resistors at the emitter to improve linearity.

The LO port of the mixer is fed by a 26-GHz buffer which is used to compensate the LO signal loss through the distribution network, ensuring the differential LO amplitude applied to the mixer is larger than 200 mV so that the mixer gain is saturated. The input matching of the LO buffer is provided by a 100-Ω resistor directly connected between the differential inputs. Although matching network composed of inductors and capacitors can provide additional voltage gain, this solution is prohibited by the limited silicon area. The LO buffer is loaded with 0.6-nH spiral inductors and 320 Ω de-Q resistors, providing a gain of 15 dB. With 280-Ω load resistor, the second mixer achieves 6-dB conversion gain and 8-GHz IF-referred bandwidth. The mixer core consumes 4-mA DC current and the LO buffer drains 1 mA.

V. Experimental Results

The 77-GHz phased array is fabricated in a 0.13-μm SiGe BiCMOS process with a f_T of 200 GHz for SiGe HBT devices.
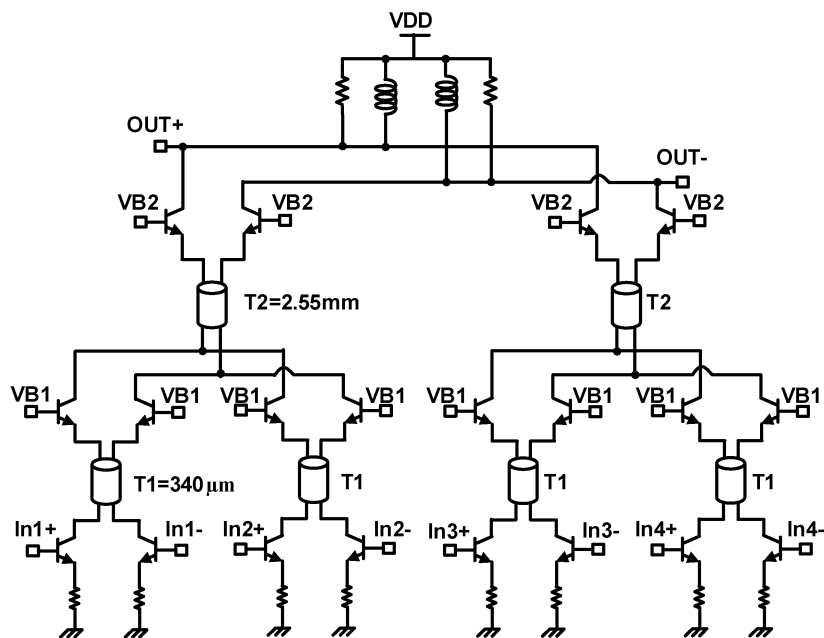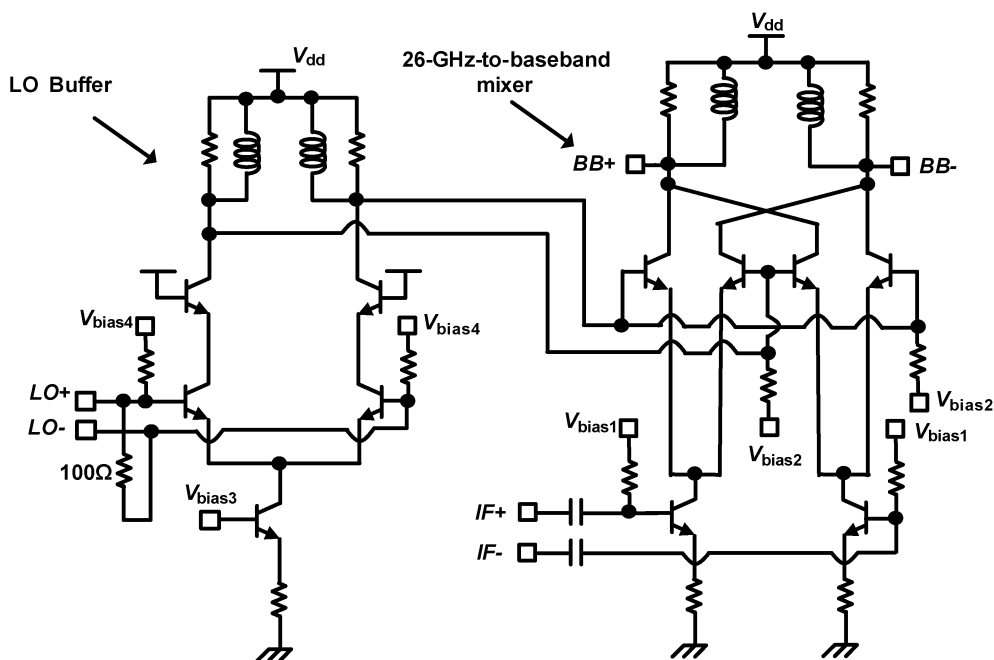
Fig. 16. 26-GHz combining amplifier.

Fig. 17. 26-GHz-to-baseband mixer and 26-GHz LO buffer.

The receiver section occupies roughly 9 mm^2 of the 6.8 mm × 3.8 mm total chip. Fig. 18 shows the die micrograph.

To accurately characterize the receiver performance, a stand-alone LNA with integrated balun is measured. One of the important parameters necessary for accurate de-embedding of the stand-alone LNA measurements is the loss of the balun and the following $\lambda/4$ t-line. Two identical baluns including the matching transmission lines are designed and connected together at their differential nodes, as shown in Fig. 19. The loss of the two series identical structures is expected to be twice that of a single one. The measured balun loss and the LNA performance versus frequency are shown in Fig. 20 and

Fig. 21, respectively. Stand-alone LNA peak gain of 23.8 dB is measured at 77 GHz with a 3-dB bandwidth of more than 6 GHz, while the lowest noise figure of 5.7 dB is measured at 75.7 GHz. The LNA consumes 17.5 mA from a 3.5-V supply.

Fig. 22 illustrates the test setup for measuring the receiver gain. The input signal at 77-GHz range is provided by a frequency quadrupler capable of delivering output frequency from 60–90 GHz. The input of the frequency quadrupler is supplied by signal generator working up to 26.5 GHz. The power of the input signal can be adjusted by a variable linear attenuator. A WR-12 planar wafer probe is used to feed the single-ended signal to LNA input. The external connections between W-band
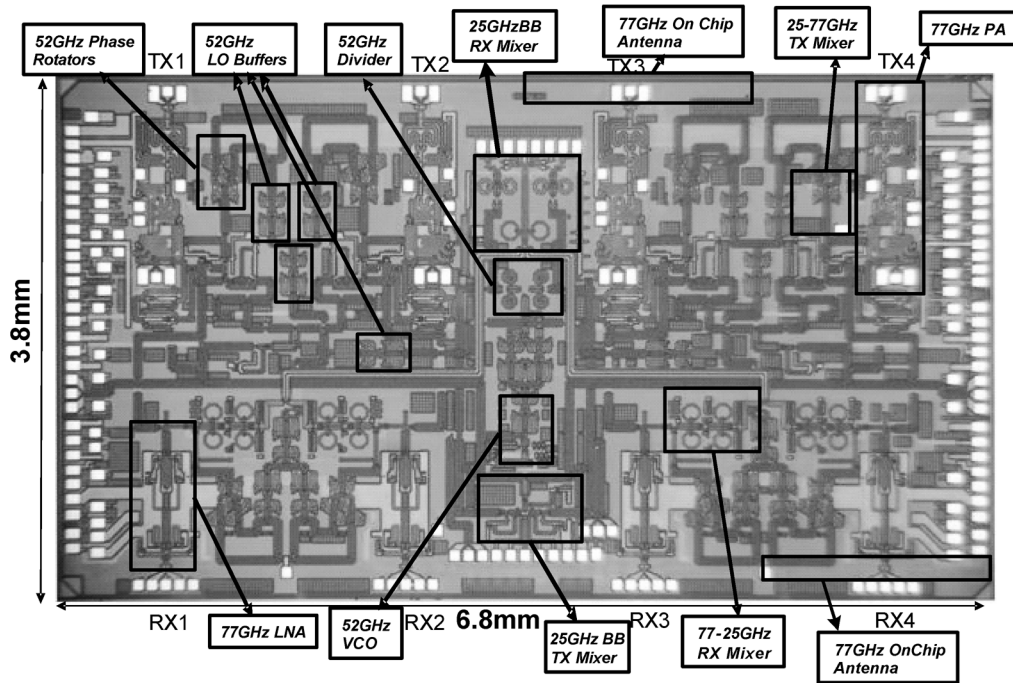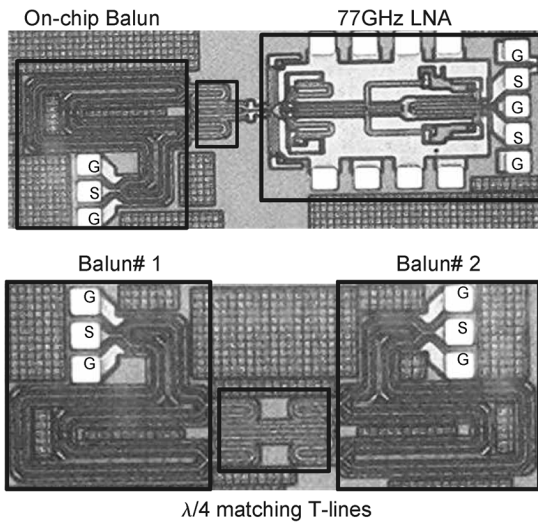
Fig. 18. Chip micrograph.

Fig. 19. 77-GHz LNA with on-chip balun.

Fig. 20. Measured on-chip balun loss.

Fig. 21. LNA gain and noise figure.

components are built using WR-12 waveguides. The microwave input power is calibrated up to the probe tip using an Agilent E4418B power meter with W-band power sensor. An exclusive OR (XOR) logic gate acting as a phase detector and a first-order *RC* low-pass filter complete the PLL which locks the phase and frequency of the 52-GHz VCO to a 50-MHz reference provided by a signal generator. The baseband outputs are characterized using Agilent 4448A spectrum analyzer. The same setup is also used for receiver noise figure measurement, except the RF inputs are replaced with a W-band noise source.

The electrical performance of the receiver is characterized after laser trimming the antennas. A 37-dB single-path receiver gain (Fig. 23) is measured at 79.8 GHz with a 2-GHz bandw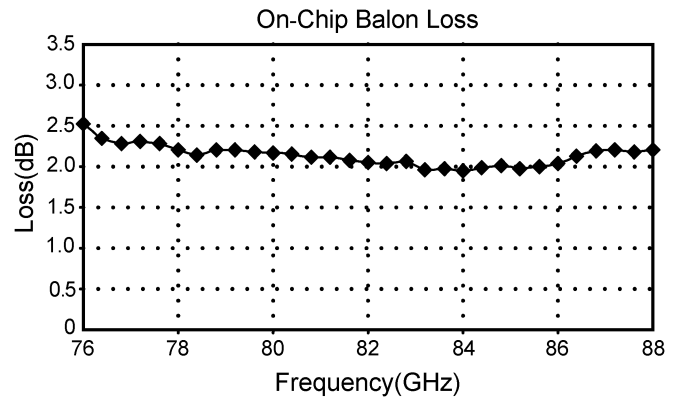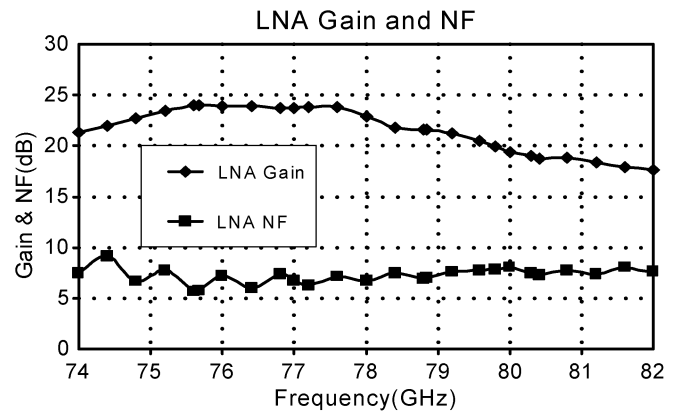idth, corresponding to an inferred array gain of 49 dB. The minimum receiver noise figure is measured to be 8 dB (at 78.8 GHz).

The radiation performance of the complete receiver is measured using the setup shown in Fig. 11 where a printed circuit
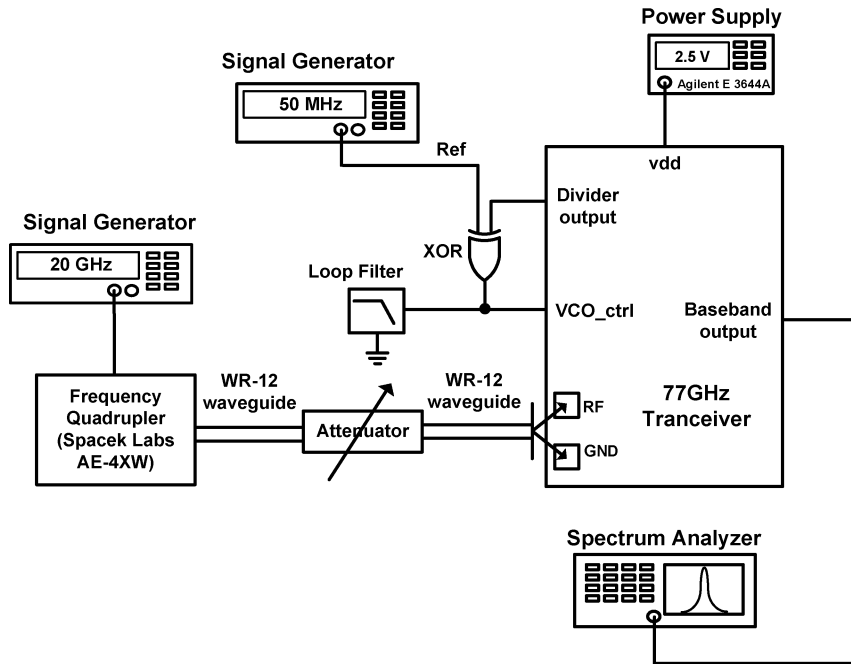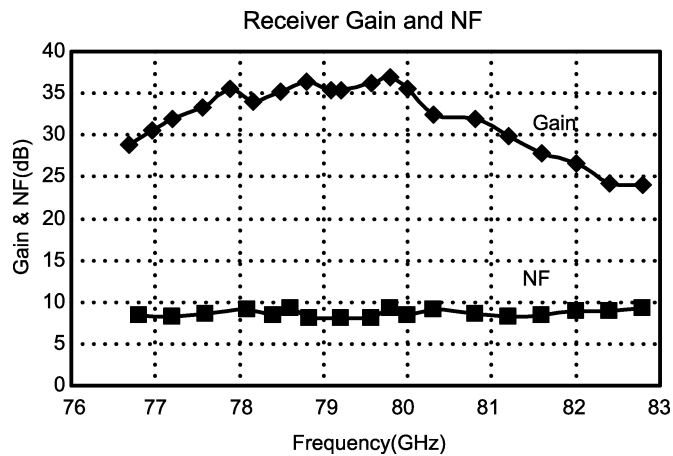
Fig. 22.   Receiver test setup.

Fig. 23.   Single path receiver gain and noise figure.

TABLE I
MEASUREMENT SUMMARY

Receiver Conversion Gain	+37dB (per element)
Inferred Array Gain	+49dB
Receiver 3dB-bandwidth	2GHz
Receiver Minimum NF	8dB (per element)
LNA Gain	+23dB
LNA 3dB-bandwidth	6GHz
LNA Minimum NF	5.7dB
LNA output referred 1dB	-5.5dBm
Antenna Gain	+2dBi
Current consumption:	
Each LNA (@3.5V)	17.5mA
Each down-conversion path (@2.5V)	40mA
Entire 4-path receiver with frequency synthesizer (@2.5V)	420mA

board (PCB) provides the supply as well as low-frequency and digital control signals to the chip and takes the baseband signal out using wirebond connections. A W-band standard horn antenna irradiates the receiver (Fig. 24). The peak measured antenna gain is +2 dBi. Based on the simulations, this gain can be further improved by 4 to 5 dB using a smaller lens with a quarter-wavelength matching layer. Fig. 25 shows the measured deembedded E-plane single-element dipole radiation pattern with and without the lens. Based on this measurement, the lens improves the gain by more than 10 dB.

The measurement results are summarized in Table I.

VI. CONCLUSION

The reported phased-array receiver, combined with the phased-array transmitter in [21] and [23], forms the first fully integrated silicon based phased-array transceiver with on-chip

antennas at 77 GHz. In the receiver, a two-step down-conversion scheme is used with a single VCO. The signal combining is performed using a novel distributed active combining amplifier at IF. In the LO path, a cross-coupled quadrature injection locked frequency divider (QILFD) divides the 52-GHz VCO frequency by a factor of 2 and is followed by a divide-by-512 divider chain. Conversion gain of more than 37 dB, 2 GHz BW, and 8 dB noise figure are achieved. The antenna gain of +2 dBi is achieved in the silicon substrate. We have shown that the lens improves the gain by more than 10 dB.
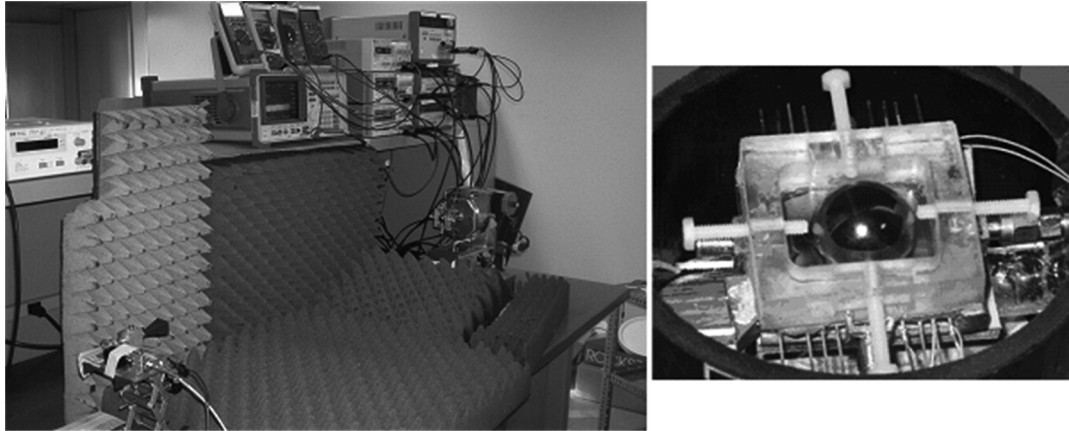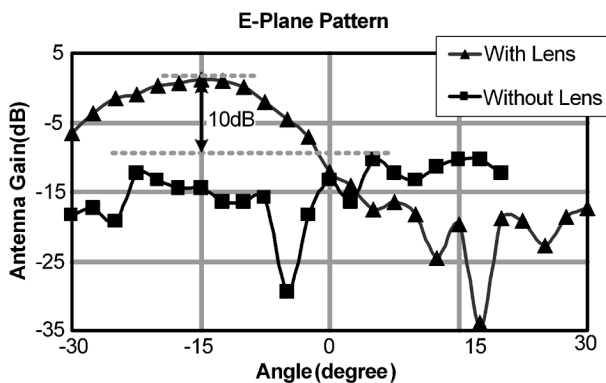
Fig. 24. Antenna measurement setup.

Fig. 25. E-plane antenna gain.

E. Keehr, A. Hassibi, and P. Focardi. The technical support for CAD tools from Agilent Technologies, Zeland Software Inc., Ansoft Corp., and Integrated Engineering Software is also appreciated.

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