An Active Cancellation Architecture for High-speed Track-and-Hold Amplifiers in 45nm CMOS SOI

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***Abstract*—This paper presents a 40GS/s track-and-hold amplifier with active cancellation. An active cancellation circuitry was implemented to mitigate the leakage caused by the parasitic capacitance of the sampling transistor. The cancellation technique increases the isolation between the track and hold modes, especially at high input frequencies. An SFDR3 of 62dB was measured for 5GHz input signal sampled at 40GS/s. A droop voltage of 20μv/ns was recorded. The chip was fabricated in IBM 45nm CMOS SOI technology node.**

***Index Terms*—Track-and-Hold, active cancellation, isolation, amplifier, ADC, SFDR, silicon, CMOS**

I. Introduction

During the past decade, there has been a significant interest in high-speed wireless communication systems and high-resolution 3D imaging radars [1]–[3]. These applications require a high-speed ADC operating with a wide analog bandwidth and a sampling rate exceeding tens of gigahertz [4], [5]. However, one of the limiting factors that prevents the performance of the ADC is the parasitic leakage of the sampling circuitry. The parasitic capacitance of the sampling transistor provides an alternate path for the signal and clock to leak to the holding capacitor. Recently, there have been some attempts to mitigate the effects of the clock leakage by building cancellation circuits to minimize the parasitic discharge of the clock on the holding capacitor [6], [7]. Most of the prior work focused on minimizing the clock leakage because the sharp rise/fall transitions in the clock waveform caused a large discharge on the holding capacitor. Although the clock leakage is important but it is systematic and predictable, and hence it can be calibrated. The is because the waveform of the clock signal is known. Unfortunately, the waveform of the input signal is unknown before sampling and its parasitic coupling depends on the shape of the input signal. For instance, if the input waveform is rapidly changing and contains high frequency components, the parasitic coupling from the input to the output of the sampling circuit becomes significant. This adds a large undesired discharge on the holding capacitor and reduces the Effective Number of Bits (ENOB).

In this paper, we introduce a novel active cancellation architecture to mitigate the undesired parasitic coupling of the input signal to the positive node of the holding capacitor. This mitigation increases the isolation between the input and sampling nodes, thus increasing the performance of the ADC at higher input frequencies.

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II. Circuit Design

A. Track and Hold Amplifier

In a sample-and-hold or a track-and-hold architecture, the sampling transistor is the key to building an ADC with a good figure of merit. The size of the sampling transistor and the holding capacitor becomes critical when the frequency of the input signal exceeds several GHz. In particular, in a track-and-hold architecture, the 3dB roll-off of the $R_{ON}C$, where R_{ON} is the resistance of the switch in the track mode and C is the effective capacitance of the holding capacitor, should be greater than the frequency of the input signal. To reduce $R_{ON}C$, the size of the sampling capacitor should be reduced. However, the size of the sampling capacitor cannot be made too small, as it increases the voltage noise on the sampled signal. Moreover, reducing the size also makes designing the subsequent buffer stage challenging, as the droop in the sampled voltage becomes the limiting factor in the performance of the ADC. Another way to reduce $R_{ON}C$ is to reduce R_{ON} by making the sampling transistor larger. However, increasing the size of the sampling transistor reduces the isolation at higher input frequencies. This is because a large sampling transistor has large parasitic capacitance. In particular, the effective parasitic capacitance between source and drain of the transistor caused by C_{SG} and C_{GD} significantly reduces the isolation in the hold mode, which leads to a reduction in ENOB. To resolve this issue, an active cancellation method is

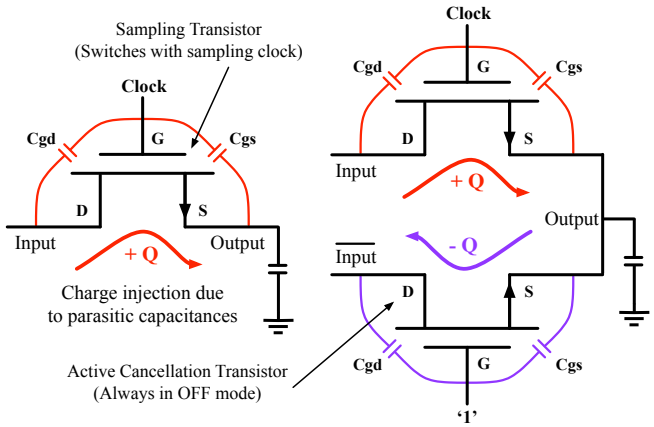

Fig. 1. (Left) Figure shows a conventional sampling switch. Parasitic capacitances C_{SG} and C_{GD} provide an alternate path for the input signal to couple to the sampling capacitor. (Right) Shows a sampling switch with active cancellation. A dummy transistor, which is always off, is added in parallel to the sampling transistor. The parasitic charge dumped by sampling switch is removed by the cancelling transistor.

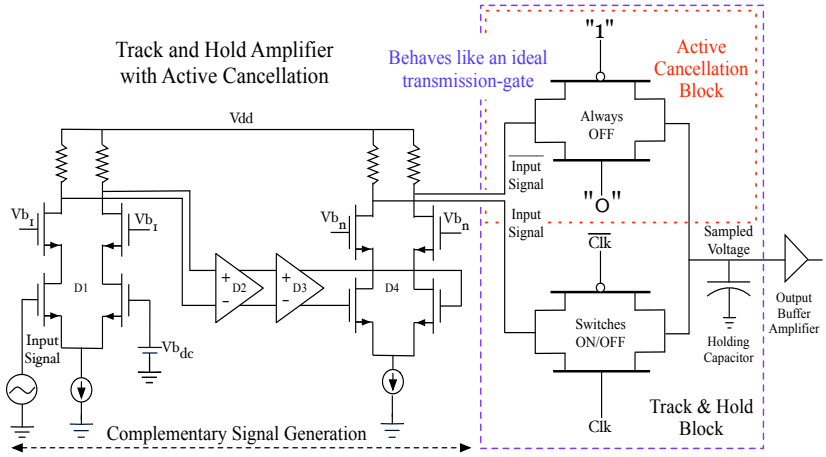

Fig. 2. Architecture for Track and Hold Amplifier with Active Cancellation

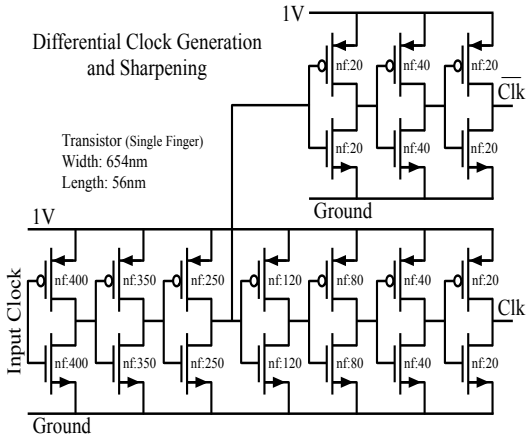

Fig. 3. Differential clock generation and sharpening circuit

proposed that increases the isolation despite the large size of the sampling transistor, making it useful in applications where the frequency of the input signal is high. Figure 1 shows the working principle of the active cancellation circuitry.

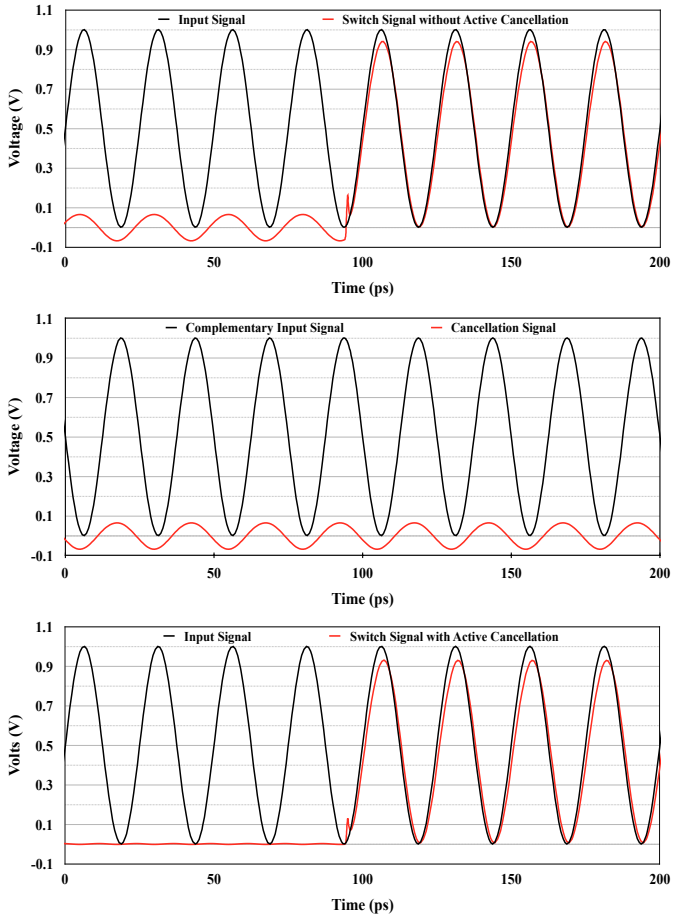

Fig. 4. Transient simulation showing the effects of active cancellation. (Top figure shows the transient output in track and hold modes at the holding capacitor when the active cancellation block is not in use. The middle figure shows the output of the active cancellation block without the sampling block. The bottom figure shows the output when the active cancellation block is used.)

B. Active Cancellation

An active cancellation method is proposed to increase the isolation between the track and hold modes. During the track mode, the transistor is switched ON, and the voltage of the holding capacitor follows the input signal. During the hold mode, the transistor is switched OFF. Ideally, there should be an infinite isolation between the input signal and the holding capacitor. However, due to the parasitic capacitance between source and drain, an alternate path is formed between the source and drain of the sampling transistor. This parasitic capacitance injects charge during the hold mode to the holding capacitor and corrupts its held value.

To mitigate the undesired charge injection, an additional cancellation circuitry is added in parallel to the sampling transistor, as shown in Fig. 1. The additional transistor (cancelling transistor) is always in the OFF mode and is fed with a negative copy of the input signal. During the hold mode, both transistors are in the OFF mode and inject charge to the holding capacitor. Since both transistors (the sampling transistor and the cancelling transistor) are equal in size, the charges injected by two transistors cancel each other. This charge cancellation process mitigates the effects of charge leakage due to parasitic capacitance and makes the sampling transistor behave like an ideal sampling switch. The complete architecture of track and hold amplifier with active cancellation is shown in Fig. 2.

The working principle of active cancellation can be further understood from Fig. 4. Fig. 4 (top) shows the voltage across the sampling switch during the track and hold modes. During the hold mode, there is a considerable amount of leakage through the switch that causes a large discharge on the holding capacitor. Furthermore, since the leakage is signal dependent, it is not possible to remove this error in the digital domain with post-processing. To resolve this issue, a cancelling transistor is used. Fig. 4 (middle) shows the voltage on the input and output nodes of the cancelling transistor. Since the input of the cancelling transistor is fed with a negative copy of the input signal, its leakage on the holding capacitor becomes negative of the leakage of the sampling transistor. Fig. 4 (bottom) shows the voltage across the holding capacitor when

both the sampling and cancellation blocks are active. As shown in this figure, the amount of the leakage signal is significantly reduced. In addition, during the track mode, the additional transistor acts as a high impedance path and does not change the tracking characteristics. Thus, the combined system behaves like an ideal transmission gate.

The amount of the cancellation depends on two parameters, one being the phase imbalance and other the gain imbalance between the input signal and its negative copy. Equation (1) shows the dependency of the cancellation to the phase imbalance, ϕ. This is shown in Fig. 5 (top) with a logarithmic scale. Equation (2) shows the dependency of the cancellation to the gain imbalance. This is shown in Fig. 5 (bottom) with a logarithmic scale.

Phase Imbalance

$$\begin{aligned}\text{Input RF signal} &= A\sin(\omega t)\\ \text{Cancellation Signal} &= A\sin(\omega t+\phi)\\ \text{Residual signal} &= A\sin(\omega t+\phi)-A\sin(\omega t)\\ &= 2A\sin(\frac{\phi}{2})\sin(\omega t+\frac{\phi}{2})\\ \text{Cancellation(dB) } \{f(\phi)\} &= 20\log_{10}(2\sin(\frac{\phi}{2}))\\ &= 20\log_{10}(\phi) \quad \forall \quad (\phi^3 \ll \phi) \quad (1)\end{aligned}$$

Gain Imbalance

$$\begin{aligned}\text{Input RF signal} &= A\sin(\omega t)\\ \text{Cancellation Signal} &= 10^{\frac{G}{20}}A\sin(\omega t)\\ \text{Residual signal} &= (1-10^{\frac{G}{20}})A\sin(\omega t)\end{aligned}$$

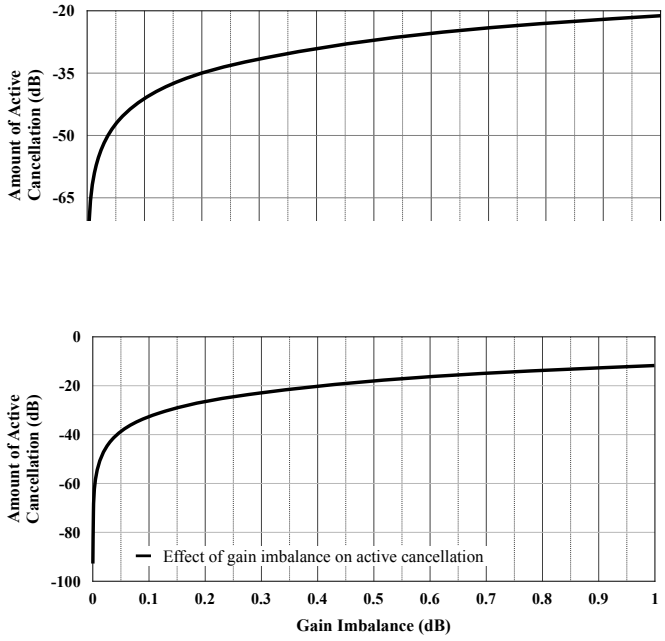

Fig. 5. (Top) Amount of cancellation as a function of phase imbalance (Bottom) Amount of cancellation as a function of gain imbalance

C. Complementary Signal and Clock Generation

In order to implement the active cancellation architecture, a cancellation signal and a signal complementary to the input signal (negative copy), have to be generated. To achieve a good level of cancellation, the gain and phase imbalances between the two signals have to be minimal over a large range of input frequencies. The generation of this complementary signal is explained next.

1) Complementary Signal Generation: In a single-ended architecture, the two complementary signals are generated by passing the input signal to a differential amplifier as shown in Fig. 2. The output of the differential amplifier consists of complementary signals with a large phase and amplitude imbalance. In order to minimize this imbalance over a wide frequency range, the complementary signals are passed through a signal conditioning block.

The signal conditioning block consists of multiple broadband differential amplifiers stacked in series. Fig. 6 shows the schematic of one of the broadband differential amplifiers. A voltage follower is added after each differential amplifier to decouple the loading of the subsequent stage and act as a voltage level converter. After passing through each stage of the differential amplifier, the gain and phase imbalances become smaller because of the high common mode rejection ratio of each differential stage. As shows in Fig. 7, the purple curve shows the voltage and phase imbalance after the first stage, the red curve shows the imbalance after the second stage, and the black curve shows the imbalance after the third stage.

Fig. 8 shows the gain and frequency response of the signal conditioning block. The purple curve shows the AC response after the first stage of signal conditioning, the red curve shows the AC response after the second stage, and the black curve shows the AC response after the third stage.

2) Complementary Clock Generation: Traditionally, the switching clock is bootstrapped [8], [9] to keep the sampling transistor linear over the input voltage swing, however, a bootstrap circuit is not very effective in high sampling frequencies.

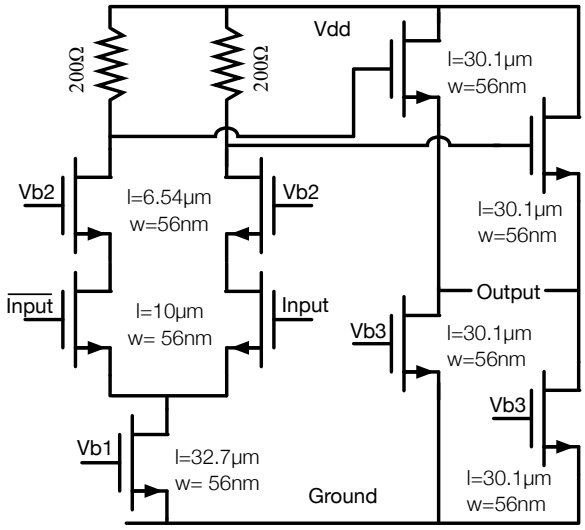

Fig. 6. Circuit schematic of a single signal conditioning block

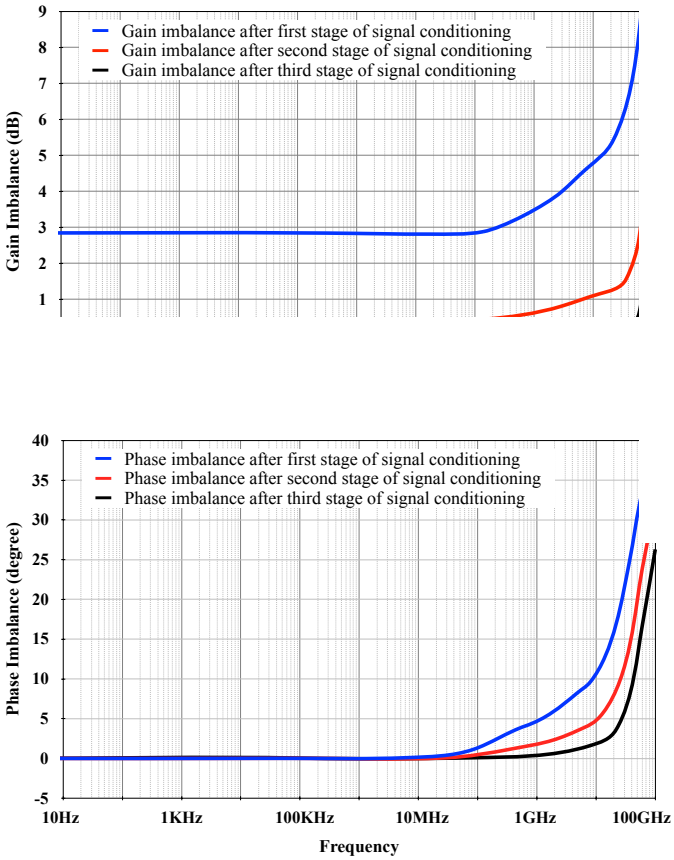

Fig. 7. Phase and gain imbalance of the complementary signal generated on chip from a single-ended RF input signal

Therefore, in this implementation, to keep the sampling transistor linear over a wide input swing, a combination of p-MOS and n-MOS are used as the transmission gate in switching. Another advantage of using p-MOS/n-MOS transmission gate is the inherent ability to mitigate clock leakage. The primary clock leakage comes from the gate-source capacitance (C_{GS}) of the p-MOS/n-MOS. Each transistor injects a charge to the

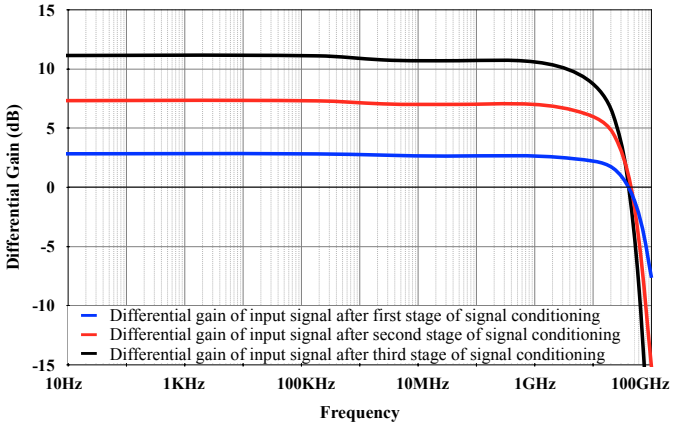

Fig. 8. Differential gain of the input RF signal after complementary signal generation and signal conditioning blocks

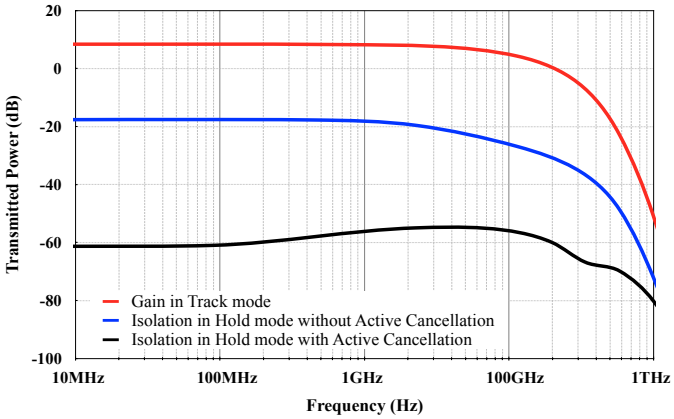

Fig. 9. The simulated isolation between the track and hold modes, with and without the active cancellation block

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is also complementary; thus mitigating the clock leakage.

To operate this transmission gate, a complementary non-overlapping clock is needed that is generated on-chip from a single-ended external clock. In this design, the single-ended external clock is passed through a multiple stages of NOT gates, as shown in Fig. 3. The NOT gates not only act as a buffer but also sharpen the edge of the clock. As the clock becomes sharper (i.e., the rise/fall time decreases), the size of the subsequent NOT stages is reduced to minimize the parasitic capacitance loading on the previous stage. To generate a complementary clock, the original clock path is divided into two paths, one having an additional NOT stage to invert the signal, as shown in Fig.3. This extra NOT stage adds delay to the complementary clock, which is compensated for by adjusting the number of transistors in the NOT stage, as shown in Fig.3.

D. Enhanced Isolation

Active cancellation circuitry increases the isolation during the hold mode by mitigating the parasitic leakage of the transmission gate. To characterize the effectiveness of the active cancellation circuitry, several simulations were performed. First, the transmitted power through the sampler was simulated in the track mode. Second, the transmitted power through the sampler was simulated in hold mode, and the active cancellation is removed. Finally, the transmitted power through the sampler was simulated again in hold mode, and the active cancellation is included. The difference between the transmitted powers in the track and hold modes is a measure of the isolation. As shown in Fig. 9, the isolation drops as the input frequency increases due to the higher leakage of the parasitic capacitances. When the active cancellation block was included, there was an increase of more than 30dB in isolation at 1GHz, which shows the effectiveness of the active cancellation circuitry. As explained in the measurement section, these results are validated throught the experiment.

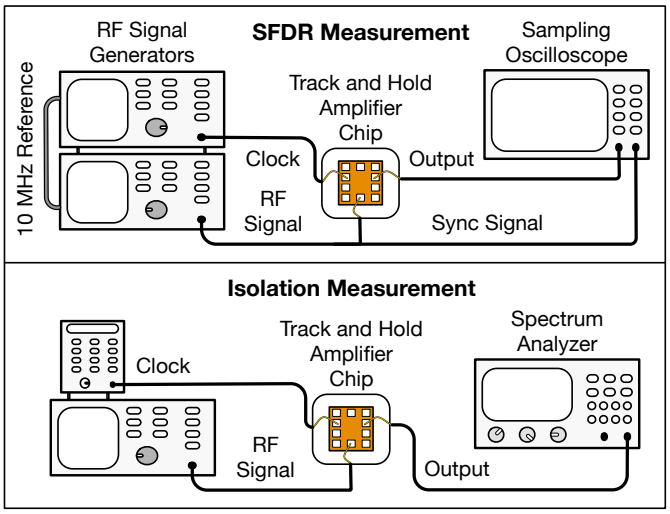

Fig. 12. Measurement setup for testing the Track and Hold Amplifier chip

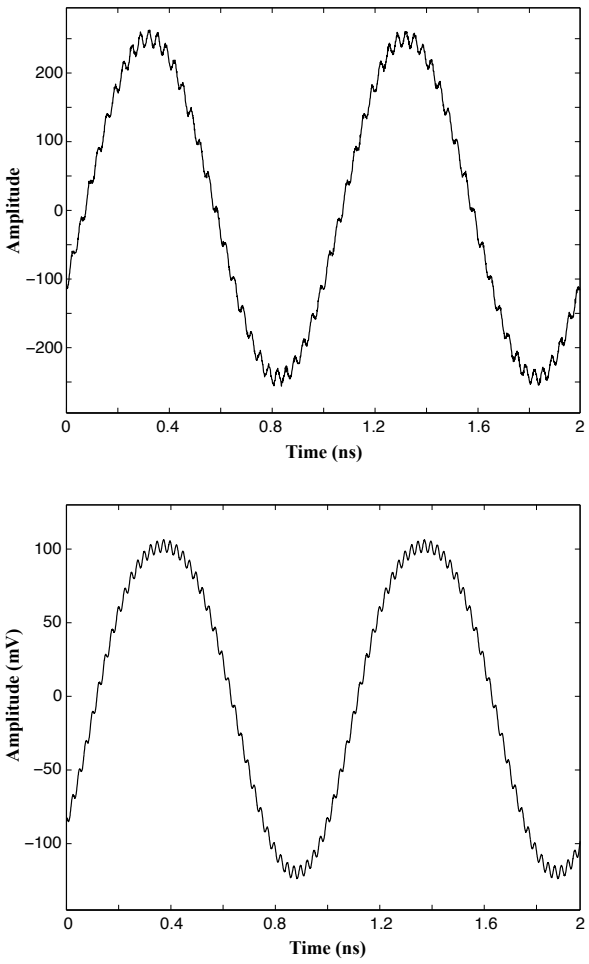

Fig. 13. Raw output of the Track-and-Hold Amplifier. Top figure shows 1GHz input signal sampled at 30GS/s and bottom figure shows 1GHz input signal sampled at 40GS/s

III. Measurement Results

A. Time-domain Measurement

Figure 12 shows the experimental setups used in time-domain and frequency-domain measurements. In the time-domain measurement, the track-and-hold chip was fed with two signals, one being the RF input signal and other being the sampling clock. Both the input signals were generated using an RF signal generator and synchronized with a 10MHz reference clock. The output of the chip was captured on a sub-sampling oscilloscope. The setup for the frequency-domain measurement, which determines the isolation, consisted of an RF signal generator to generate the input signal and a spectrum analyzer to determine the output power at different frequencies. In the isolation measurement, a DC voltage level was used to toggle between track and hold modes. All the RF signals were fed to the chip and captured using 67GHz RF probes.

The performance of the track and hold amplifiers is determined by measuring the spurious free dynamic range (SFDR) of the sampled signal over different sampling frequencies and input power levels. Fig. 13 shows the raw output of the amplifier. Fig. 13(top) shows the output of the chip for an input signal of 1GHz sampled at 30GS/s. Fig. 13(bottom) shows the output for the 1GHz sampled at 40GS/s.

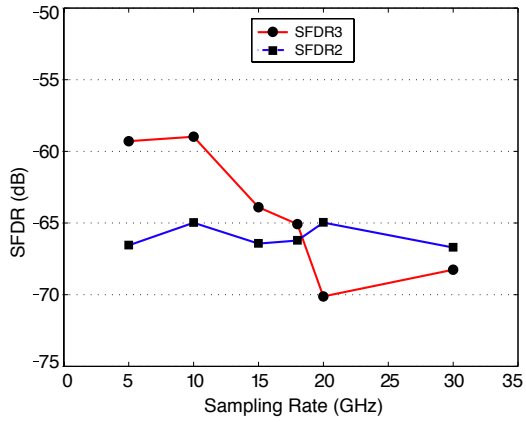

Fig. 10. Measured SFDR for 1GHz input signal sampled at different sampling frequencies

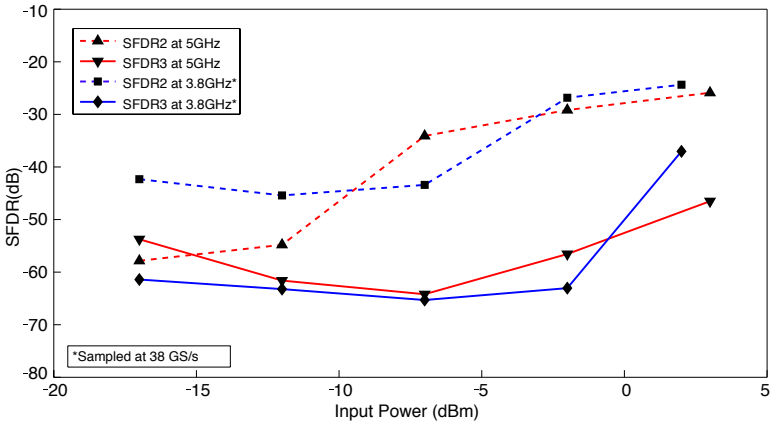

Fig. 11. Measured SFDR2 and SFDR3 versus input signal power at a sampling frequency of 40GS/s

IC Specification	This Work	[10]	[11]	[12]	[13]
Process	45nm SOI CMOS	130nm CMOS	180nm SiGe BiCMOS	130nm BiCMOS	90nm SiGe HBT
Die Specification	850umx450um	1mm^2	1.28x1.15mm^2	0.09mm^2	0.49mm^2
Supply Voltages	2.5V, 1V	1.8V	4V, 3.3V	1.2V	3.9V
Power Consumption	415mW	270mW	640mW	71mW	560mW
Sampler					
Input	Single-ended	Differential	Differential	Differential	Differential
Max Sampling Rate	>40GS/s	30GS/s	50GS/s	20GS/s	40GS/s
SFDR2	>72dB@ Fin=1GHz Fs= 40GS/s	SFDR=40dB@ Fin=1GHz Fs= 30GS/s	SFDR=42dBc@ Tone=30,30.1 GHz Fs=40GS/s	SFDR>32dB@ Fin=1GHz Fs= 20GS/s	>65dB@ Fin=1GHz Fs= 40GS/s
SFDR3	>66dB@ Fin=1GHz Fs=30GS/s				75dB@ Fin=1GHz Fs= 40GS/s
Isolation	>30dB@ Fin=1GHz	Not reported	Not reported	Not reported	Not reported
Droop Voltage	20uv/ns	10mv/ns	Not reported	40uv/ns	Not reported

TABLE I. COMPARISON WITH STATE OF THE ART

In the first experiment, the input frequency was fixed at 1GHz and the sampling frequency was varied from 5GHz to 30GHz. The sampled signal was averaged 128 times to reduce the noise of the oscilloscope, and then DFT was calculated to measure the SFDR. Fig. 10 shows the 2nd and 3rd harmonic SFDR for various sampling frequencies.

In a separate experiment, the linearity of the amplifier was shown by measuring SFDR at various input power levels. In this measurement, the sampling frequency was fixed at 40GS/s and the input power was swept at various frequencies. SFDR2 and SFDR3 are relatively flat for a wide range of input powers, as shown in Fig. 11. A droop voltage of 20μv/ns was observed for a sampled signal of 350mV. This is equivalent to 10-bit accuracy for a hold time of 10ns.

B. Frequency-domain Measurement

A high isolation between track and hold modes is for the performance of an ADC. To measure the is the amplifier was first put in the track mode. Then th frequency was swept from 100MHz to 10GHz, and the spectrum was recorded. Next, the amplifier was swit the hold mode, and the input frequency was swept aga difference in the output power levels, between the tra hold modes, was measured to calculate the isolation r The measured isolation is plotted in Fig. 14.

The results for this chip are compared with the s the art in Table I. The track-and-hold amplifier was fab using 45nm IBM CMOS SOI technology, it occupies of 850μm$\times$450μm including pads and 0.12 mm^2 witho The total power consumed by the chip was 415mW at sampling frequency. Finally, the chip micrograph is sh Fig.15.

IV. CONCLUSION

A 40GS/s track-and-hold amplifier was designed and fabricated in 45nm IBM CMOS SOI technology node. A novel active cancellation method is presented that mitigates the parasitic signal leakage through the sampling switch. This allows the sampler to operate at a higher input frequency without degrading the ENOB number. This architecture does not require a differential input. A single-ended input signal is fed to the chip and converted to a differential signal on the chip. In addition, an on-chip clock generation and sharpening circuit was used to convert a single-ended input clock to a differential one and to sharpen its rise/fall time. An SFDR3 of 62 dB [illegible]

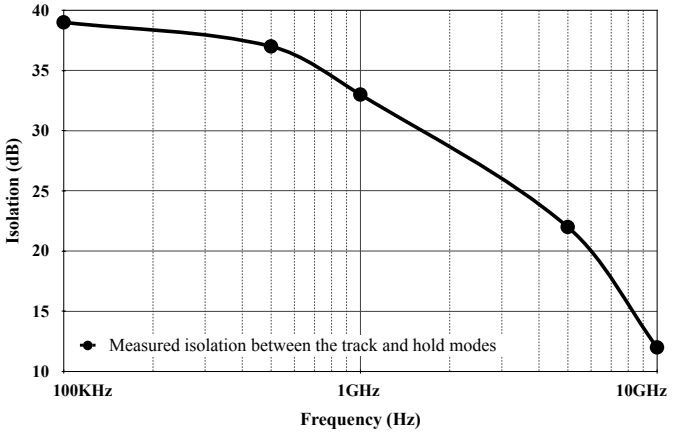

Fig. 14. Measured isolation between track and hold modes at various input frequencies

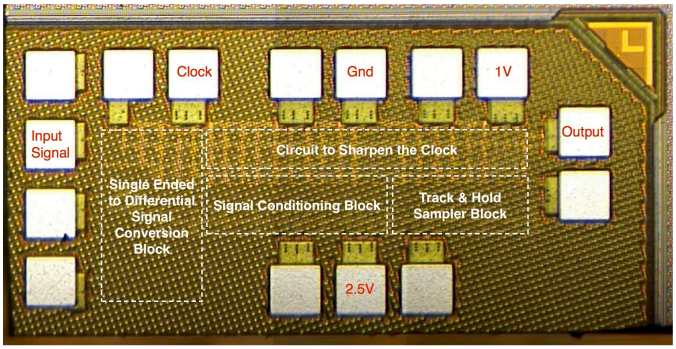

Fig. 15. Chip micrograph of Track-and-Hold Amplifier in 45nm IBM CMOS-SOI node, measuring 850μm×450μm including pads and 0.12 mm^2 without pads

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