A Single-Chip In-Band Full-Duplex Low-IF Transceiver with Self-Interference Cancellation

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Abstract — A 3.8-4.8GHz single-chip in-band full-duplex (FD) transceiver with self-interference cancellation (SIC) is reported. The RX has a noise figure (NF) of 3.1dB/6.3dB at 10MHz/50kHz IF with TX and SIC off. The 1/f noise corner is 60kHz, more than one order of magnitude lower compared to prior work. Moreover, for the first time, the operation of RX and SIC is demonstrated when a co-integrated TX is active at the same time and generating more than 20dBm output power. When TX and SIC are on, at -10dBm SI power, the NF is 6.8dB/11.1dB at 10MHz/50kHz IF. This is lower by 5.6dB/9.6dB at 10MHz/50kHz IF compared to the NF with SIC off.

Index Terms — Full-duplex, Transceiver, BiCMOS.

I. Introduction

In-band full-duplex (FD) transceivers have a broad range of applications including wireless communication, radar sensing, and spectroscopy. The performance of RX in these transceivers is significantly impacted by the self-interference (SI) caused by TX. Recently, several fully-integrated FD chips have been reported that offer self-interference cancellation (SIC) [1-5]. However, when characterizing the RX and SIC block, the prior work either used an off-chip TX, or significantly limited the TX output power (-18dBm in [1]). In a more practical situation, the RX and SIC block would be integrated with the TX on the same chip, and the TX would generate a considerably higher output power (targeted at >20dBm in this work). Therefore, it remains unclear how a FD RX and the associated SIC would behave under such conditions. Moreover, most of the previous work focused on wireless communication and utilized a mixer-first or current-mode mixer-first architecture. This architecture provides good RX linearity and reconfigurability, but the NF is poor at low IF. In many FD applications, such as radar sensing and spectroscopy, the RX IF frequency can be as low as tens of kHz [6]. Hence, existing SIC techniques are unsuitable in these situations. To the best knowledge of the authors, the only FD transceiver that targeted at low IF applications was reported in [5]. However, the RX NF in [5] was significantly deteriorated due to the large noise contribution from the SIC block.

In this work, a single-chip FD transceiver with SIC is reported. For the first time, the operation of the RX and SIC is demonstrated while a co-integrated TX is on and generating >20dBm output power. Moreover, low NF at low IF as well as high RX linearity is achieved by avoiding large voltage

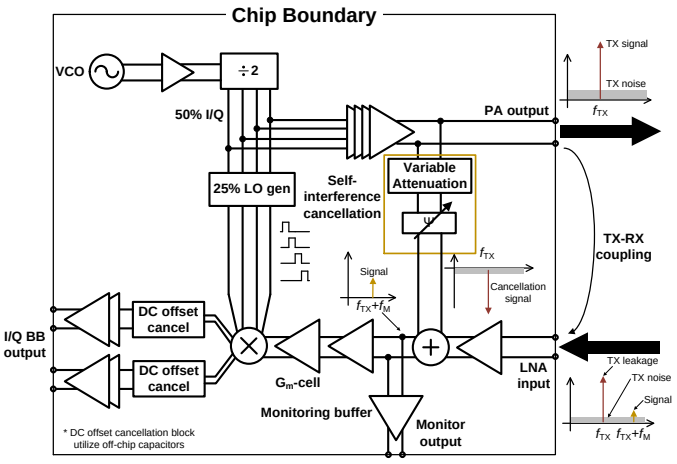

Fig. 1: Architecture of the single-chip transceiver with integrated self-interference cancellation.

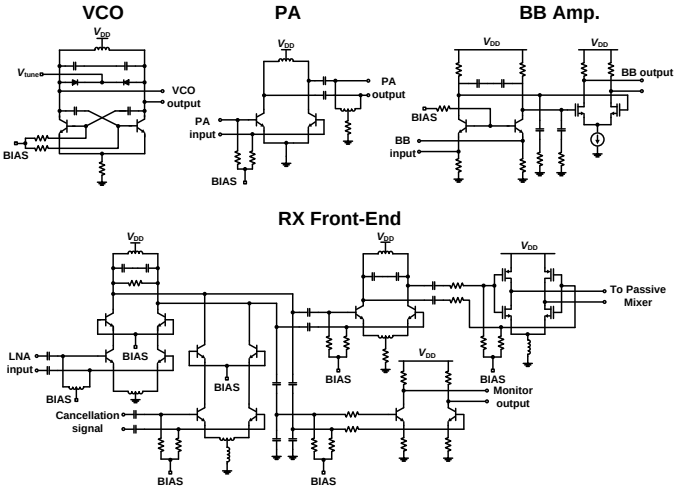

Fig. 2: The detailed schematic of the VCO, PA, baseband amplifier and the RX front-end.

amplification in the SIC block. When the TX and SIC are off, the RX achieves a measured NF of 3.1dB/6.3dB at 10MHz/50kHz IF with a 60kHz 1/f noise corner. This 1/f noise corner is more than one order of magnitude lower compared to prior work [3]. When the TX is on and TX SI is present, the RX SI P1dB is -20dBm. It increases to -8dBm with SIC on. At -10dBm SI power, the measured RX NF is 6.8dB/11.1dB at 10MHz/50kHz IF with SIC on. This is lower by 5.6dB/9.6dB at 10MHz/50kHz IF compared to the case

when SIC is off, demonstrating the functionality and importance of the SIC when a co-integrated TX is generating >20dBm output power.

II. Design of the Transceiver

In this section, the transceiver design is presented. Fig. 1 plots the architecture of the proposed FD transceiver. It is targeted at low IF FD applications, such as the magnetic resonance spectroscopy [6]. A VCO followed by a CML I-Q divider generates a TX signal ranging from 3.8GHz to 4.8GHz. It is then amplified by a set of amplifiers and delivered off-chip through a differential PA. In many spectroscopy applications [5-6], the desired RX signal experiences a frequency shift of f_M compared to the TX frequency. This frequency shift is caused by the magnetic field modulation or mechanical chopping [6]. In these applications, f_M typically ranges from tens to hundreds of kHz. In order to minimize the 1/f noise contribution of mixers and baseband amplifiers, instead of using a mixer-first design, the RX signal is strongly amplified before down-conversion. After this step, a G_m-cell converts the RF voltage into current, which is sent to passive mixers for down-conversion. The signal is then further amplified at baseband. The schematics of several major blocks of the transceiver are presented in Fig. 2.

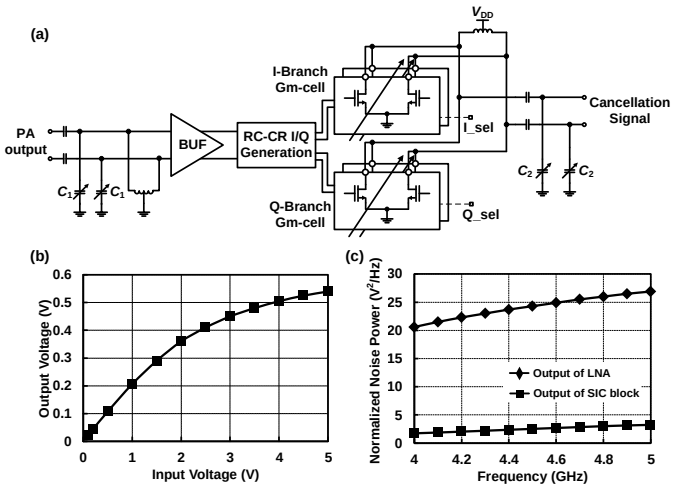

Fig. 3: (a) Schematic of SIC block. (b) Simulated output of the SIC block under different input voltages. (c) Simulated noise power at the LNA output and the SIC block output when the SIC gain is set at the maximum value.

During the operation of the transceiver, TX SI is present at the input of the RX. This raises the RX NF by saturating the amplifiers before down-conversion, thereby increasing the 1/f noise contribution from mixers and baseband amplifiers. To avoid these problems, SIC circuits were used in the previous work. In [2-4], the SIC used the mixer-based architecture, which injected large 1/f noise and was unsuitable for low IF applications. In [5], the SIC did not use a mixer-based architecture but still added a lot of noise to RX under large SI. This is because, in [5], the TX output was heavily attenuated before being sent to the SIC block. The SIC block then amplified the cancellation signal by as much as 20dB to cancel the large SI. This large voltage gain amplified the noise from the SIC block as well, deteriorating the RX NF and reducing the benefits of SIC.

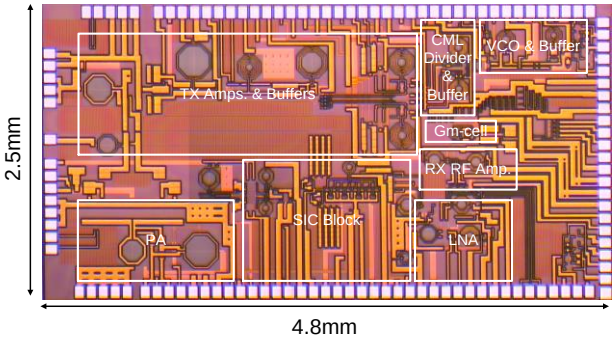

Fig. 4: Chip image with major blocks are labeled .

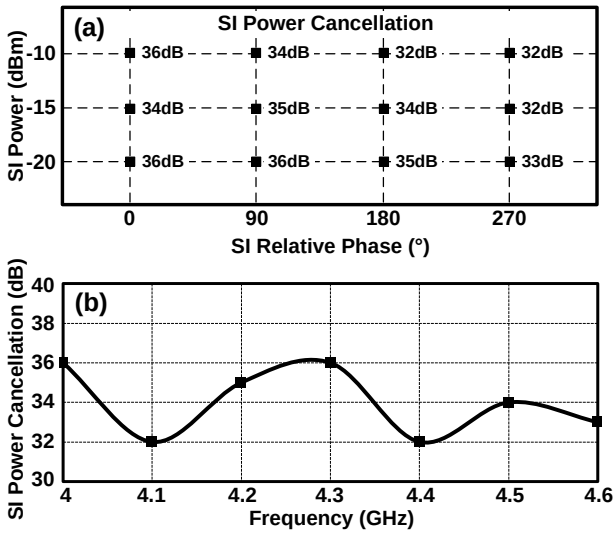

Fig. 5: (a) Measured SI cancellation under different SI power and phase. (b) Measured SI cancellation under different frequencies.

In this work, the main goal is to cancel the SI signal with minimum noise penalty. To achieve this goal, instead of attenuating the TX output first and amplifying it in the SIC block, the TX output is directly attenuated to the desired amplitude. This design minimizes the noise contribution from the SIC block by avoiding the large voltage amplification. However, the SIC block must be carefully designed to satisfy stringent linearity/reliability requirements due to the large voltage swing at its input. The schematic of the reported SIC block is presented in Fig. 3(a). At the input of the SIC block, a passive capacitive divider with tunable dividing ratio reduces the amplitude of the TX output to less than 1V. This enables the use of active devices in the following stages. In this work, the variable dividing range of the capacitive divider is 14dB in simulation. In order to further increase the tuning range of the amplitude of the cancellation circuit, variable gain stages are added in the following circuits. In this design, a buffer is used after the divider. The buffer is built with high-breakdown

TABLE I

PERFORMANCE COMPARISON WITH PRIOR ARTS

	RFIC 2014 [1]	ISSCC 2015 [2]	ISSCC 2015 [3] + RFIC 2015 [4]	RFIC 2015 [5]	This work
On-chip blocks	Transceiver	RX only	Transceiver	Transceiver	Transceiver
Operating freq.	0.1-1.5GHz	0.8-1.4GHz	0.15-3.5GHz	4.6-5.3GHz	3.8-4.8 GHz
TX output power	-18dBm	N.A.	13dBm	22dBm	**22dBm**
Maximum RX gain	55dB	42dB	24dB	41dB	46dB
RX NF with TX/SIC off	5-8dB	4.8dB	6.3dB	N.A.	**3.1dB (at 10MHz IF)**
RX NF at 50kHz IF with TX/SIC off	N.A.	N.A.	N.A.	N.A.	**6.3dB**
RX 1/f noise corner with TX/SIC off	N.A.	N.A.	2MHz	N.A.	**60kHz**
RX NF degradation when SIC is on (TX off)	N.A.	0.9-1.5dB	4-6dB	N.A.	**<0.6dB**
RX NF when co-integrated TX is on and SIC block cancels TX SI	10.5dB (-18dBm TX and SI power)	N.A.	N.A.	N.A.	**6.8dB/11.1dB at 10MHz/50kHz IF (22dBm/-10dBm TX/SI power)**
SI P1dB	-17.3dBm	-8dBm	N.A.	-8dBm	-8dBm
Technology	65nm CMOS	65nm CMOS	65nm CMOS	0.13µm BiCMOS	0.13µm BiCMOS

transistors to withstand the large voltage swing. After the buffer, an I-Q generator and a Cartesian phase shifter are used. Based on the simulation, the SIC block achieves a variable attenuation of -13dB to -33dB with a maximum output voltage of more than 500mV. As shown in Fig. 3(c), even at the maximum gain setting, the noise power at the SIC block output is considerably smaller than that at the LNA output, incurring a simulated noise penalty of only 0.2dB.

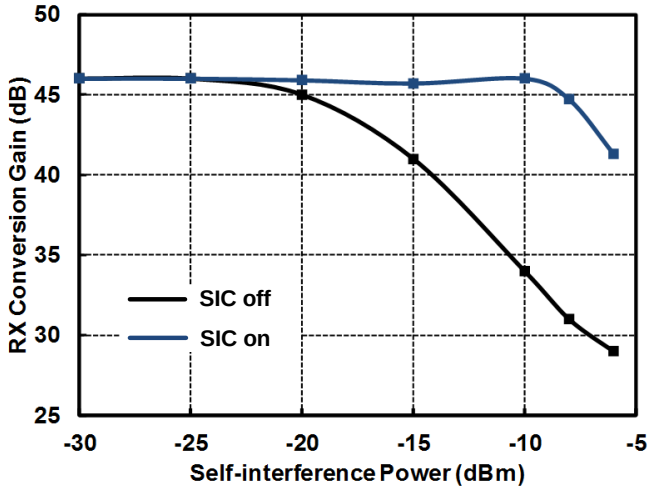

Fig. 6: Measured RX conversion gain with and without SIC.

III. MEASUREMENT RESULTS

The reported transceiver was fabricated in IBM 0.13µm BiCMOS process technology. Fig. 4 shows the chip micrograph. The TX includes an on-chip VCO, providing frequency tunability from 3.8GHz to 4.8GHz. The PA delivers a maximum differential output power of 22dBm. To characterize the performance of the RX and SIC block, the TX output is sent to the RX input through an external variable-gain attenuator and a phase shifter to mimic a wide range of TX SI. The RX achieves a conversion gain of 46dB without TX SI. The SI P1dB is -20dBm with the SIC off. When the SIC is on, the SI power can be reduced by at least 32dB. The power, phase, and frequency of the SI signal have been varied extensively to confirm that accurate cancellation can be achieved over a wide range of SI signal, as presented in Fig. 5. The measurement results for linearity of the RX is shown in Fig. 6. With SIC on, the SI P1dB of the RX increases by 12dB to -8dBm.

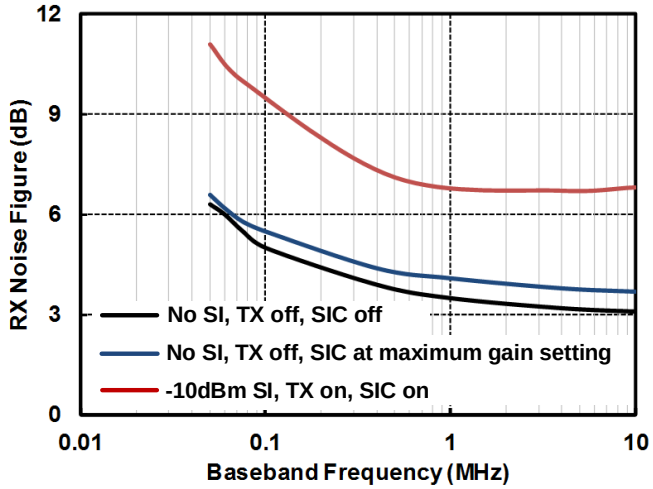

Fig. 7: Measured NF of the RX under various conditions.

The RX NF with and without the SIC block and TX is reported next. During the NF measurement, a stable external RF source is utilized as the LO to improve measurement accuracy, especially at low IF. As shown in Fig. 6, the RX achieves a NF of 3.1dB/6.3dB at 10MHz/50kHz IF, with the TX and SIC off. The 1/f noise corner is 60kHz. When the TX remains off but the SIC is turned on and set at the maximum gain, the noise penalty is within 0.6dB across all the IF. When

both TX and SIC are turned on and the TX SI is -10dBm at the RX input, the RX achieves a NF of 6.8dB/11.1dB at 10MHz/50kHz IF. This is lower by 5.6dB/9.6dB at 10MHz/50kHz IF compared to the NF when SIC is off.

Table I compares this work with previous publications that utilized SIC. It can be observed that the 1/f noise corner of the reported RX is considerably lower than prior works [1-5]. Moreover, the reported transceiver represents the first work that demonstrates the functionality of a FD RX and SIC when a co-integrated TX is generating more than 20dBm output power.

IV. Conclusion

In this work, a 3.8-4.8GHz single-chip in-band full-duplex transceiver with SIC is presented. The reported RX achieves more than one order of magnitude lower 1/f noise corner compared to prior works. Moreover, for the first time, the operation of RX and SIC block is demonstrated when a co-integrated TX is working simultaneously and generating more than 20dBm output power.

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