A 0.2-2.6GHz Instantaneous Frequency-to-Voltage Converter in 90nm CMOS

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***Abstract* — This paper presents a novel architecture for detecting the frequency of sinusoidal or square-wave signals with a short settling time. The architecture is based on detecting consecutive rising edges of the input signal and is able to generate a dc voltage proportional to the signal frequency in a time as short as only one input cycle. Measurements show that it can detect signals with frequencies up to 2.6 GHz. The chip is fabricated in a 90nm CMOS process. The total die area is 0.132 mm^2 and consumes 6.5 mW from a 1-V power supply.**

***Index Terms* — CMOS integrated circuits, cognitive radio, frequency conversion, frequency-locked loops, reconfigurable architectures.**

I. Introduction

Advances in wireless communication systems and rapid occupation of various radio frequency bands have created a need for smart reconfigurable systems and sensors that can detect the operating frequency of the received electromagnetic waves. In recent years, significant amount of work has been done on developing cognitive radio systems that can sense used RF channels in the environment and allocate unused frequency bands for their operation. A frequency detector circuit is a key enabler for the front-end of such systems that can be used to build frequency-locked loops, as well as self-tuned reconfigurable receivers. The output settling time in such circuits needs to be short so that a fast spectrum sensing can be achieved for the frequency-hopping purpose.

In this work, we have designed and implemented a high-speed frequency-to-voltage converter that can detect the instantaneous frequency of the input signal with a 2.6 GHz bandwidth. This circuit can be used in cognitive radio systems to fulfill the need for sensing used frequency channels. It is also an essential block in frequency-locked loops [1]. The proposed frequency detector is based on the idea of detecting consecutive rising edges of the incoming signals to make the detection faster. [1]-[2] presented methods based on charging one capacitor and discharging it to another capacitor using two or three switches. However, this architecture requires several cycles to converge the output voltage to the final dc value, causing a large settling time and limiting the frequency-locked loop performance. While in this work, the proposed architecture can generate its final output in one cycle of the input, i.e. 1- ns for a 1-GHz input. Implementing the architectures in [1]-[2] also need several control signals to adjust timings, which are eliminated in this work. [3]-[4] have also presented a frequency-to-current converter capable of tuning a VCO but they cannot achieve high-enough frequency for many wireless applications.

The remainder of this paper describes the proposed architecture. Section II describes the circuit details for converting a signal frequency to a dc voltage. Section III reports the test setup and measurement results. Finally, Section IV concludes this paper.

II. Circuit Architecture

In this section, the architecture of the proposed high-speed frequency-to-voltage converter is presented. In order to avoid the effect of analog input amplitude on the output voltage, we apply the input signal to a high-gain amplifier to saturate it and then utilize a digital method to measure the frequency. This method is based on detecting the consecutive rising edges of a signal and charging a capacitor during this time interval so that the final voltage of the capacitor would be proportional to one period of the input signal. [1]-[2] have used accumulating methods, which take several cycles to produce the desired output and thus have large settling times. However, in the proposed method, the instantaneous frequency is measured after one cycle, which is the fastest possible settling time. The circuit has a certain operating bandwidth (2.6 GHz) but the frequency range can be extended by adding a mixer and shifting the center frequency.

The detailed circuit of the proposed architecture is illustrated in Fig. 1. After introducing a high gain to the sinusoidal input, a sharp square-wave signal is generated. The generated square-wave signal passes through two positive edge detectors, which detect the first and second rising edges of the signal. The system has a reset input, which starts the frequency measurement. The second edge detector has an enable input, which is generated after the first edge detector detects the first rising edge. The output capacitor is connected to a current source and can only be charged when both of the PMOS switches (M_1 and M_2) are on. The charging happens only between the first two rising edges of the input so the final output voltage becomes proportional to one period of the signal. After this step, the

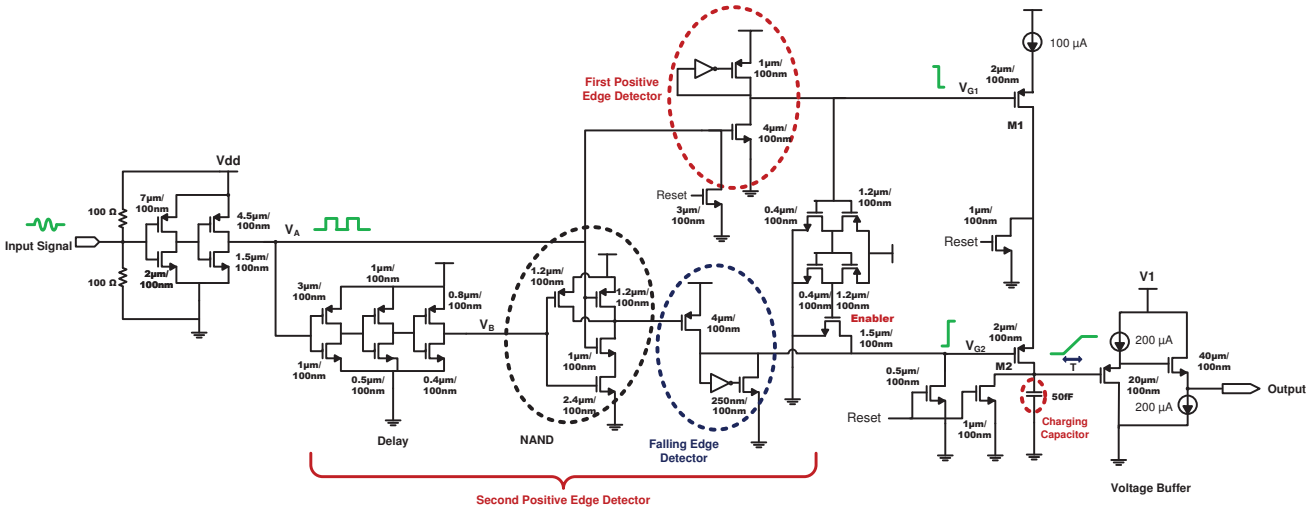

Fig. 1. Proposed frequency-to-voltage converter circuit.

output voltage remains constant until the reset input resets the operation of the system.

The edge detector circuits may conventionally be implemented using digital latches and flip-flops but they do not provide enough speed and consume high power. In the proposed edge detector circuits, only three transistors are employed with a feedback topology. The output voltage of this block will be saturated when a transition from 0V to 1V occurs in the input signal. The second edge detector has a larger delay time on its path to make sure that it does not detect the first rising edge of the signal. There is a NAND gate right between the delay line and the second edge detector that generates a pulse with the same frequency but a smaller duty cycle than the input signal. This block is used to limit the operation of the second edge detector to a much shorter time so that its output does not saturate during the rest of the first cycle. A brief timing diagram describing the transitions of each node voltage is shown in Fig. 2.

A voltage buffer is used after the output node to drive the 50-Ω input impedance of the oscilloscope. This buffer consists of two stages of source followers. The PMOS source follower increases the level of the output by a certain amount, which is then cancelled by the NMOS source follower with the same level shift. So the output voltage level will not change from its expected value, while it can drive the 50-Ω load.

III. Measurement Results

The fabricated frequency-to-voltage converter is characterized using a sampling oscilloscope (Agilent DCA-X 86100D) and SMA cables/connectors. A block diagram of the test setup is illustrated in Fig. 3. An RF signal generator (HP 8340B) and a low-frequency arbitrary waveform generator (Agilent 33250A), which is used for generating the reset signal, are synchronized using a 10-MHz reference signal.

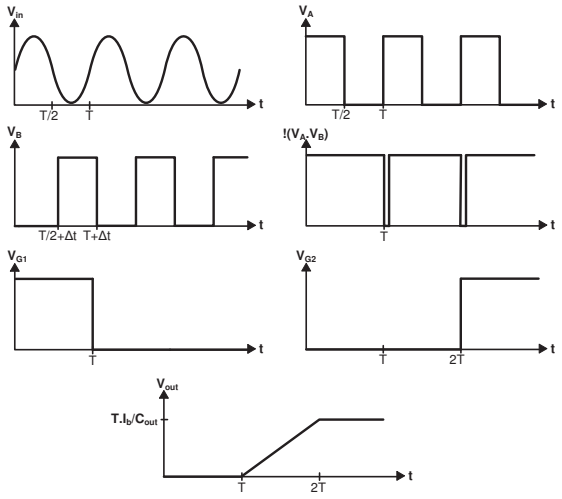

Fig. 2. Timing diagram of key circuit nodes.

A 10-MHz reset signal is generated with the AWG to reset the operation of the circuit every 100 ns. Applying a 1-GHz signal to the circuit input will result in an output voltage converging to 240 mV, as shown in Fig. 4. The transition phase of the output voltage is also shown in Fig. 3, which demonstrates a charging time equal to one input cycle, i.e. 1 ns at a GHz. Fig. 5 illustrates how the output voltage changes with increasing the input signal frequency. The strong correlation between these two parameters proves that the output voltage of the circuit can be used to

calculate the signal frequency. Table I compares this work with the prior art.

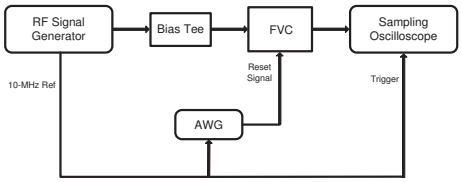

Fig. 3. Block diagram of the test setup.

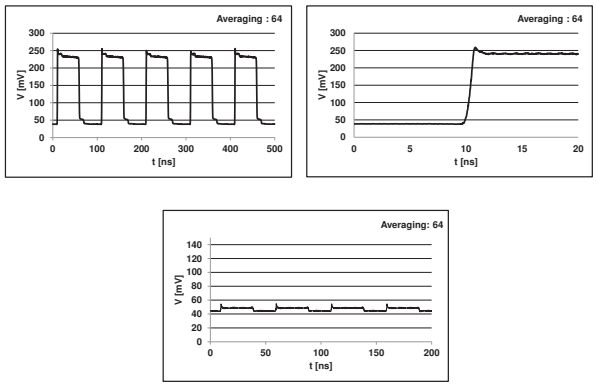

Fig. 4. Measured time-domain output waveform for a 1-GHz input and a 10-MHz reset signal, with two different timespans (top) and a 2.6-GHz input (bottom).

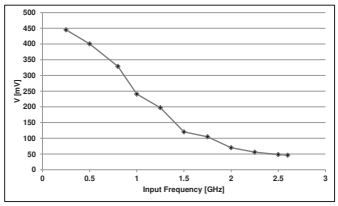

Fig. 5. Measured output voltage versus the sinusoidal input frequency.

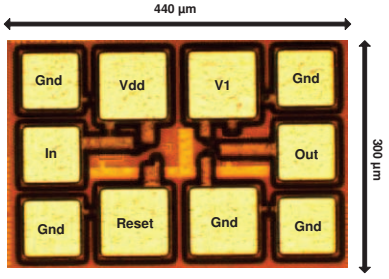

Fig. 6. Micrograph of the chip.

IV. Conclusion

In this paper, a frequency-to-voltage converter with a single-cycle settling time is reported. It employs two novel edge detector blocks, several digital gates and a buffer that drives a 50-Ω load. The converter operates with input frequency range up to 2.6 GHz, while consuming 6.5 mW from a 1-V power supply. The output voltage changes from 440 mV to 45 mV by varying the input frequency from 200 MHz to 2.6 GHz. This work is fabricated in a 90nm CMOS process technology. The size of the chip, including the pads, is 440 µm × 300 µm. A micrograph of the chip is shown in Fig. 6.

TABLE I
Comparison with Prior Art

	This work	[1]	[4]
Maximum Frequency	**2.6 GHz**	5 GHz	1.15 GHz
Settling Time	**1 ns @ 1 GHz (one cycle)**	~100 ns @ 83.3 MHz	500 ps @ 1.15 GHz
Minimum Input Power	**-17.7 dBm @ 1 GHz**	N/A	N/A
Chip Area	**0.132 mm^2 (with bondpads)**	0.22 mm^2 (FLL)	0.015 mm^2 (estimated, with VCO)
Supply Voltage	**1 V**	N/A	1.8 V
Power Consumption	**6.5 mW**	N/A	3.6 mW
Technology	**90nm CMOS**	350nm CMOS	180nm CMOS

Acknowledgement

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